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Speed-Electromotive-Force-Adaptive Voltage-Level Selection for Four-Level Switched Reluctance Motor Drives with Reduced Torque Ripple and Improved Efficiency

Research paper

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Abstract: A speed-electromotive-force (EMF)-adaptive minimum-level voltage selector with an explicit voltage-margin deadband is presented for a four-phase 8/6 switched reluctance motor driven by a four-level shared-switch converter with a bidirectional buck–boost front end. Phase-voltage states are $V_{dc}+V_{cap}$, V_{dc}, 0 and $-V_{cap}$. An experimentally identified non-linear flux-linkage map $\hat{\lambda}(\theta,i)$, obtained as a function of mechanical rotor position and phase current, supplies the incremental-inductance and position-dependent speed-EMF information required by the online voltage-demand calculation, from which the controller estimates the voltage needed for a bounded commanded current slope; the boosted level is applied only when the estimated voltage demand exceeds the main-source level by the prescribed margin, while $-V_{cap}$ is prioritised after turn-off to hasten current extinction and route winding energy to the auxiliary link. Attainable current slopes, front-end volt–second balance, auxiliary-link sizing, two-group current reconstruction and peak device-voltage stresses are derived. Equal-condition benchmarking at 50 V main and 100 V auxiliary links gives maximum torque-ripple reductions of 6.5 percentage points over the speed sweep and 3.5 percentage points over the load sweep, together with a 2.0-percentage-point improvement in the converter-orientated efficiency metric at rated speed relative to the asymmetric half-bridge (AHB) baseline. Reduced-voltage tests on a 0.9 kW prototype demonstrate multilevel current regulation at 500 and 1,200 r/min, regenerative braking at 900 r/min, balanced phase currents at 900 r/min and same-group non-overlap. A measured AHB reference on the same machine provides a hardware comparison at low and high speed.

Keywords: *switched reluctance motor • four-level converter • voltage-demand control • current reconstruction • energy recovery*

1. Introduction

Switched reluctance motors (SRMs) are increasingly considered for traction, aerospace, starter–generator and industrial drives because their magnet-free rotor is mechanically robust, tolerant of high temperature and compatible with wide-speed operation. Their doubly salient magnetic structure nevertheless produces non-linear phase inductance, discrete torque production, acoustic excitation and pronounced torque ripple, so the converter topology and the current-control strategy together determine the usable torque–speed envelope (Bostanci et al., 2017; Pires et al., 2020; Abdel-Aziz et al., 2024).

Two operating regimes are particularly demanding. At high speed, the position-dependent speed electromotive force (EMF) and the shortened conduction interval restrict current build-up, so a limited DC-link voltage cannot force the commanded current before the poles overlap; the drive then degenerates into single-pulse operation, and the current reference is no longer tracked. After turn-off, a slowly decaying tail current can extend beyond the positive

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inductance-slope region, producing negative torque together with additional copper and semiconductor losses. Both effects are governed by the voltage that the converter can impose on the winding during magnetisation and demagnetisation, and both are therefore addressable at the level of the power stage rather than only at the level of the torque controller.

The asymmetric half-bridge (AHB) remains the reference converter because it provides independent phase control and the three states $+V_{dc}$, 0 and $-V_{dc}$. Its magnetisation and demagnetisation rates are, however, both fixed by the single DC-link voltage and cannot be raised transiently when the speed EMF grows. C-dump and improved-recovery converters increase the available negative voltage and recycle part of the phase energy, but they add a recovery path that must process the full demagnetisation energy (Mir et al., 1997; Tomczewski and Wrobel, 2014). Reduced-switch regenerative structures improve current extinction with fewer controlled devices, although their usable voltage states and phase-overlap constraints remain topology dependent (Rana and Ravi Teja, 2022).

Multilevel and voltage-boosting converters address the high-speed limitation without operating every device continuously from an elevated DC link. Representative developments include three-level neutral-point-clamped and integrated multilevel structures (Peng et al., 2017; Gan et al., 2017), a reduced-switch grid-fed multilevel converter designed to improve magnetisation and demagnetisation (Chaurasiya et al., 2023) and an integrated converter that combines multilevel operation with grid-to-vehicle charging (Shah and Payami, 2023). More recent work has introduced a four-level shared-switch converter with a buck–boost recovery stage (Chithrabhanu and Vasudevan, 2025), a five-level SRM converter with coordinated topology and control analysis (Ge et al., 2025), a reconfigurable four-level T-type fault-tolerant converter (Wang et al., 2025) and a high-voltage shared-leg neutral-point-clamped inverter that reduces the switch, diode, gate-driver and current-sensor counts while retaining three-level operation (Yousefi-Darani and Narimani, 2026). These studies confirm the benefits of additional voltage levels, but their principal emphasis is on topology, voltage balancing, fault tolerance, component reduction or system integration rather than on *deciding* which level to apply at each instant.

Control-orientated approaches reduce torque pulsation through torque sharing, predictive control, direct torque control or multilevel hysteresis bands (Kimpara et al., 2022; Reddy et al., 2020; Deepak et al., 2025). Two-current-sensor integration has also been demonstrated for four-phase drives when the converter and phase schedule permit unambiguous current assignment (Chen et al., 2019). The authors' earlier three-level converter study used elevated negative voltage for rapid demagnetisation (Mir and Santra, 2026); it did not compute the instantaneous positive phase-voltage demand or select the minimum sufficient positive level online.

The unresolved issue addressed here is therefore not the existence of a four-level shared-switch converter but the absence—among the cited structures—of an explicit online rule that fuses current error, rotor position, speed and non-linear magnetic information to decide whether the normal source voltage is sufficient. A current-error-only law tends to request the boosted state unnecessarily at low speed, where it yields no benefit but commutates against the full stacked link and therefore incurs the highest switching energy, or too late at high speed, after the speed EMF has already collapsed the available current slope. In both cases the extra voltage level is used inefficiently. This paper closes that gap through the following contributions:

1. A flux-map-based voltage-demand calculation (Section 3.1) that retains the normal positive level while the estimated demand remains within the prescribed voltage-margin deadband and engages the boosted level only when additional headroom is required;
2. A prioritised four-state switching law (Section 3.2) that cleanly separates boosted excitation, normal excitation, zero-voltage regulation and negative-voltage energy recovery, with demagnetisation given the highest priority, together with an analysis of the minimum-level policy subject to the voltage-margin deadband and of its sensitivity to flux-map error (Section 3.3);
3. Auxiliary-link voltage and capacitance design relations, an explicit sensing-error interpretation for two-group current reconstruction, and closed-form peak device voltage-stress relations for both the main and the front-end converter, followed by a hardware-requirement comparison with the AHB (Sections 4.2–4.6); and
4. Equal-condition benchmarking against AHB and C-dump baselines, complemented by reduced-voltage experimental demonstrations of dynamic transitions, motoring at two speeds, regenerative braking, balanced four-phase operation and a measured AHB reference on the same machine (Section 5).

2. SRM Model and Current-Slope Requirement

2.1. Per-phase electrical model

For one phase, the non-linear voltage equation is

$$v_{ph} = Ri + \frac{d\lambda(\theta,i)}{dt} = Ri + L_{inc}(\theta,i)\frac{di}{dt} + e_\theta(\theta,i,\omega), \tag{1}$$

where

$$L_{inc} = \frac{\partial\lambda}{\partial i},\ e_\theta = \omega\frac{\partial\lambda}{\partial\theta},\ \frac{di}{dt} = \frac{v_{ph} - Ri - e_\theta}{L_{inc}}. \tag{2}$$

Here v_{ph} is the phase terminal voltage, R is the phase resistance, i is the instantaneous phase current, $\lambda(\theta,i)$ is the non-linear phase flux linkage, θ is the rotor position and ω is the mechanical angular speed. The incremental inductance $L_{inc} = \partial\lambda / \partial i$ and the position-dependent speed EMF $e_\theta = \omega\partial\lambda / \partial\theta$ both vary strongly with position and saturation, which is precisely why a fixed link voltage is a poor match to the winding over a wide speed range.

The per-phase equivalent circuit that realises Eq. (1) is drawn in Figure 1. Eq. (2) shows that, at a given operating point, the current slope di / dt is set entirely by the *headroom* between the applied voltage v_{ph} and the internal drops $Ri + e_\theta$. Because e_θ scales with ω, that headroom collapses as speed rises even though the winding itself is unchanged; enlarging it on demand, and only on demand, is the single objective of the proposed four-level stage.

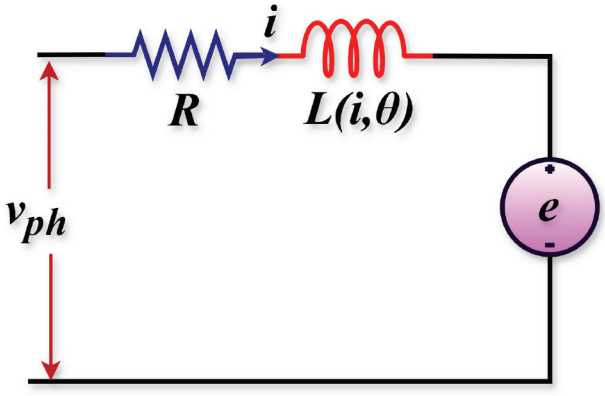


Figure 1. Per-phase equivalent circuit of the SRM. The converter impresses v_{ph} across the series combination of the winding resistance R, the non-linear incremental inductance $L_{inc}(\theta,i)$ and the speed-EMF source e_θ, , with the phase current i referenced into the positive terminal. EMF, electromotive force; SRM, switched reluctance motor.

2.2. Torque and the four current slopes

The electromagnetic torque follows from the magnetic co-energy,

$$T_e(\theta,i) = \left.\frac{\partial W_c'(\theta,i)}{\partial\theta}\right|_i,\ W_c'(\theta,i) = \int_0^i \lambda(\theta,\iota)\,d\iota, \tag{3}$$

where T_e is the electromagnetic torque, W_c' is the magnetic co-energy and ι is a dummy current variable. Eq. (3) reduces to $T_e \approx 1/2 i^2 \partial L / \partial\theta$ in the unsaturated linear approximation, which makes explicit that torque is produced only while the current occupies a rising-inductance region; current that persists into the falling-inductance region after turn-off produces braking torque and must therefore be extinguished quickly.

Substituting the four converter terminal voltages into Eq. (2) gives the four attainable current slopes

$$i_1 = \frac{V_{dc} + V_{cap} - Ri - e_\theta}{L_{inc}}, \quad i_2 = \frac{V_{dc} - Ri - e_\theta}{L_{inc}},$$
$$i_3 = \frac{-Ri - e_\theta}{L_{inc}}, \quad i_4 = \frac{-V_{cap} - Ri - e_\theta}{L_{inc}}. \tag{4}$$

Here i_1–i_4 are the slopes produced by the boosted-magnetisation, normal-magnetisation, zero-voltage and demagnetisation states, respectively, and an overdot denotes a time derivative; V_{dc} is the main DC-source voltage and V_{cap} is the auxiliary-capacitor voltage. The AHB slopes are recovered from Eq. (2) with $v_{ph} = \pm V_{dc}$.

Two consequences of Eq. (4) are used throughout the paper. First, relative to an AHB fed from the same main source, the boosted state raises the available positive slope by exactly V_{cap} / L_{inc}, and, because $V_{cap} > V_{dc}$ in this design, the $-V_{cap}$ state shortens extinction relative to $-V_{dc}$. With the $2:1$ auxiliary-to-main ratio adopted here, and neglecting $Ri + e_\theta$ only for a first-order comparison, the ideal voltage-driven contribution to the leading-edge slope is three times the AHB value, and the negative applied voltage is twice as large. The measured waveforms in Section 5.5 exhibit the corresponding current-rise and current-decay trends predicted by the ordered voltage states. Second, the four slopes are strictly ordered,

$$i_1 > i_2 > i_3 > i_4, \tag{5}$$

independently of the operating point, because the numerators differ by the fixed increments V_{cap}, V_{dc} and V_{cap} while the denominator is common. Ordering Eq. (5) makes a *minimum-level* selection meaningful: the states form a monotone ladder, so the lowest state that satisfies the ideal voltage demand is unique. The implemented selector of Section 3 adds the explicit margin ΔV_s around the normal-to-boosted transition to suppress state chatter.

Before introducing the finite voltage set, Figure 2 establishes the mechanical rotor-angle convention used to identify the positive-torque region and the common firing schedule. The four hardware states that realise the ordered slopes of Eq. (4) are then shown in Figure 3 and Table 1, so their physical meaning is available directly alongside the current-slope derivation.

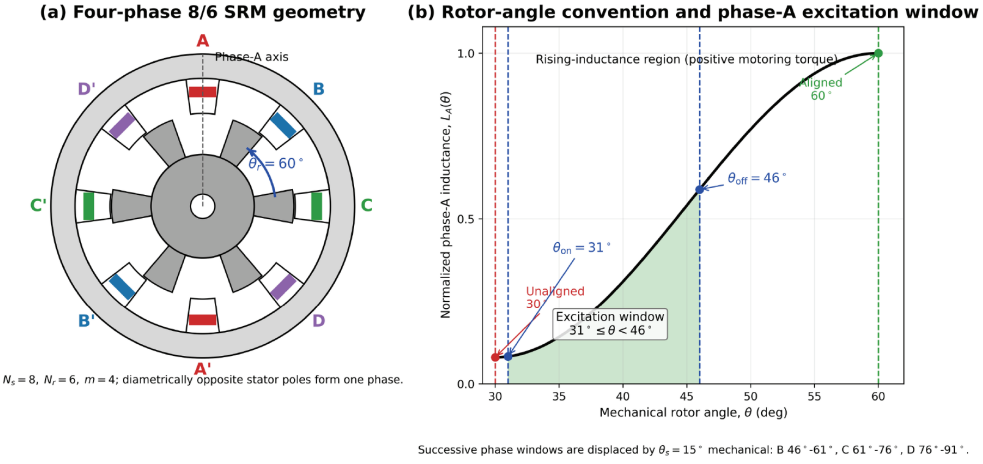


Figure 2. Four-phase 8/6 SRM geometry and rotor-angle convention: (a) eight-stator-pole/six-rotor-pole cross-section with diametrically opposite stator poles forming phases A–D; and (b) phase-A mechanical-angle reference showing the unaligned position at 30°, the aligned position at 60° and the implemented excitation interval $\theta_{on} = 31^\circ$ to $\theta_{off} = 46^\circ$. Successive phase windows are displaced by 15° mechanical and interpreted periodically over the 60° rotor-pole pitch. SRM, switched reluctance motor.

The four ordered current slopes in Eq. (5) correspond directly to the four motor-side switching states of Figure 3 and Table 1. This establishes the physical voltage state associated with each analytical slope before the voltage-selection law is introduced.

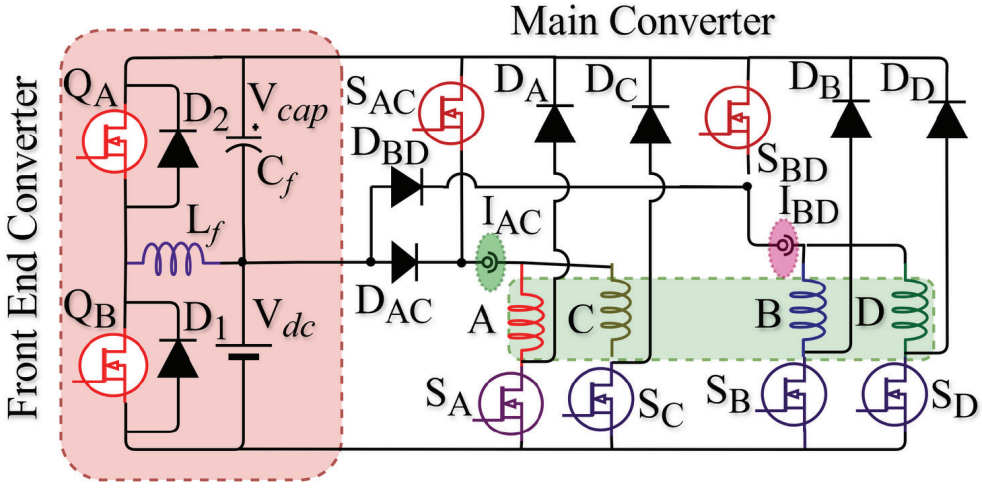


Figure 3. Four-level front-end-assisted shared-switch converter for the four-phase 8/6 SRM. The stacked DC links provide the voltage potentials 0, V_{dc} and $V_{dc}+V_{cap}$, from which the four phase-voltage states are synthesised. Phases A and C share the switch S_{AC} and the single current sensor I_{AC}; phases B and D share S_{BD} and I_{BD}. SRM, switched reluctance motor.

Table 1. Phase-A motor-side switching states.

State	S_A	S_{AC}	Phase voltage	Function and resulting slope
1	ON	ON	$V_{dc}+V_{cap}$	Boosted magnetisation; steepest positive slope i_1
2	ON	OFF	V_{dc}	Normal magnetisation; AHB-equivalent slope i_2
3	OFF	ON	0	Freewheel/clamp; natural decay i_3
4	OFF	OFF	$-V_{cap}$	Diode-assisted demagnetisation and recovery; fastest extinction i_4

AHB, asymmetric half-bridge.

2.3. Rotor-angle convention and phase excitation windows

For the four-phase 8/6 SRM, the mechanical rotor-pole pitch and the displacement between successive phase excitation windows are

$$\theta_r = \frac{360^\circ}{N_r} = \frac{360^\circ}{6} = 60^\circ,\ \ \theta_s = \frac{360^\circ}{mN_r} = \frac{360^\circ}{4\times 6} = 15^\circ, \tag{6}$$

where $N_r = 6$ and $m = 4$. The controller uses the mechanical rotor position referenced to the calibrated encoder zero. In the adopted magnetic convention, phase A is unaligned at 30° and reaches the subsequent aligned position at 60°; hence the interval between these positions is the rising-inductance region for positive motoring torque. The implemented phase-A excitation window is

$$\theta_{on} = 31^\circ,\ \ \theta_{off} = 46^\circ, \tag{7}$$

and the B-, C- and D-phase windows are displaced successively by 15° mechanical. The same $31^\circ / 46^\circ$ base schedule is used for the proposed converter, AHB and C-dump cases, so that the comparison isolates converter voltage capability and voltage-level selection rather than independent firing-angle optimisation.

The geometry and phase-A reference used by these definitions are shown in Figure 2; the figure separates the global mechanical rotor angle from the local magnetic aligned/unaligned positions and shows the implemented 31°–46° excitation window.

3. Speed-EMF-Adaptive Voltage Selection

3.1. Voltage-demand computation

The measured rotor position, mechanical speed and phase current index an offline flux-linkage map $\hat{\lambda}(\theta,i)$, stored as a uniform two-dimensional table in on-chip flash and addressed by bilinear interpolation. Finite differences of the map provide the estimated incremental inductance $\hat{L}_{inc}$ and the position-dependent speed EMF $\hat{e}_{\theta}$.

3.1.1. Experimental identification of the magnetic lookup table (LUT)

The non-linear phase flux-linkage characteristic used by the controller was experimentally identified for the investigated 0.9-kW four-phase 8/6 SRM over one complete 60° mechanical rotor-pole pitch and the required phase-current range. At each locked mechanical rotor position θ_k, the selected phase was initially de-energised and then excited while the phase terminal voltage $v_{ph}(t)$ and phase current $i(t)$ were acquired simultaneously. Using the measured phase resistance R, the corresponding flux linkage was reconstructed from the winding-voltage relation,

$$\lambda\left(\theta_k, i(t)\right) = \int_0^t \left[v_{ph}(\tau) - Ri(\tau)\right] d\tau, \tag{8}$$

which is the standard voltage-integration relation used for SRM flux-linkage identification (Bilgin et al., 2019). Repeated measurements were obtained over the required current range and rotor positions; records at each operating point were averaged before interpolation. The resulting experimental magnetisation data form the two-dimensional relationship $\lambda = \lambda(\theta,i)$, with mechanical rotor position and phase current as the independent variables. The identified data were resampled onto the uniform controller grid

$$\theta = 0^{\circ}:1^{\circ}:60^{\circ},\ \ i = 0:0.5:20\,|\,\mathrm{A}, \tag{9}$$

yielding a 61×41 (2,501-point) lookup table. One rotor-pole pitch is sufficient because the phase magnetic characteristic is periodic over 60° mechanical. Bilinear interpolation is used between adjacent stored grid points during real-time operation. The quantities required by the voltage-demand law are obtained from local finite differences of the identified map,

$$\hat{L}_{inc}(\theta,i) = \frac{\partial\hat{\lambda}}{\partial i},\ \ \hat{e}_{\theta}(\theta,i,\omega) = \omega\left.\frac{\partial\hat{\lambda}}{\partial\theta}\right|_{\mathrm{rad}}. \tag{10}$$

Although the stored LUT is indexed in mechanical degrees, the position derivative used in the speed-EMF calculation is converted to a per-radian derivative before multiplication by the mechanical angular speed ω in rad/s, that is,

$$\left.\frac{\partial\hat{\lambda}}{\partial\theta}\right|_{\mathrm{rad}} = \frac{180}{\pi}\left.\frac{\partial\hat{\lambda}}{\partial\theta}\right|_{\mathrm{deg}}. \tag{11}$$

This keeps $\hat{e}_{\theta}$ dimensionally consistent in volts. Figure 4 summarises the experimental identification procedure and the resulting two-dimensional flux-linkage surface.

The current error and the bounded commanded slope are

$$\varepsilon_i = I_{ref} - i,\ i^{\star} = \mathrm{sat}\left(k_s\varepsilon_i, -i_{max}, i_{max}\right), \tag{12}$$

where k_s is the slope-control gain and $\dot{i}_{max}$ limits the requested transient. The corresponding phase-voltage demand is obtained directly from the model Eq. (1),

$$v_{req} = Ri + \hat{e}_{\theta} + \hat{L}_{inc}\,i^{\star}. \tag{13}$$

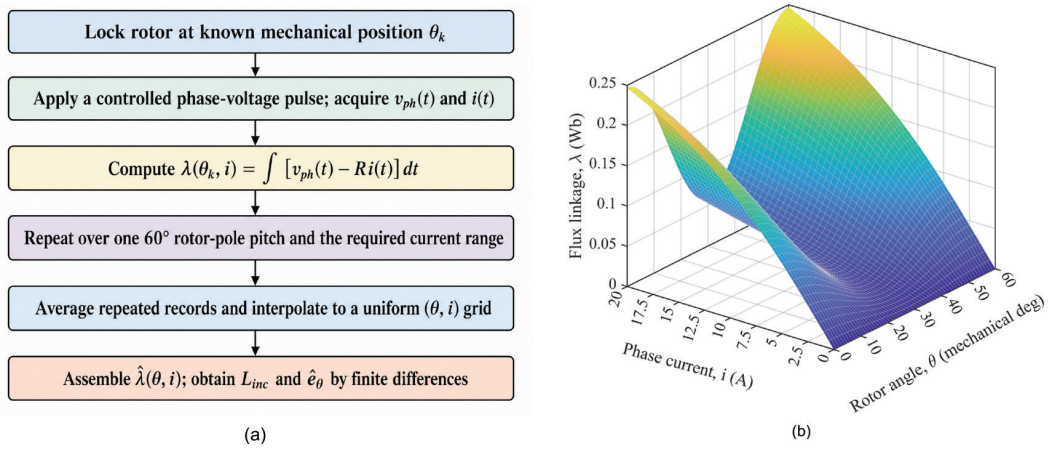


Figure 4. Experimental identification of the magnetic characteristics of the investigated 0.9-kW four-phase 8/6 SRM: (a) locked-rotor phase-voltage/current acquisition and flux-linkage reconstruction procedure and (b) experimentally identified $\lambda(\theta, i)$ surface over one 60° mechanical rotor-pole pitch and the $0-20$ A phase-current range. The identified data are resampled onto a 61×41 rotor-position/current grid for online bilinear interpolation in the voltage-demand controller. SRM, switched reluctance motor.

Eq. (13) is the pivot of the method: it converts non-linear magnetic and speed information, which is otherwise only implicit in the current error, into a single voltage-demand quantity that can be compared directly with the available converter levels.

For positive current build-up, the controller retains the normal voltage level while $v_{req} \le V_{dc} + \Delta V_s$ and engages the boosted level when the estimated demand exceeds this threshold. The interval $V_{dc} < v_{req} \le V_{dc} + \Delta V_s$ therefore forms a prescribed voltage-margin deadband that suppresses unnecessary transitions between the normal and boosted states. The voltage demand is evaluated directly from the magnetic-map quantities through the feed-forward relation in Eq. (13), without iterative optimisation or online model inversion.

3.1.2. Slope-gain selection

The gain k_s is selected from the desired current-error convergence time rather than treated as an arbitrary tuning constant. For a locally constant I_{ref} and operation below the slew limiter,

$$i^\star = k_s \varepsilon_i. \tag{14}$$

If the selected phase voltage satisfies $v_{ph} \ge v_{req}$, then the attainable current rise is at least the demanded rise and

$$\dot{\varepsilon}_i \le -k_s \varepsilon_i, \left|\varepsilon_i(t)\right| \le \left|\varepsilon_i(0)\right| e^{-k_s t}, \tag{15}$$

so the unsaturated current-error time constant is approximately $\tau_i = 1/k_s$. For the implemented controller, $k_s = 1{,}000\ \mathrm{s}^{-1}$ and $i_{max} = 10\ \mathrm{kA/s}$ are used. At 2,000 r/min, one 15° mechanical stroke lasts

$$t_{15^\circ} = \frac{15^\circ}{360^\circ\left(2{,}000/60\right)} = 1.25\ \mathrm{ms}, \tag{16}$$

whereas $\tau_i = 1\ \mathrm{ms}$. Thus, the nominal capture time is shorter than one rated-speed phase stroke. The additional design condition $k_s \Delta I_o \le \dot{i}_{max}$ prevents the ordinary outer-band error from being permanently driven into the slew clamp. Increasing k_s increases the term $\hat{L}_{inc} k_s \varepsilon_i$ in v_{req}, engaging $V_{dc} + V_{cap}$ earlier and improving current capture at the cost of increased boosted-state occupancy; decreasing k_s has the opposite effect.

3.2. Prioritised four-state selector

With inner and outer current bands $\Delta I_i < \Delta I_o$, voltage margin ΔV_s and latched turn-off flag q_{off}, the implemented selector is

$$v_{ph} = \begin{cases} -V_{cap}, & q_{off} = 1 \text{ or } \varepsilon_i < -\Delta I_o, \\ V_{dc} + V_{cap}, & \varepsilon_i > \Delta I_o \text{ and } v_{req} > V_{dc} + \Delta V_s, \\ V_{dc}, & \varepsilon_i > \Delta I_i, \\ 0, & \text{otherwise.} \end{cases} \tag{17}$$

The ordering in Eq. (17) reflects the operating priorities of the proposed control law. Demagnetisation is assigned the highest priority so that, once the turn-off condition is reached, the outgoing phase is driven through the $-V_{cap}$ state until current extinction. During the active conduction interval, the boosted state $V_{dc} + V_{cap}$ is selected only when the phase-current error exceeds the outer band and the estimated voltage demand satisfies $v_{req} > V_{dc} + \Delta V_s$. This combined current-error and voltage-demand condition distinguishes the proposed selector from a current-error-only switching law. The V_{dc} and zero-voltage states are subsequently used to regulate the phase current within the prescribed current bands. The voltage margin ΔV_s establishes the transition between the normal and boosted excitation states and suppresses repeated switching between these levels when the estimated voltage demand is close to the normal-link threshold.

3.3. Minimum-level selection with voltage-margin deadband and sensitivity to map error

The exact current-error dynamics follow directly from $\varepsilon_i = I_{ref} - i$:

$$\dot{\varepsilon}_i = \dot{I}_{ref} - \frac{v_{ph} - Ri - e_\theta}{L_{inc}}. \tag{18}$$

For a locally constant current reference, $\dot{I}_{ref} \approx 0$, so $\dot{\varepsilon}_i = -\dot{i}$. If the selected phase voltage satisfies $v_{ph} \geq v_{req}$, then the attainable current rise satisfies $i \geq i^* = k_s \varepsilon_i$ and therefore

$$\dot{\varepsilon}_i \leq -k_s \varepsilon_i, \left|\varepsilon_i(t)\right| \leq \left|\varepsilon_i(0)\right| e^{-k_s t}. \tag{19}$$

For $\Delta V_s = 0$, the ordered voltage set, therefore, admits the unique minimum level that satisfies the estimated demand. The implemented law uses $\Delta V_s > 0$ as a deliberate normal-to-boosted deadband. Hence, in the interval $V_{dc} < v_{req} \leq V_{dc} + \Delta V_s$, the controller intentionally retains V_{dc} to prevent chatter rather than claiming exact satisfaction of the ideal demand. Once $v_{req} > V_{dc} + \Delta V_s$ and the outer current-error condition is met, the boosted level is admitted. The implemented policy is thus a minimum-level selection subject to the prescribed voltage-margin deadband.

The estimates are not exact in practice, and the consequences of that must be stated explicitly. Let $\delta L = \hat{L}_{inc} - L_{inc}$ and $\delta e = \hat{e}_\theta - e_\theta$ denote the map errors. From Eq. (13), the demand error is $\delta v = \delta e + \delta L \dot{i}^*$ and is therefore bounded by $\left|\delta e\right| + \left|\delta L\right| \dot{i}_{max}$; it is a bounded perturbation of a *threshold*, not of a commanded voltage or current. Two directions must be distinguished:

- An *overestimate* advances the transition to the boosted state. It cannot cause spurious excitation, because the second branch of Eq. (17) still requires $\varepsilon_i > \Delta I_o$: when the current is already inside the outer band, no amount of demand overestimation can engage the boost. The penalty is confined to a slightly premature use of the higher-stress state.
- An *underestimate* delays the transition. The band controller continues to regulate through the V_{dc} and zero states, so the drive remains stable, but the leading-edge slope reverts to the AHB value until the estimate crosses the threshold. This is the error direction that matters for performance, and it is the one addressed by the design guidance in Section 5.7.

The margin ΔV_s is chosen above the combined ripple contributed by current-sensor noise, map interpolation and the numerical differentiation used to form $\hat{L}_{inc}$ and $\hat{e}_\theta$, so that small variations around V_{dc} do not repeatedly exchange the normal and boosted states. In this sense, ΔV_s plays for the level selection the role that a hysteresis band plays for a two-level chopper: it trades a small, bounded departure from the ideal switching surface for guaranteed freedom from chatter.

3.3.1. Analytical robustness to controller-map uncertainty

The sensitivity of the voltage-demand calculation to magnetic-map uncertainty is examined by perturbing the controller LUT while keeping the physical machine model and operating conditions unchanged:

$$\hat{\lambda}_{\delta}(\theta,i)=(1+\delta)\hat{\lambda}(\theta,i),\ \delta\in\{-0.10,-0.05,0,+0.05,+0.10\}. \tag{20}$$

For a uniform multiplicative perturbation, the corresponding incremental inductance and speed-EMF estimates become

$$\hat{L}_{\mathrm{inc},\delta}=(1+\delta)\hat{L}_{\mathrm{inc}},\ \hat{e}_{\theta,\delta}=(1+\delta)\hat{e}_{\theta}. \tag{21}$$

The resulting change in the estimated phase-voltage demand is therefore

$$\begin{aligned}\Delta v_{\mathrm{req}} &= v_{\mathrm{req},\delta}-v_{\mathrm{req}}\\ &= \delta\left(\hat{e}_{\theta}+\hat{L}_{\mathrm{inc}}i^{\star}\right)\\ &= \delta\left(v_{\mathrm{req}}-Ri\right).\end{aligned} \tag{22}$$

For the largest considered perturbation, $|\delta|=0.10$, the corresponding magnitude of the voltage-demand displacement is

$$\left|\Delta v_{\mathrm{req}}\right|=0.10\left|v_{\mathrm{req}}-Ri\right|. \tag{23}$$

Thus, LUT uncertainty primarily shifts the normal-to-boosted voltage transition. A positive perturbation increases the estimated voltage demand and therefore advances the engagement of $V_{\mathrm{dc}}+V_{\mathrm{cap}}$, whereas a negative perturbation reduces the estimated demand and delays the transition. Since the measured phase current remains in the closed-loop feedback path, the current-regulation bands continue to govern the phase-current response in both cases.

The corresponding current-tracking sensitivity is quantified using the RMS current error,

$$e_{i,\mathrm{RMS}}=\sqrt{\frac{1}{N}\sum_{k=1}^{N}\left(I_{\mathrm{ref},k}-i_k\right)^2}. \tag{24}$$

Eqs. (22) and (23) show that the considered $\pm5\%$ and $\pm10\%$ controller-map perturbations result in a bounded displacement of the voltage-level selection boundary while preserving closed-loop phase-current regulation.

3.4. Per-sample implementation

The complete closed-loop structure, including the outer speed loop, magnetic-map voltage-demand calculation, four-state selector, current reconstruction, rotor-position feedback and auxiliary-link regulator, is shown in Figure 5. The mechanical subsystem is explicitly represented by the electromagnetic torque T_e, externally applied load torque T_L, rotor speed ω and rotor position θ, with

$$J\frac{d\omega}{dt}=T_e-T_L-B\omega, \tag{25}$$

where J is the combined rotor–load inertia and B is the viscous-friction coefficient. The resulting speed and rotor position are fed back to the speed-control and phase-scheduling paths, respectively. The per-sample motor-side decision sequence is detailed separately in Figure 6.

The digital implementation runs from a 50-kHz interrupt on a TMS320F28069 controller; the sequence executed once per sample is read from top to bottom. After a one-time load of the flux-linkage map and the control constants, each interrupt acquires the rotor position θ, mechanical speed ω, auxiliary voltage V_{cap} and the two group currents i_{AC} and i_{BD}; it identifies the active phase $k\in\{A,B,C,D\}$ from the rotor sector and the conduction-enable flag q_k, and assigns the group current to phase k using Eq. (32).

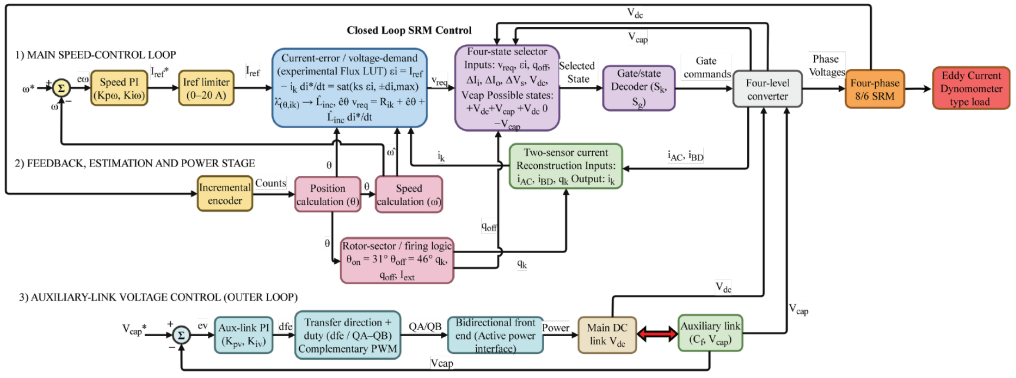


Figure 5. Closed-loop control architecture of the proposed four-level SRM drive, showing the outer speed loop, magnetic-LUT-based voltage-demand calculation, four-state voltage selector, converter, SRM electrical and mechanical dynamics with the applied load torque T_L, rotor-position/speed feedback, two-group current reconstruction and auxiliary-link regulation. LUT, lookup table; PI, proportional–integral; PWM, pulse-width modulation; SRM, switched reluctance motor.

The control signals are stated in engineering units for reproducibility: $e_\omega = \omega^\star - \omega$ is expressed in r/min and the output of the speed proportional–integral (PI) controller is I_{ref} in amperes, limited to 20 A; $e_v = V_{cap}^\star - V_{cap}$ is expressed in volts and the auxiliary PI output is the dimensionless front-end duty command. With $T_s = 20\mu s$, the reported gains give discrete integral increments $K_{i\omega}T_s = 1.6\times10^{-5}$ and $K_{iv}T_s = 2.4\times10^{-4}$ per update. The simulation current-band half-widths are $(\Delta I_i, \Delta I_o) = (1.0, 1.5)\,|\,\mathrm{A}$ and the experimental values are $(0.5, 0.75)|\mathrm{A}$. The current-band values are operating-point-dependent implementation parameters rather than invariant parameters of the proposed selector. The full-voltage simulation employs $(\Delta I_i, \Delta I_o) = (1.0, 1.5)$ A because the available +150-V excitation and −100-V demagnetisation levels produce substantially steeper current slopes. Using the narrower prototype bands under these voltage levels would unnecessarily increase the event-driven motor-side switching activity. In the reduced-voltage prototype, where the available phase-voltage levels are +60 V, +20 V, 0 V, and −40 V, the lower attainable current slopes permit the narrower bands $(\Delta I_i, \Delta I_o) = (0.5, 0.75)$ A to provide tighter current regulation. In both cases, $\Delta I_i < \Delta I_o$ and the same four-state selection law in Eq. (17) is retained.

The turn-off branch is evaluated first. The implemented firing angles are $\theta_{on} = 31^\circ$ and $\theta_{off} = 46^\circ$ mechanical. When $\theta \geq \theta_{off,k}$, or when the turn-off latch q_{off} is already set, q_{off} remains set and the $-V_{cap}$ state is commanded until $i_k < I_{ext}$; the phase is then disabled and the latch is reset. If the phase is still inside its conduction window, the controller reads $\hat{\lambda}(\theta, i)$, $\hat{L}_{inc}$ and $\hat{e}_\theta$ from the map, forms ε_i and $i^\star$, and evaluates v_{req}. The selector then applies the outer-band-plus-voltage-sufficiency test, followed by the inner-band test, to choose boosted, normal or zero-voltage operation. Finally, the chosen state is mapped to the phase-select command S_k and the group-shared command S_g ($S_g = S_{AC}$ for phases A/C and $S_g = S_{BD}$ for phases B/D), after which control returns to the next sampling instant.

The outer speed loop generates the current reference using the implemented digital PI gains $(K_{p\omega}, K_{i\omega}) = (0.025, 0.80)$. Its output is limited to the machine's 20-A peak-current capability. These gains are reported as controller implementation values; their numerical interpretation follows the speed-error and current-command scaling used in the digital signal processor (DSP) code.

The auxiliary-link regulator runs in parallel with the motor-side logic. Its error $e_v = V_{cap}^\star - V_{cap}$ is processed by a PI controller with implemented digital gains $(K_{pv}, K_{iv}) = (0.08, 12)$, which sets the front-end transfer direction and duty ratio d_{fe}. The complementary Q_A/Q_B commands regulate the prototype auxiliary link at 40 V; during the reported tests, the measured voltage remained within approximately ±2 V of this reference. The two loops are decoupled in authority: the motor-side selector does not wait on the front end, and the front end does not override a demagnetisation command.

3.4.1. Control-update and motor-side switching frequencies

The TMS320F28069 operates with a 90-MHz processor clock, while the controller interrupt and bidirectional front-end pulse-width modulation (PWM) operate at 50 kHz, corresponding to a control-update interval of $T_s = 20\,|\,\mu$s s. The motor-side phase switching, in contrast, is hysteresis/event driven and therefore varies with rotor position, phase-current slope, speed EMF, hysteresis-band width and the selected voltage state.

The theoretical number of central processing unit (CPU) clock cycles contained within one 20-μs control-update interval is

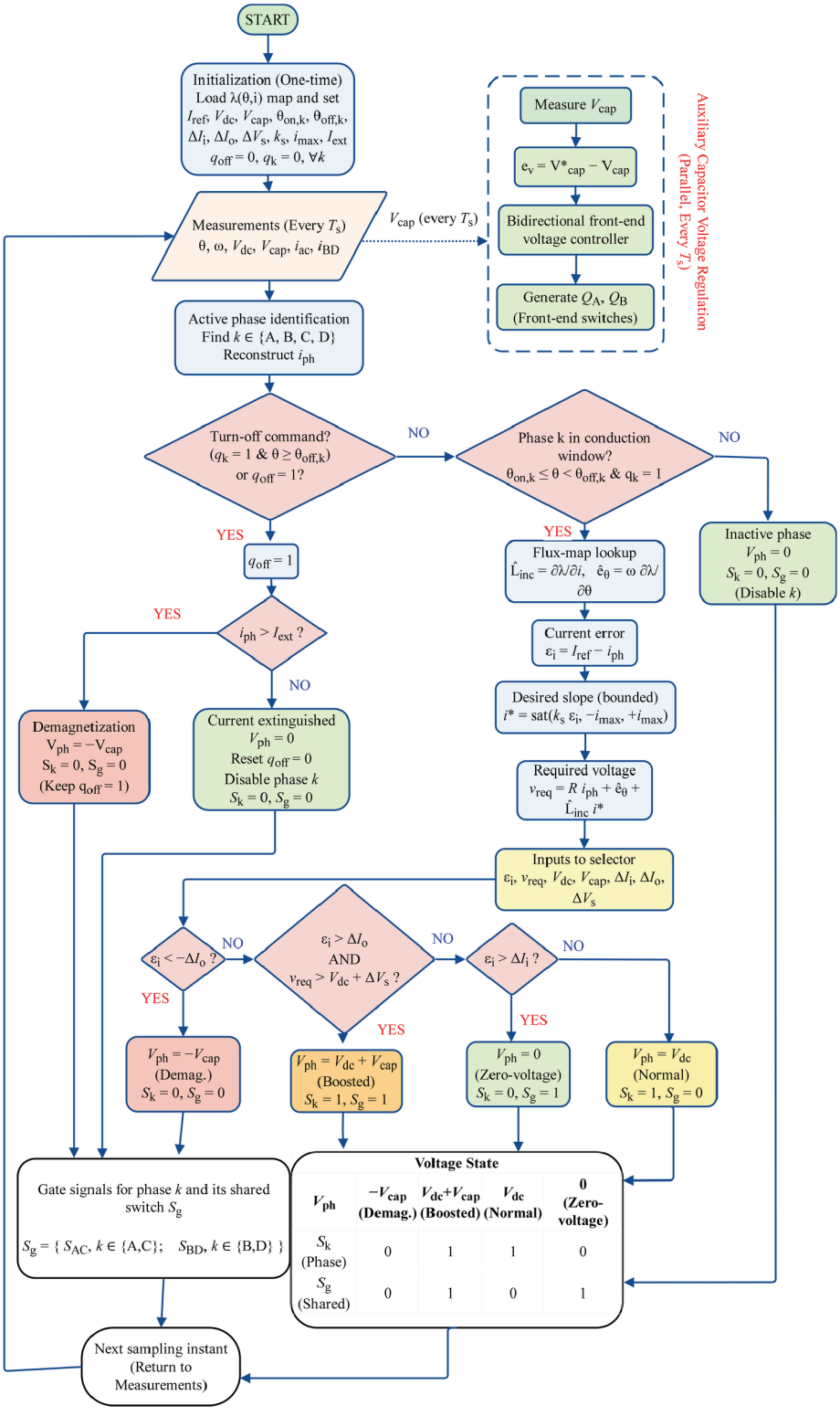


Figure 6. Per-sample execution of the speed-EMF-adaptive selector. The motor-side path (left and centre) performs current reconstruction, the latched turn-off test, the flux-map lookup, the evaluation of v_{req} from Eq. (13) and the prioritised four-state decision of Eq. (17); the dashed block (upper right) is the parallel auxiliary-capacitor voltage regulator that sets the bidirectional front-end duty ratio. The inset table maps each selected voltage state to the phase command S_k and the group-shared command S_g. EMF, electromotive force; SRM, switched reluctance motor.

$$N_{\text{interval}} = f_{\text{CPU}} T_s = \left(90 \times 10^{6}\right)\left(20 \times 10^{-6}\right) = 1{,}800. \tag{26}$$

The value in Eq. (26) represents the total theoretical number of processor clock cycles within one control-update interval and should not be interpreted as the computational budget available exclusively to the proposed voltage-level selector. In practice, a portion of this interval is also required for interrupt servicing, analogue-to-digital converter (ADC) acquisition, rotor position and speed processing, current reconstruction, auxiliary-link regulation and other controller operations. The proposed selector itself is deterministic and non-iterative, comprising bilinear LUT interpolation, local finite-difference evaluations, computation of the scalar v_{req} and a finite set of logical comparisons during each sampling interval.

In summary, q_k is the phase conduction enable, q_{off} the latched demagnetisation command, I_{ext} the extinction threshold, $\theta_{on,k}$ and $\theta_{off,k}$ the firing angles, S_k and S_g the phase- and shared-switch commands, e_v the auxiliary-voltage error and d_{fe} the bidirectional front-end duty ratio.

4. Converter, Current Sensing and Design Method

4.1. Four-level converter and operating states

The converter topology and phase-state table are introduced together with the current-slope derivation so that the analytical states and physical switching states are directly connected. The present section develops the corresponding current paths, device stresses, sensing arrangement and bidirectional front-end design. Figure 7 shows the detailed phase-A current paths for States 1–4 of Table 1.

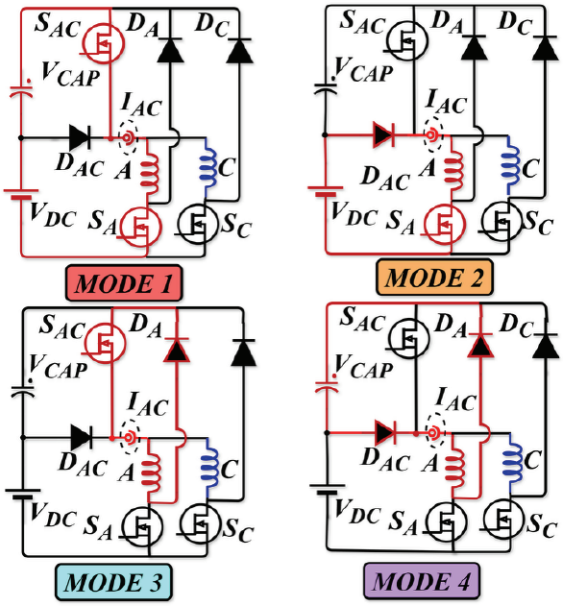


Figure 7. Phase-*A* current paths for the four operating states: (a) boosted magnetisation with S_A and S_{AC} conducting; (b) normal magnetisation with S_A conducting; (c) zero-voltage freewheeling with S_{AC} conducting; and (d) negative-voltage demagnetisation through the diode return path, which returns the trapped winding energy to C_f. These modes correspond to States 1–4 in Table 1.

4.2. Device voltage stress

Because the stage synthesises its levels from the two stacked links, the off-state voltage of every device is bounded by one of the three link potentials $\{0, V_{dc}, V_{dc}+V_{cap}\}$. Evaluating the largest potential difference that appears across each device over the four states of Table 1 gives the peak blocking voltages in Table 2. The phase-select switch and the upper phase diode must withstand the full stacked voltage $V_{dc}+V_{cap}$, whereas each shared switch and shared diode only span the auxiliary segment V_{cap}.

Table 2. Main-converter peak device voltage stress (phase-A branch; other phases identical by symmetry).

Device (per branch)	Function	Peak off-state voltage
Phase switch S_A	Magnetising-loop selection	$V_{dc} + V_{cap}$
Shared switch S_{AC}	Auxiliary-level insertion	V_{cap}
Upper diode D_A	Freewheel / demag. clamp	$V_{dc} + V_{cap}$
Shared diode D_{AC}	Recovery path to V_{cap}	V_{cap}

This asymmetry is a direct and practically useful benefit of the shared-switch arrangement: the two group-shared devices, which are the shared elements introduced by the topology, carry the lower V_{cap} rating. The blocking requirements are therefore stated symbolically so that they scale with any chosen pair $\left(V_{dc}, V_{cap}\right)$ rather than with one worked operating point. Device selection therefore follows the derived blocking-voltage requirements together with the appropriate transient-voltage, current-rating and derating margins.

4.3. Bidirectional front-end energy-transfer modes

The front-end stage is a non-isolated two-quadrant buck–boost cell formed by the complementary switch pair Q_A–Q_B, the antiparallel diodes D_2–D_1 and the inductor L_f. Its leg spans the full stacked link, from the top rail (potential $V_{dc} + V_{cap}$) to ground, while L_f connects the leg midpoint to the inter-link node at potential V_{dc}. The same magnetic component therefore transfers energy in either direction, and the commanded direction is set by the auxiliary-voltage error e_v rather than being tied to motoring or braking: demagnetisation first returns phase energy to C_f, after which excess V_{cap} energy can be delivered to the main link; conversely, the main source replenishes C_f whenever V_{cap} falls below its reference. The front end regulates the net energy imbalance of the auxiliary link. This differs structurally from the conventional C-dump recovery path, although the processed energy and losses depend on the operating point and switching strategy.

Figure 8 resolves the two transfer directions into four subintervals, summarised with the impressed inductor voltage in Table 3. In Mode A, Q_A conducts and the leg midpoint is pulled to the top rail, so L_f sees $v_{L_f} = \left(V_{dc} + V_{cap}\right) - V_{dc} = +V_{cap}$ and is energised from the auxiliary link. In Mode B, Q_A turns off and the current freewheels through the lower diode D_1; the midpoint drops to ground and $v_{L_f} = 0 - V_{dc} = -V_{dc}$, releasing energy into V_{dc}. Modes C and D reverse the process: Q_B energises L_f from V_{dc} ($v_{L_f} = -V_{dc}$) and after Q_B turns off, D_2 commutates the current to the top rail, delivering $v_{L_f} = +V_{cap}$ into C_f.

Because the inductor is always impressed with either $+V_{cap}$ or $-V_{dc}$, continuous-conduction volt–second balance over each direction gives

$$d_{AB} V_{cap} - \left(1 - d_{AB}\right) V_{dc} = 0,\ d_{AB} = \frac{V_{dc}}{V_{dc} + V_{cap}}, \tag{27}$$

$$d_{CD} V_{dc} - \left(1 - d_{CD}\right) V_{cap} = 0,\ d_{CD} = \frac{V_{cap}}{V_{dc} + V_{cap}}, \tag{28}$$

where d_{AB} is the Mode-A duty for auxiliary-to-main transfer and d_{CD} is the Mode-C duty for main-to-auxiliary transfer. At $V_{cap}^{\star} = 2V_{dc}$ these evaluate to $d_{AB} = 1/3$ and $d_{CD} = 2/3$, and their sum is unity, consistent with a single leg regulating the inter-link node; the complementary sum is a convenient commissioning check, since a measured pair that does not sum to unity indicates discontinuous conduction or an incorrect dead-time compensation. The practical PI output is clamped to the admissible duty range and includes dead time between Q_A and Q_B to prevent shoot-through.

The same top-rail-to-ground swing that fixes the inductor voltage also fixes the front-end device stress: with the leg placed across the full stacked link, each of Q_A, Q_B, D_1 and D_2 blocks $V_{dc} + V_{cap}$ in its off state, as listed in Table 4. The front-end devices therefore fall in the same voltage class as the motor-side phase switches, so a single device type covers both stages and simplifies procurement and gate-drive design.

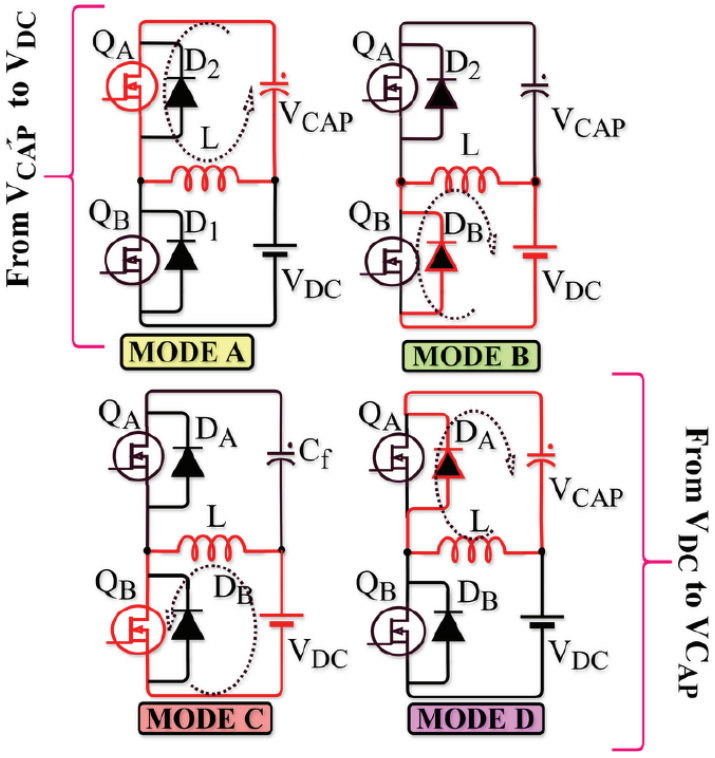


Figure 8. Bidirectional front-end subintervals. Modes A–B transfer energy from V_{cap} to V_{dc} through Q_A and D_1, whereas Modes C–D transfer energy from V_{dc} to V_{cap} through Q_B and D_2. The highlighted path indicates the conducting element in each subinterval; the corresponding inductor voltages are listed in Table 3.

Table 3. Bidirectional front-end switching subintervals and inductor voltage.

Mode	Q_A	Q_B	Conducting element	v_{L_f}	Energy-transfer function
A	ON	OFF	Q_A	$+V_{cap}$	$V_{cap} \rightarrow L_f$: energise
B	OFF	OFF	D_1	$-V_{dc}$	$L_f \rightarrow V_{dc}$: aux-to-main
C	OFF	ON	Q_B	$-V_{dc}$	$V_{dc} \rightarrow L_f$: energise
D	OFF	OFF	D_2	$+V_{cap}$	$L_f \rightarrow V_{cap}$: main-to-aux

Table 4. Front-end peak device voltage stress.

Device	Function	Peak off-state voltage
Switch Q_A	Upper leg (aux $\rightarrow$ main)	$V_{dc} + V_{cap}$
Switch Q_B	Lower leg (main $\rightarrow$ aux)	$V_{dc} + V_{cap}$
Diode D_1	Lower antiparallel (to V_{dc})	$V_{dc} + V_{cap}$
Diode D_2	Upper antiparallel (to V_{cap})	$V_{dc} + V_{cap}$

4.4. Auxiliary-link voltage and capacitance

The auxiliary-voltage reference is fixed by the more demanding of the current-rise and current-extinction requirements. The positive-slope condition is

$$V_{cap}^{\star} \geq \max\left[0,\, v_{req,max} - V_{dc}\right], \tag{29}$$

where $v_{req,max}$ is the maximum required phase voltage over the specified operating region. For an approximately linear decay from turn-off current I_{off} to zero within a target time t_d,

$$V_{cap}^{\star} \geq \max\left[0, \frac{\hat{L}_{inc} I_{off}}{t_d} - Ri - \hat{e}_{\theta}\right]. \tag{30}$$

If the net phase energy that is buffered before the front end processes it is ΔE, the first-order capacitor requirement for an allowed ripple excursion ΔV_{cap} is

$$C_f \geq \frac{\Delta E}{2V_{cap}^{\star}\,\Delta V_{cap}}. \tag{31}$$

Eqs. (29)–(31) cleanly separate the voltage requirement, which is set by the fastest slope that must be produced, from the energy-buffer requirement, which is set by the largest transient imbalance that must be absorbed. The simulation design uses $V_{dc} = 50$ V and $V_{cap}^{\star} = 100$ V; the reduced-voltage prototype preserves the same $V_{cap} / V_{dc} = 2$ ratio with $V_{dc} = 20$ V and $V_{cap}^{\star} = 40$ V. Consequently, the four voltage-level ratios, the corresponding ideal voltage-driven slope increments, and the ideal front-end duty ratios are preserved in per-unit terms; the actual phase-current slopes additionally depend on Ri, e_{θ} and L_{inc} and therefore remain operating-point dependent. The front-end PI regulator compares the measured V_{cap} with $V_{cap}^{\star}$, selects the A–B or C–D sequence according to the sign of e_v, and modulates d_{fe} about the ideal ratios in Eq. (28) to compensate losses and transient energy exchange.

4.5. Two-group current reconstruction

One current sensor measures the A/C group, and another measures the B/D group. With gate/sector indicators $g_k \in \{0,1\}$,

$$\begin{aligned} i_A &= g_A i_{AC}, i_C = g_C i_{AC}, \\ i_B &= g_B i_{BD}, i_D = g_D i_{BD}. \end{aligned} \tag{32}$$

The scheduling constraints $g_A g_C = 0$ and $g_B g_D = 0$ make the assignment unique. If the group-sensor errors are n_{AC} and n_{BD}, the reconstruction errors satisfy

$$\tilde{i}_A = g_A n_{AC}, \tilde{i}_C = g_C n_{AC}, \tilde{i}_B = g_B n_{BD}, \tilde{i}_D = g_D n_{BD}, \tag{33}$$

so that, under correct sector identification and non-overlap, the reconstruction is a unity-gain mapping of the sensor error: it does not amplify it, and no error is transferred between phases. It is important to state the boundary of this result precisely. The constraint is on *same-group* phases only: phases A and B, which are adjacent in the excitation sequence and belong to different groups, may overlap freely and are observed to do so in the measurements of Section 5.5. Overlap of A with C, or of B with D, would render the individual currents unobservable from a single group measurement and would require an additional sensor or an observer. For the four-phase 8/6 machine, same-group phases are two strokes apart, so the constraint is satisfied by a wide angular margin for any practical firing-angle schedule; it is nevertheless an explicit operating constraint rather than an unmodelled assumption, and it is verified experimentally rather than assumed.

4.6. Hardware requirement compared with the asymmetric half-bridge

Because the additional voltage levels are obtained by sharing one switch between two phases rather than by adding a leg per phase, the proposed stage does not trade device count for capability in the way that is usual for multilevel structures. Table 5 compares the two converters for the same four-phase machine, counting directly from Figure 3. The controlled-switch and diode counts are identical to those of a four-phase AHB, the current-sensor count is halved and two passive components (L_f, C_f) are added. In exchange, the drive gains a fourth phase-voltage level, a positive magnetising voltage of $V_{dc} + V_{cap}$ instead of V_{dc}, and a negative demagnetising voltage of $-V_{cap}$ instead of $-V_{dc}$.

The associated design trade-off is the increased blocking-voltage requirement. Six of the eight controlled switches must withstand $V_{dc} + V_{cap}$, while the two group-shared devices require the V_{cap} voltage class. The boosted state also commutates against the full stacked link. These requirements are quantified in Tables 2 and 4 and are included in the converter-loss analysis of Section 5.6. The selective engagement of the boosted level limits unnecessary high-voltage commutations while preserving the additional voltage headroom required for high-speed current regulation.

Table 5. Hardware requirement for the same four-phase 8/6 machine.

Quantity	Four-phase AHB	Proposed four-level stage
Controlled switches	8	8 (($S_A - S_D, S_{AC}, S_{BD}, Q_A, Q_B$)
Diodes	8	8 ($D_A - D_D, D_{AC}, D_{BD}, D_1, D_2$)[‡]
Phase-current sensors	4	2 (one per phase group)
Inductors	—	1 (L_f)
Capacitors	1 (DC link)	2 (DC link and C_f)
Distinct phase-voltage levels	3	4
Positive magnetising voltage	V_{dc}	$V_{dc} + V_{cap}$
Negative demagnetising voltage	$-V_{dc}$	$-V_{cap}$
Peak device blocking voltage	V_{dc}	$V_{dc} + V_{cap}$; V_{cap} for shared devices

[‡] D_1 and D_2 are the antiparallel diodes of Q_B and Q_A and are realised by the MOSFET body diodes in the prototype.
AHB, asymmetric half-bridge; MOSFET, metal–oxide–semiconductor field-effect transistor.

4.7. Positioning against recent literature

Table 6 positions the contribution against recent multilevel SRM converter and control studies. Recent structures reduce device count, add charging capability, provide fault tolerance, or improve voltage balancing and torque control. The distinguishing feature of the present work is the combined use of a four-level shared-switch power stage, two-group current sensing and an online v_{req} calculation that applies the boosted state only when the estimated phase-voltage demand exceeds the normal source capability, together with a full peak-voltage-stress characterisation of both stages. The closest power stage in the literature is that of Chithrabhanu and Vasudevan (2025); the distinction claimed here is therefore not the topology but the decision rule that governs it, and the accompanying stress, sensing and hardware-count analysis.

5. Simulation and Experimental Results

The drive is evaluated in two stages. Simulation, at the full 50-V design point, is used for the quantitative torque-ripple and efficiency benchmarking of Section 5.6, because it permits the machine model, source voltage, current reference, firing angles, speed and load to be held exactly equal across the three converters compared. Measurement, at the reduced 20-V operating point, is used to verify that the converter and the selector behave as designed on real hardware, including a directly measured AHB baseline on the same machine and controller. Table 7 lists both parameter sets. The $2:1$ auxiliary-to-main voltage ratio is common to simulation and experiment, so the synthesised voltage-level ratios and ideal voltage-driven slope increments are preserved in per-unit terms, while the actual current slopes remain operating-point dependent through Ri, e_θ and L_{inc}.

Table 6. Positioning against recent multilevel SRM studies.

Study	Main contribution	Principal emphasis	Distinction relative to the present work
Chaurasiya et al. (2023)	Reduced-switch multilevel grid-fed drive	Faster magnetisation and demagnetisation	Topology-led; no flux-map v_{req} selection
Shah and Payami (2023)	Fully integrated multilevel converter with charging capability	G2V integration	Charging integration rather than voltage-margin minimum-level phase-voltage selection
Chithrabhanu and Vasudevan (2025)	Four-level shared-switch converter with buck–boost recovery	Topology, soft chopping and recovery stage	Closest power stage; online speed-EMF demand criterion is not the stated focus
Ge et al. (2025)	Five-level SRM converter and control analysis	Additional voltage levels	Different power stage; no two-group demand-based selector
Deepak et al. (2025)	Multilevel hysteresis direct-torque control	Torque-ripple reduction	Torque-vector selection rather than phase-voltage-demand estimation
Wang et al. (2025)	Four-level reconfigurable T-type fault-tolerant converter	Fault tolerance and hybrid excitation	Different machine/converter objective
Yousefi-Darani and Narimani (2026)	Three-level shared-leg NPC inverter; eight switches and two sensors	High-voltage operation and neutral-point balancing	Three levels; no boosted/recovery four-state demand selector
Present work	Four-level shared-switch stage, two sensors, v_{req}-based control and device-stress analysis	Voltage-margin minimum-level positive excitation and negative recovery	Combines topology, magnetic-map demand estimation, sensing constraint, peak-stress tables and a measured AHB baseline

AHB, asymmetric half-bridge; EMF, electromotive force; SRM, switched reluctance motor.

Table 7. Simulation and prototype parameters.

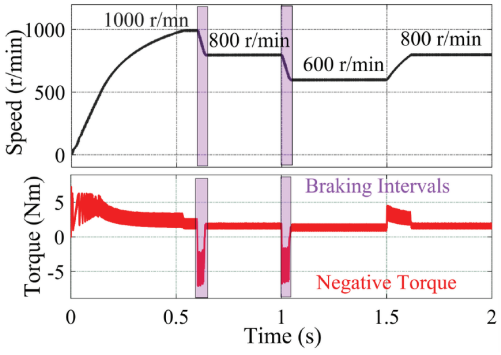
Parameter	Simulation	Experiment
Main source V_{dc}	50 V	20 V
Auxiliary reference V_{cap}^{*}	100 V	40 V
Synthesised phase-voltage levels	$+150, +50, 0, -100$ V	$+60, +20, 0, -40$ V
Current reference I_{ref}	10 A	6 A
Current bands ΔI_i, ΔI_o	1 A, 1.5 A	0.5 A, 0.75 A
Firing angles θ_{on}, θ_{off}	31°, 46° mechanical	
Magnetic LUT	Experimentally identified $\hat{\lambda}(\theta, i)$ map; $0° - 60°$ mechanical, $0 - 20$ A, 61×41 grid	
Speed-loop PI gains $(K_{p\omega}, K_{i\omega})$	$(0.025, 0.80)$	
Auxiliary-voltage PI gains (K_{pv}, K_{iv})	$(0.08, 12)$	
Measured prototype V_{cap} regulation	—	40 ± 2 V
Load condition	3 N·m	Eddy-current brake
Motor	Four-phase 8/6 SRM, 0.9 kW, 2,000 r/min rated speed and 20 A peak current	
Digital controller	TMS320F28069 with a 50-kHz control interrupt	
Front end	$f_s = 50$ kHz, $L_f = 2.3$ mH, $C_f = 4{,}700\mu$ F and bidirectional PI regulation	

LUT, lookup table; PI, proportional–integral; SRM, switched reluctance motor.

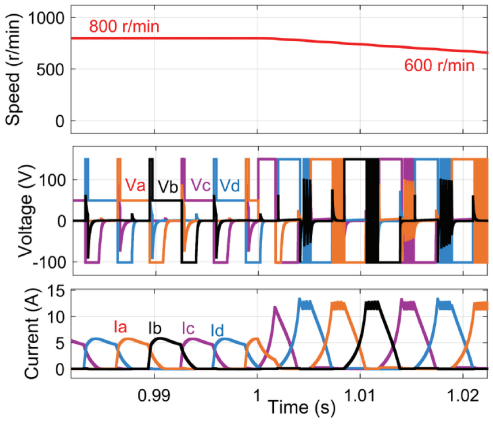
5.1. Simulated dynamic operation of the adaptive selector

Figure 9a presents the rotor-speed and electromagnetic-torque responses during the commanded operating transitions. During the deceleration from 800 to 600 r/min, the drive enters the braking interval, which is identified by the corresponding negative-torque excursion. Figure 9b provides an expanded view of this transition and shows the associated phase-voltage and phase-current waveforms during the change from motoring to braking operation, thereby illustrating the converter-state transition and current response over the braking interval.

The phase voltage switches cleanly among $+150$ V, $+50$ V, 0 and -100 V. Because each level maps to a unique selector state through Table 1, this waveform is a direct state-level check of the implementation: the appearance of a fifth level, or of a level at an unexpected instant, would indicate a decoding error. As designed, the boosted



(a) Rotor-speed and electromagnetic-torque responses.

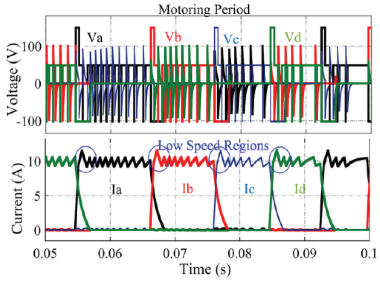


(b) Phase-voltage and phase-current responses.

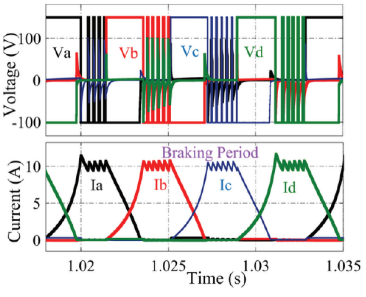
Figure 9. Simulated dynamic response of the proposed SRM drive: (a) rotor-speed and electromagnetic-torque response during commanded transitions; and (b) phase-voltage and phase-current behaviour during the 800-to-600 r/min motoring-to-braking transition. SRM, switched reluctance motor.

state appears only when $v_{req} > V_{dc} + \Delta V_s$, and not whenever the current error alone becomes positive—which is the behaviour that distinguishes the demand-based law of Eq. (17) from a current-error-only law.

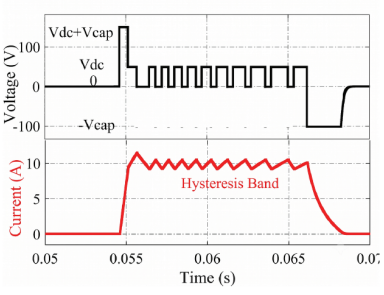
The long-window record in Figure 9b is used as an envelope/state-occupancy view, while Figure 10 provides expanded switching-scale intervals in which individual voltage levels and phase-current trajectories are resolved. All simulation time axes are expressed in seconds.



(a) Low-speed phase response.



(b) Braking operation.



(c) Generated four-level phase voltage.

Figure 10. Simulated operating characteristics of the proposed four-level SRM drive: (a) low-speed phase-voltage and phase-current response with the boosted level suppressed; (b) braking operation using the negative-voltage energy-recovery path; and (c) generated four-level phase voltage and corresponding phase-current response. SRM, switched reluctance motor.

5.2. Low-speed, braking and level-synthesis detail

Figure 10 isolates three intervals of the same run at an expanded time base. At low speed, Figure 10a, the estimated demand stays below the normal-link capability throughout the conduction window, so regulation is dominated by the V_{dc} and zero states, and $-V_{cap}$ appears only at commutation. This is the intended behaviour, and it is the case in which a current-error-only law would waste the boosted level: the current error can be large at a chopping edge even though the calculated demand remains within the V_{dc} capability.

During braking, Figure 10b, the excitation is shifted onto the negative inductance slope, and the demagnetisation path transfers winding energy to the auxiliary link, where it is available either for the next magnetisation or for return to the main source through Modes A–B of Table 3. Figure 10c isolates the generated phase-voltage waveform against the current envelope and confirms clean synthesis of all four commanded levels, including the boosted $V_{dc} + V_{cap}$ pulses at the top of the trace, which are seen to be concentrated in the leading edge of the current pulse and to cease once the current has entered the hysteresis band.

The braking panel is an extinction/recovery demonstration rather than a minimum-ripple sustained regenerative-current test. Once the turn-off latch is asserted, the controller intentionally retains $-V_{cap}$ until $i < I_{ext}$, giving

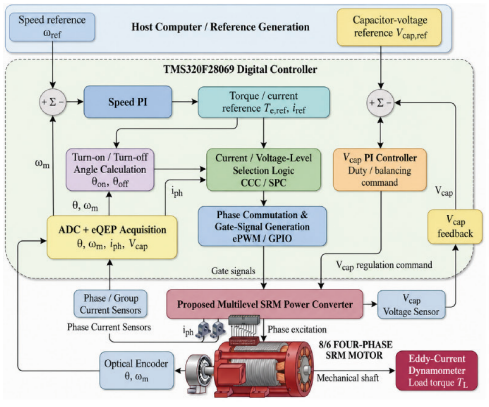
$$\frac{di}{dt} = \frac{-V_{cap} - Ri - e_\theta}{L_{inc}}, \tag{34}$$

which maximises the available negative current slope and minimises tail current beyond the desired conduction region. Alternating 0 and $-V_{cap}$ (soft chopping) could reduce current ripple during sustained regenerative current regulation, but it would lower the average demagnetising voltage and extend extinction time; that alternative braking objective is outside the present study.

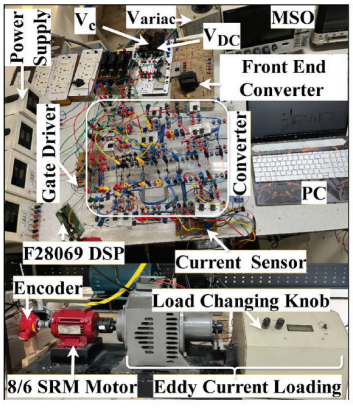
5.3. Prototype and measured dynamic response

The experimental investigation evaluates the converter-state synthesis, phase-current regulation, rotor-speed transitions, regenerative operation, auxiliary-link regulation and the proposed/AHB hardware behaviour. The functional power, control, sensing, and loading arrangement of the experimental platform is shown in Figure 11.

Figure 11 presents the experimental platform used for hardware validation. Panel (a) shows the functional power, control, feedback and loading arrangement, while panel (b) shows the laboratory prototype and associated measurement setup. The bench comprises the 0.9-kW four-phase 8/6 SRM, the TMS320F28069 controller, the proposed four-level converter with its bidirectional front-end stage, an incremental encoder, group-current sensing and an eddy-current brake. During the reported hardware tests, the converter is supplied from a 20-V main DC source, while the auxiliary link is regulated at approximately 40 V. This reduced-voltage operating point is used to demonstrate converter-state synthesis, current regulation and dynamic operation.



(a) Functional arrangement of the experimental test platform.

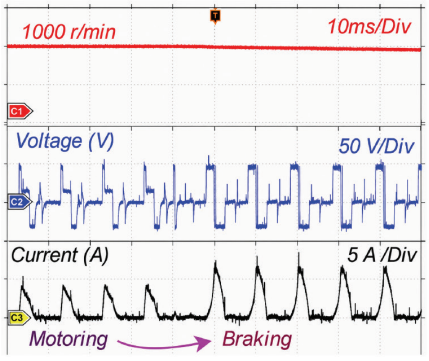


(b) Laboratory prototype and measurement setup.

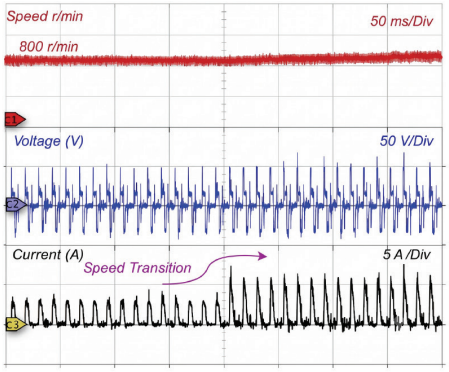
Figure 11. Experimental implementation of the proposed SRM drive: (a) functional arrangement of the converter, controller, sensing, machine and loading system; and (b) laboratory prototype and measurement setup. ADC, analogue-to-digital converter; CCC, current chopping control; DSP, digital signal processor; ePWM, enhanced pulse-width modulator; eQEP, enhanced quadrature encoder pulse; GPIO, general-purpose input/output; MSO, mixed-signal oscilloscope; PC, personal computer; PI, proportional–integral; SPC, single-pulse control; SRM, switched reluctance motor.

Figure 12 presents the measured dynamic response of the proposed drive during both deceleration and acceleration. In Figure 12a, the speed decreases from approximately 1,000 to 800 r/min and the corresponding phase-voltage and phase-current waveforms show the transition from motoring to braking operation. The negative-voltage state is activated during the deceleration interval to support current extinction and regenerative energy transfer.

Figure 12b shows the subsequent acceleration from approximately 800 to 1,000 r/min. During this transition, the phase-current response remains well regulated, and the converter resumes the required positive voltage states to rebuild the phase current as the speed increases. The measured responses therefore demonstrate stable converter operation during both motoring-to-braking and braking-to-motoring transitions. The auxiliary-link voltage remains regulated around 40 V during the reported tests.



(a) Measured deceleration from 1,000 to 800 r/min showing the motoring-to-braking transition and corresponding phase-voltage/current response.

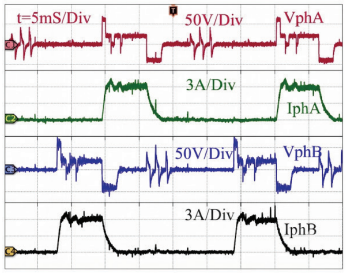


(b) Measured acceleration from 800 to 1,000 r/min showing the braking-to-motoring transition and corresponding dynamic response.

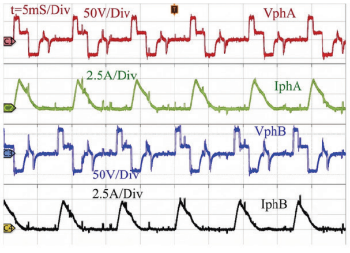
Figure 12. Measured dynamic response of the proposed four-level SRM drive during speed transitions: (a) deceleration from 1,000 to 800 r/min with motoring-to-braking operation; and (b) acceleration from 800 to 1,000 r/min with recovery to motoring operation. SRM, switched reluctance motor.

5.4. Steady-state motoring and regenerative braking

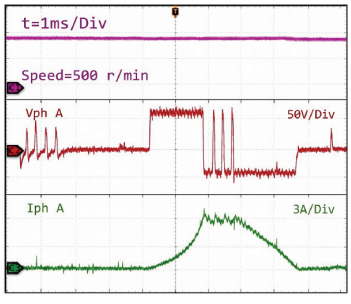
Figure 13 presents the measured steady-state waveforms at three representative operating points, in each case for two phases or for the phase voltage and current of one phase.



(a) Motoring at 500 r/min.



(b) Motoring at 1,200 r/min.



(c) Braking at 900 r/min.

Figure 13. Measured hardware waveforms of the proposed converter-fed SRM drive: (a) low-speed motoring at 500 r/min, showing phase-A and phase-B voltages (50 V/div) and currents (3 A/div) at 5 ms/div; (b) high-speed motoring at 1,200 r/min (50 V/div, 2.5 A/div, 5 ms/div), where regulation is retained; and (c) regenerative braking at 900 r/min (50 V/div, 3 A/div, 1 ms/div), showing current extinction under the $-V_{cap}$ state.

At 500 r/min, Figure 13a shows low-speed chopped current regulation. The dominant displayed phase-voltage states are the normal positive and zero states, followed by the negative state at commutation. This behaviour is consistent with the intended low-speed action of Eq. (17), in which the boosted state is not required when the estimated demand remains within the main-source capability. Phases A and B conduct in the expected sequence.

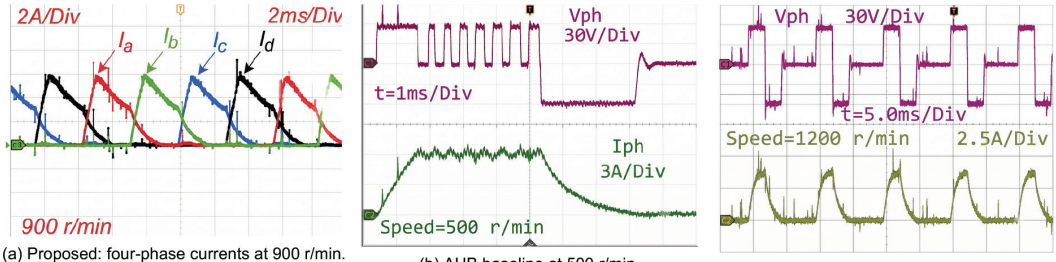
At 1,200 r/min, Figure 13b retains intra-stroke voltage transitions and a bounded current pulse, rather than the single broad pulse observed in the AHB record. This is consistent with the availability of additional voltage headroom as the speed EMF increases. The comparison with the AHB reference at the same speed is discussed in Section 5.5.

The braking record at 900 r/min, Figure 13c, shows controlled excitation followed by current extinction under the negative-voltage state. The displayed decay is steeper than the preceding rise and is consistent with the slope ordering in Eq. (4). The waveform verifies operation of the negative-voltage path; it does not, by itself, quantify the energy returned to the main source.

5.5. Experimental comparison with the AHB baseline

To separate the contribution of the power stage from that of the machine and the control platform, the same prototype was reconfigured to operate as a conventional AHB, driving the identical machine from the identical controller, encoder and firing-angle schedule. Figure 14 presents the resulting comparison.

Figure 14a shows the four reconstructed phase currents of the proposed drive at 900 r/min. Three observations follow. The four strokes are of equal amplitude and equal duration, which confirms that the shared-switch arrangement does not introduce inter-phase asymmetry despite S_{AC} and S_{BD} each serving two phases. Each stroke rises steeply, is regulated near its peak, and is extinguished before the rotor reaches the next commutation point, so no tail current is carried into the falling-inductance region. Finally, although adjacent phases overlap—i_A with i_B, and i_B with i_C—the same-group pairs (i_A, i_C) and (i_B, i_D) do not overlap at any instant. This directly checks the same-group non-overlap condition required by Eq. (32) for the displayed firing schedule, while ordinary adjacent-phase overlap remains permitted.



(a) Proposed: four-phase currents at 900 r/min.

(b) AHB baseline at 500 r/min.

(c) AHB baseline at 1,200 r/min.

Figure 14. Experimental comparison against the AHB baseline on the same machine, controller and firing-angle schedule: (a) the four reconstructed phase currents of the proposed drive at 900 r/min (2 A/div), showing equal strokes and non-overlapping same-group pairs; (b) AHB operation at 500 r/min (30 V/div, 1 ms/div), where chopped current regulation is retained; and (c) AHB operation at 1,200 r/min (30 V/div, 2.5 A/div, 5 ms/div), where chopping is lost, the current no longer settles at its reference, and the decay extends past turn-off. AHB, asymmetric half-bridge.

Figures 14b and c show the AHB baseline at 500 r/min and 1,200 r/min. At 500 r/min, the AHB behaves essentially as the proposed drive does at the same speed: the phase voltage chops, and the current reaches and holds its reference. This agreement is itself an important result, because it confirms the premise of the selector: at low speed the additional level is not needed, and a drive that engaged it there would incur the higher switching energy of the stacked link for no benefit. It also explains why the two converters exhibit almost identical torque ripple below approximately 800 r/min in Figure 15a.

At 1,200 r/min, the AHB waveform exhibits a broad phase-voltage pulse, a rounded current peak and a prolonged current tail after turn-off, reflecting the reduced voltage headroom available for current build-up and demagnetisation. In contrast, the proposed drive at the same speed, shown in Figure 13b, maintains distinct intra-stroke voltage transitions and a well-regulated phase-current pulse. This behaviour demonstrates the improved high-speed current-control capability provided by the additional voltage levels of the proposed converter.

Table 8 summarises the principal experimental observations. Together, the measured records demonstrate multilevel switching, phase-current regulation, dynamic speed transitions, negative-voltage demagnetisation, balanced phase sequencing, same-group non-overlap and the high-speed operating contrast with the AHB reference. The torque-ripple and comparative-efficiency results of Section 5.6 are evaluated separately under the equal-condition simulation framework defined at the beginning of Section 5.

5.6. Torque ripple and comparative efficiency under the adopted loss model

Figure 15a–c presents an equal-condition simulation comparison of the proposed converter, the AHB, and the C-dump topology. The same SRM model and operating conditions are used in all three cases so that the influence of the converter and voltage-selection strategy can be assessed consistently.

The electromagnetic torque ripple is evaluated as

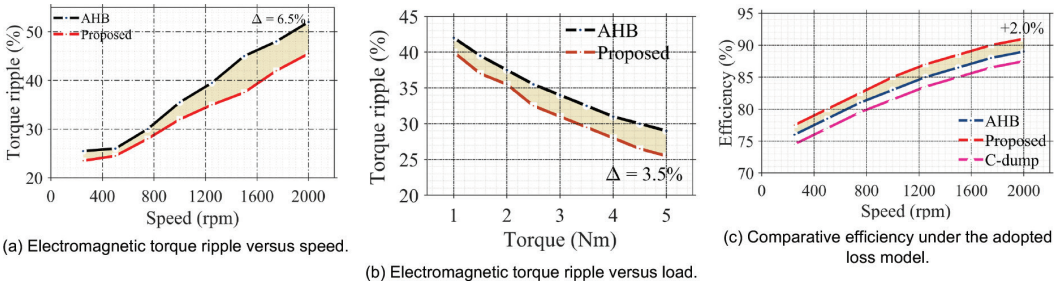
$$T_{ripple}(\%) = 100\frac{T_{e,\max} - T_{e,\min}}{\overline{T}_e}, \tag{35}$$

where $T_{e,\max}$, $T_{e,\min}$ and $\overline{T}_e$ are determined over one electrical cycle after steady-state operation is reached. For all three converter cases, the machine parameters, main-source voltage, phase-current reference, rotor speed, load torque and firing angles are kept identical. The common firing schedule is

Table 8. Measured records and the claims they support.

Record	Figure	Direct observation	Validated aspect
Commanded speed transitions	12b	Speed follows the commanded sequence; multilevel phase-voltage activity and bounded current are retained	Stable closed-loop operation during the displayed transitions
Motoring, 500 r/min	13a	Normal-positive and zero states dominate; $-V_{cap}$ only at commutation	Boosted level correctly withheld when $v_{req} \le V_{dc} + \Delta V_s$
Motoring, 1,200 r/min	13b	Intra-stroke voltage transitions and bounded current retained	Additional voltage headroom remains available at high speed
Braking, 900 r/min	13c	Negative-voltage current extinction; decay steeper than rise	Operation of the negative-voltage path and qualitative slope ordering
Proposed, 900 r/min	14a	Four equal strokes; (i_A, i_C) and (i_B, i_D) never overlap	Phase symmetry under shared switches; non-overlap condition of Eq. (32)
AHB, 500 r/min	14b	Regulation comparable to the proposed drive	No advantage claimed at low speed; premise of the voltage-margin minimum-level rule
AHB, 1,200 r/min	14c	Broad voltage pulse, rounded current peak and extended tail	Qualitative high-speed contrast with the proposed-drive record

AHB, asymmetric half-bridge.



(a) Electromagnetic torque ripple versus speed.

(b) Electromagnetic torque ripple versus load.

(c) Comparative efficiency under the adopted loss model.

Figure 15. Performance comparison of the proposed converter, AHB and C-dump under identical operating conditions: (a) torque ripple versus speed, (b) torque ripple versus load, and (c) comparative efficiency versus speed. AHB, asymmetric half-bridge.

$$\theta_{on} = 31^{\circ}, \theta_{off} = 46^{\circ} \text{ mechanical.} \tag{36}$$

Using the same firing angles and operating conditions for all cases provides a consistent basis for comparing the electromagnetic torque-ripple performance without introducing additional differences due to independent controller or firing-angle optimisation.

Below approximately 300 r/min, both drives exhibit similar ripple, as seen at the left of Figure 15a, because the main source alone can establish the commanded current without boost; this corresponds to the measured agreement between the two converters at 500 r/min in Figure 14b. As speed increases, the AHB current rise is progressively limited by the speed EMF, whereas the proposed selector calls $V_{dc} + V_{cap}$ precisely when the required slope can no longer be obtained from V_{dc}. The improvement therefore grows with speed and reaches 65 percentage points at 2,000 r/min. The load sweep in Figure 15b shows a maximum improvement of 35 percentage points at the highest investigated load, where the larger current excursions again benefit most from the extra voltage headroom. The trend of both curves, and not only their endpoints, is the substantive result: the benefit appears where the theory predicts it and is absent where the theory predicts no benefit.

Figure 15c compares the efficiency characteristics of the proposed converter, the AHB and the C-dump topology under identical operating conditions. The common loss model is expressed as

$$P_{loss,cmp} = P_{Cu} + P_{cond} + P_{sw} + P_{FE}, \tag{37}$$

where P_{Cu} is the phase-winding copper loss, P_{cond} is the semiconductor conduction loss, P_{sw} is the switching loss and P_{FE} represents the front-end device and passive-component losses. The corresponding comparative efficiency is evaluated as

$$\eta_{cmp}(\%) = 100\frac{P_{mech,out}}{P_{mech,out} + P_{loss,cmp}}. \tag{38}$$

The same loss-evaluation framework is applied to all converter cases, providing a consistent basis for comparison over the investigated speed range. As shown in Figure 15c, the proposed converter achieves an improvement of approximately 2.0 percentage points over the AHB at rated speed.

The improvement is associated with the adaptive utilisation of the available voltage levels. The normal V_{dc} level is retained when it provides sufficient current-rise capability, while the boosted $V_{dc} + V_{cap}$ state is introduced as the speed EMF increases and additional voltage headroom is required. This selective use of the boosted state reduces unnecessary high-voltage commutations while maintaining the required phase-current build-up at higher speeds, resulting in the efficiency trend observed in Figure 15c.

5.7. Discussion, validation scope and limitations

The simulation and experimental results together establish the operating characteristics of the proposed drive over the investigated conditions. The comparative analysis evaluates torque-ripple and efficiency trends under identical machine and operating parameters, while the hardware results demonstrate the four-level switching sequence, phase-current regulation, motoring and regenerative operation, dynamic speed transitions, auxiliary-link regulation and the proposed/AHB operating behaviour. These results provide a consistent assessment of the proposed voltage-selection strategy from both performance and hardware-operation perspectives.

Three further limitations bound the applicability of the method and each has a stated remedy.

- *Flux-map dependence.* The demand calculation Eq. (13) relies on an offline map of the specific machine. A systematic underestimate can delay engagement of the boosted level and reduce the high-speed benefit. Temperature dependence and machine-to-machine variation should therefore be addressed through map validation or adaptation before deployment beyond the tested prototype.
- *Sensing constraint.* Two-sensor reconstruction requires the non-overlap constraints of Eq. (32). These are satisfied by a wide margin for the four-phase 8/6 machine, and adjacent-phase overlap remains permitted, as verified in Figure 14a. Applications that require *same-group* phase overlap—for instance, an extended-dwell strategy at very high speed—must add a sensor or an observer or must reassign the phase grouping.
- *Elevated blocking requirement.* Six of the eight switches must block $V_{dc} + V_{cap}$ rather than V_{dc}, as tabulated in Sections 4.2 and 4.3. This is the price of the additional level, and it must be accounted for at the design stage; the two group-shared devices are the exception and require only the V_{cap} rating, while the remaining switch positions are selected for the full stacked-link blocking requirement.

6. Conclusion

A speed-EMF-adaptive minimum-level voltage selector with an explicit voltage-margin deadband has been developed for a four-level shared-switch converter feeding a four-phase 8/6 SRM. The controller converts current error, rotor position, speed and flux-map information into an instantaneous voltage demand, retains V_{dc} within the prescribed normal-to-boosted margin, uses $V_{dc} + V_{cap}$ when the estimated demand exceeds that margin and additional positive headroom is required, and prioritises $-V_{cap}$ after turn-off. The analysis establishes the ordered current-slope set, the front-end transfer intervals, auxiliary-link sizing relations, two-group current assignment, and device-voltage stresses.

Under identical operating conditions, the proposed drive achieves maximum torque-ripple reductions of 6.5 percentage points over the investigated speed range and 3.5 percentage points over the load range, while the corresponding converter-orientated efficiency comparison shows an approximately 2.0-percentage-point advantage over the AHB at 2,000 r/min. The hardware results further demonstrate stable operation during dynamic speed transitions, low- and high-speed motoring, regenerative braking, balanced phase-current sequencing and the same-group non-overlap required by the two-sensor configuration. The measured AHB comparison at 1,200 r/min further illustrates the improved high-speed current-regulation capability provided by the proposed voltage-selection strategy.

Future work will extend the investigated operating range and examine the proposed voltage-selection strategy under broader loading, speed and machine operating conditions.

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