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Experimental Comparison of Single-Tier and Multi-Tier Switched-Capacitor Active Cell-Balancing Topologies

Research paper

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Abstract: This paper presents an experimental comparison of capacitor-based active cell-balancing topologies implemented on a 12S1P lithium-ion battery pack. The study focuses on evaluating the balancing performance of single-tier switched-capacitor (SC), double-tiered switched-capacitor (DTSC), and extended double-tiered switched-capacitor with an additional capacitor (DTSCAC) configurations under identical initial conditions. A modular hardware platform was developed to enable controlled and repeatable experiments. The balancing process was evaluated based on voltage equalisation of individual cells, with completion defined as a maximum voltage difference of 50 mV between the highest and lowest cell. Experimental results show that the DTSC topology generally achieves shorter balancing times compared to the SC configuration, particularly for moderate cell distances. In contrast, the DTSCAC topology does not provide consistent improvement and may result in longer balancing times. In addition to balancing time analysis, current waveforms were measured at multiple nodes within the battery pack to provide insight into charge transfer behaviour. The results highlight the influence of topology and cell position on balancing performance.

Keywords: *active cell-balancing • battery management system • capacitor • lithium-ion battery • switched-capacitor balancing*

1. Introduction

Lithium-ion battery systems are widely used in electric vehicles and energy storage applications due to their high energy density, long cycle life, and favourable performance characteristics. However, when multiple cells are connected in series to form a battery pack, differences in cell parameters such as capacity, internal resistance, and self-discharge rates lead to imbalances in the state of charge (SOC). These imbalances can reduce usable capacity, accelerate degradation, and, in extreme cases, cause safety risks due to overcharging or deep discharge of individual cells (Andrea, 2010; Marcin et al., 2024; Plett, 2015).

To mitigate these issues, cell-balancing techniques are employed as a fundamental function of battery management systems. Conventional passive balancing methods dissipate excess energy in resistive elements, resulting in low efficiency and increased thermal stress. In contrast, active balancing methods enable energy transfer between cells, improving overall efficiency (Qi and Lu, 2014; Wei and Zhu, 2009).

Among active balancing techniques, capacitor-based methods represent a favourable compromise between complexity, cost, and performance. In particular, switched-capacitor (SC) topologies are attractive due to their simple structure and straightforward control implementation. More advanced configurations, such as double-tiered switched-capacitor (DTSC) systems, can further improve balancing speed, as demonstrated in simulation-based studies (Marcin et al., 2023, 2024; Pascual and Krein, 1997; Takeda and Koizumi, 2017).

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Capacitor-based balancing has remained an active area of research, and recent reviews have systematically classified and compared the available equalisation structures (Ashraf et al., 2025; Ghaeminezhad et al., 2021; Li et al., 2025; Qu et al., 2022). Most of the comparative work, however, is based on simulations (Di Rienzo et al., 2023; Marcin et al., 2024; Sotto et al., 2024), while experimental studies typically focus on a single proposed topology validated on small battery strings of four to six cells (Alvarez-Diazcomas et al., 2023; Da Silveira et al., 2023; Izadi et al., 2025). In these studies, the analysis is usually limited to overall balancing performance, whereas detailed measurement of the current distribution within the pack is rarely reported. This is especially important for SC systems, where charge transfer depends on the circuit topology and cell arrangement (Caspar et al., 2018).

In previous work, simulation studies of various capacitor-based balancing topologies were carried out, demonstrating the influence of topology and operating conditions on balancing speed (Marcin et al., 2023, 2024). The present work extends these results experimentally. A controlled experimental comparison of several SC topologies implemented on the same configurable hardware platform and under identical initial conditions has not yet been reported.

This study addresses this gap and presents an experimental comparison of capacitor-based active cell-balancing topologies, including single-tier, double-tiered, and extended configurations. The study focuses on evaluating balancing time under identical initial conditions and presents current waveforms at multiple nodes within the battery pack, particularly in the vicinity of the lowest cell during the balancing process. A controlled experimental methodology is used to ensure repeatability and reliability of results. Furthermore, a quantitative analysis of charge transfer as a function of switching frequency is performed for the single-tier topology. The results provide an experimental comparison of the investigated topologies and highlight the influence of circuit configuration and cell position on balancing performance.

2. Capacitor-Based Active Cell-Balancing Topologies

Capacitor-based active cell-balancing methods utilise capacitors as energy storage elements to transfer charge between cells with different states of charge. Among these methods, switched-capacitor (SC) topologies are widely used due to their simple structure and ease of control implementation.

2.1. Single-tier switched-capacitor topology

In the basic SC configuration (Figure 1), capacitors are connected between adjacent cells and periodically switched using complementary control signals. During one switching phase, the capacitor is connected to a higher-voltage cell and becomes charged. In the subsequent phase, the capacitor is connected to a neighbouring lower-voltage cell, transferring the stored charge. This process repeats periodically, resulting in the gradual equalisation of voltages across the battery pack (Pascual and Krein, 1997).

Since energy transfer occurs only between adjacent cells, the balancing speed depends on the relative position of cells within the series stack. In cases where cells requiring balancing are located far apart, charge must be transferred sequentially through multiple intermediate cells, which can significantly increase the balancing time (Baughman and Ferdowsi, 2008).

2.2. Double-tiered switched-capacitor topology

To overcome the limitation of sequential charge transfer, the DTSC topology (Figure 1) introduces an additional layer of capacitors. This configuration enables more direct energy transfer between cells that are further apart in the battery stack, reducing the number of intermediate steps required. As a result, the DTSC topology can improve balancing speed, particularly in scenarios where significant differences exist between non-adjacent cells. However, this improvement comes at the cost of increased circuit complexity and a higher number of components (Takeda and Koizumi, 2017).

2.3. Extended configurations

Further modifications of the DTSC topology include the addition of extra capacitive paths, such as in the double-tiered switched-capacitor with an additional capacitor (DTSCAC) configuration, where an additional capacitor is introduced to enhance charge transfer between cells located at opposite ends of the battery pack. These configurations aim to further improve balancing performance.

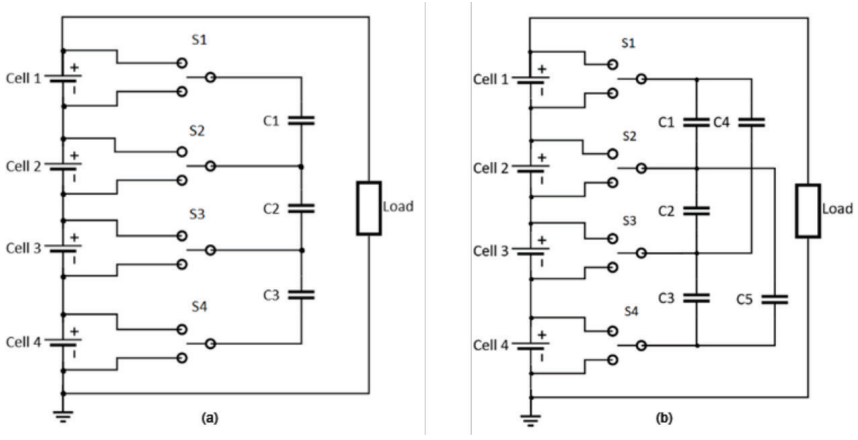

Figure 1. SC balancing (a), DTSC balancing (b). DTSC, double-tiered switched-capacitor; SC, switched-capacitor.

Previous simulation studies have demonstrated that DTSC topologies can achieve faster balancing compared to conventional SC configurations, particularly in cases where significant differences exist between distant cells. However, the increased number of capacitors and associated circuitry leads to higher system complexity and cost (Marcin et al., 2023, 2024).

In this work, all three configurations (SC, DTSC, and DTSCAC) are implemented on the same hardware platform, allowing direct experimental comparison under identical conditions.

3. Simulation Background

This work builds upon previously developed simulation models of capacitor-based active cell-balancing systems. In earlier studies, all three above-mentioned topologies were analysed using MATLAB Simulink. The simulations focused on evaluating balancing performance in terms of SOC evolution and the time required to reduce the difference between cells (Marcin et al., 2024).

For initial SOC values in the range of approximately 94.5%–98%, the SC topology achieved balancing within approximately 1,312 se, while the DTSC topology reduced this time to approximately 1,186 s. These results indicate the potential improvement in balancing speed achieved by multi-tier configurations.

The simulation models were based on ideal switching elements controlled by complementary PWM signals, which simplified the analysis but did not fully capture nonideal effects present in real systems. In addition, the simulations were performed using battery models with different cell chemistry compared to the experimental setup, which may influence the balancing behaviour (Marcin et al., 2024). Therefore, the simulation results serve only as a reference for expected behaviour and cannot be directly compared with the experimental results presented in this work.

4. Balancing Circuit and Hardware Implementation

4.1. Circuit implementation of balancing topologies

The presented analysis is focused on a 12-cell lithium-ion battery pack connected in series (12S1P configuration). The balancing system is based on a configurable capacitor-based circuit that allows implementation of multiple balancing topologies within a single hardware structure. The electrical configuration of the circuit is shown in Figure 2.

The circuit supports several topologies, including:

- SCs,
- DTSCs,
- DTSCAC,
- Modular switched-capacitors (MSCs).

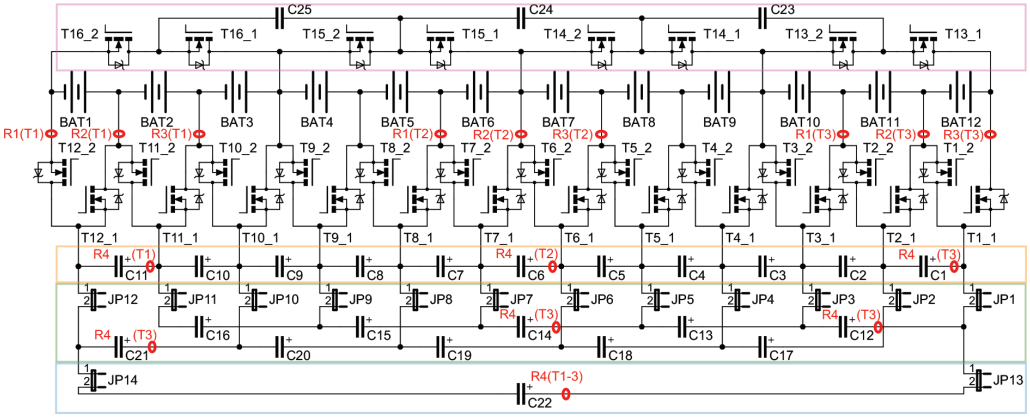

Figure 2. Proposed balancing circuit diagram with different topologies: R1–R4 nodes with current measurement (0.1–0.3 for each test placement), orange – SC, green – DTSC, blue – DTSCAC, pink – MSC. DTSC, double-tiered switched-capacitor; DTSCAC, double-tiered switched-capacitor with an additional capacitor; MSC, modular switched-capacitor; SC, switched-capacitor.

The individual topologies can be selected by an appropriate configuration of the circuit connections (jumpers), enabling direct comparison under identical hardware conditions.

The described circuit structure enables direct comparison of different balancing strategies under identical conditions, as all topologies are implemented within the same system and share the same hardware components. It is also designed to allow access to multiple nodes within the battery pack, enabling measurement of current distribution and charge transfer behaviour during the balancing process. This feature is essential for experimental analysis and comparison of different balancing strategies. Circuit and battery parameters used in this article are presented in Table 1.

4.2. Hardware architecture and control

The circuit described above was implemented in a modular hardware platform designed for experimental investigation of capacitor-based balancing methods. The overall system configuration is shown in Figure 3 and consists mainly of a battery module, a balancer module, and a control unit.

Table 1. Battery pack and balancing circuit parameters.

Parameter group	Parameter	Value	Unit
Battery cell	Cell chemistry	LFP (APR18650M1B)	-
	Nominal voltage	3.3	V
	Rated capacity	1.2	Ah
	Internal resistance (range)	16.8–18.3	mΩ
	Charging voltage	3.6	V
	Charging current	1.5	A
	Charge termination @ 3.6 V	<50	mA
Battery pack	Number of cells	12 (in series)	-
(12S1P)	Nominal voltage	40	V
	Charging voltage (12 in parallel)	3.6	V
	Charging current	6, 15	A
	Charge termination @ 3.6 V	<0.5–0.7	A
	Charging method	CCCV	-
Balancing circuit	Topology	SC/DTSC/DTSCAC	-
	Capacitor capacitance	10,000/10,000/2 × 2,200	μF
	Switching frequency	1	kHz

CCCV, constant-current constant-voltage; DTSC, double-tiered switched-capacitor; DTSCAC, double-tiered switched-capacitor with an additional capacitor; LFP, lithium ion phosphate; SC, switched-capacitor.

The battery module is composed of 12 lithium-ion cells (APR18650M1B) connected in series, forming a 12S1P battery pack. Each cell is accessible through dedicated connection points, which allow both balancing and measurement of electrical quantities at different nodes within the pack. This configuration enables direct observation of voltage and current behaviour during the balancing process. For accurate voltage monitoring of individual cells, a dedicated measurement board based on the Infineon TLE9012DQU was used. This solution ensures reliable acquisition of cell voltages without introducing additional current paths that could influence the balancing process. This hardware schematic corresponds to Figure 2 mentioned above.

The balancer module implements a configurable capacitor-based balancing circuit using MOSFET switches and electrolytic capacitors. The circuit is designed to support multiple topologies, including SC, DTSC, and extended configurations such as DTSCAC. The switching elements are realised using N-channel MOSFET transistors (P140LF4QL), which are controlled through isolated gate driver circuits (UCC21330BDR). The complete balancer consists of 12 gate driver circuits, each controlling a pair of MOSFET transistors. In total, 24 MOSFETs are used in the circuit, enabling bidirectional switching for each cell connection. To ensure proper operation of the high-side and low-side transistors, each driver channel is supplied by an independent isolated 12–12 V DC/DC converter. As a result, a total of 24 DC/DC converters are used to provide galvanically isolated power for all switching elements. This eliminates the need for bootstrap circuits and avoids undesired current paths across the battery pack.

The switching signals are generated by the control unit in the form of complementary PWM signals with a duty cycle of 50% and a defined dead time of 500 ns. The switching frequency can be adjusted, which allows investigation of its influence on charge transfer and balancing behaviour for different topologies.

The hardware platform is designed to enable detailed measurement of electrical quantities during the balancing process. In particular, the circuit allows access to multiple nodes within the battery pack, making it possible to measure currents in selected branches using an external oscilloscope. This feature is essential for the analysis of current distribution, especially in the vicinity of the lowest SOC cell, where charge transfer effects are most pronounced.

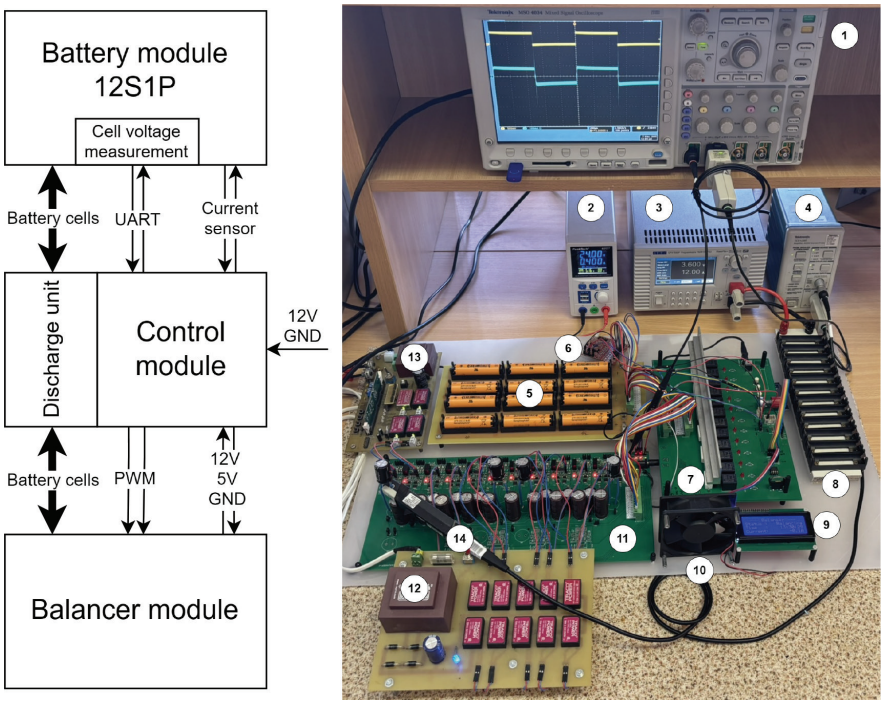

Figure 3. Balancer block diagram (left) and full experimental balancer setup with wiring (right) – 1. Oscilloscope Tektronix MSO4034, 2. Power supply 24 V for the cooling fan, 3. Power supply 3.6 V for charging battery cells, 4. Current probe amplifier Tektronix TCPA300, 5. Battery module, 6. Voltage measuring board Infineon TLE9012DQU, 7. Control module with discharge unit, 8. Charger for battery cells (parallel), 9. Display for control module, 10. Cooling fan for discharge process, 11. Balancer module, 12,13. External DC/DC power supply for transistor gates, 14. Current probe Tektronix TCP312.

4.3. Discharge unit for initial conditions

In addition to the balancing functionality, the system includes a discharge unit used for the preparation of repeatable initial conditions. This unit enables the controlled generation of voltage differences between individual cells prior to the balancing process. Each cell can be discharged through a dedicated branch consisting of a relay and a 1.5 Ω resistor connected in parallel with the cell. This configuration results in a discharge current of approximately 2˚C, enabling rapid and controlled imbalance generation.

The use of controlled discharge times allows precise adjustment of cell voltages, ensuring consistent and comparable initial conditions for all experimental scenarios. This is essential for reliable comparison of balancing performance between different topologies.

5. Charge Transfer Analysis as a Function of Switching Frequency

In order to quantify the charge transfer capability of the balancing system, the current waveform of a selected cell was analysed using data acquired from the oscilloscope. The current signal was exported in a discrete form (.csv), and the transferred charge was calculated over one switching period using a numerical integration approach based on a simplified Coulomb counting method.

The charge was obtained by numerical integration of the measured current waveform. In discrete form, the transferred charge within one switching period can be expressed as

$$Q = \sum_{i=1}^{N} |\, i(t_i) \,| \cdot \Delta t$$

where $i(t_i)$ is the measured current at time instant t_i, Δt is the sampling time step, and N is the total number of samples within one switching period. The absolute value is used because the current alternates direction during the switching process, and both charging and discharging contribute to the total transferred charge.

To enable comparison across different switching frequencies, the charge per period was multiplied by the corresponding switching frequency. The resulting charge transfer rate is given by

$$Q_{\text{rate}} = Q \cdot f$$

where f is the switching frequency and Q_{rate} represents the charge transfer rate expressed in Coulombs per second (C/s).

5.1. Experimental conditions

The analysis was performed using the SC topology under identical operating conditions. The duty cycle of the switching signals was fixed at 50%, and only the switching frequency was varied. The measurements were carried out within a short time interval (approximately 5 min), ensuring that the battery voltages and currents remained nearly constant and the system operated under quasi-steady conditions.

The evaluated current corresponds to the current of a selected cell involved in the charge transfer process, which allows consistent comparison of the charge transfer capability across different switching frequencies.

5.2. Results

The calculated charge transfer rates for different switching frequencies are summarised in Table 2 and shown in Figure 4.

From the presented results, it is observed that the charge transfer rate increases with switching frequency. However, the increase becomes less significant at higher frequencies. Based on these results, a switching frequency of 1 kHz was selected for further analysis, as increasing the frequency beyond this point provides only a marginal improvement in charge transfer while leading to higher switching losses in the system.

Table 2. Charge transfer rate as a function of switching frequency.

Switching frequency (Hz)	Charge transfer rate (C/s)
200	0.004588
300	0.005441
500	0.012585
700	0.013600
1,000	0.014274
2,000	0.015079
3,000	0.015210

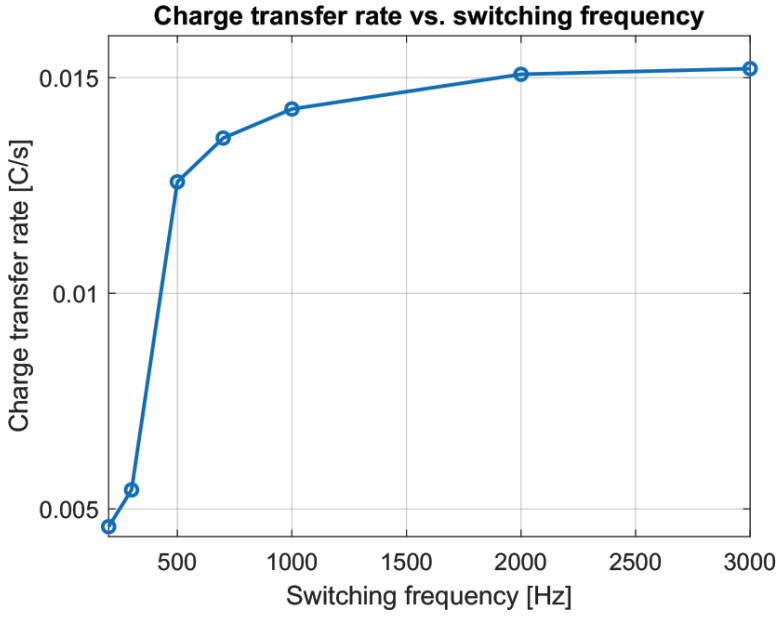

Figure 4. Charge transfer rate as a function of switching frequency.

6. Experimental Methodology and Results

6.1. Experimental setup and test concept

The experimental analysis was carried out on a 12-cell lithium-ion battery pack connected in series (12S1P configuration) using a modular capacitor-based balancing system. The primary objective of the measurements was to compare the balancing performance of three different topologies, namely SC, DTSC, and DTSCAC configurations.

In addition to the comparison of balancing time, the current distribution within the battery pack was analysed during the balancing process. These measurements provide supplementary insight into the charge transfer mechanisms, particularly in the vicinity of the lowest SOC cell.

The experiments were designed in a way that allows direct comparison between different configurations while maintaining identical initial conditions. Only the position of selected cells within the battery pack was changed between individual tests, ensuring that the observed differences are caused solely by the relative distance between the cells. All measurements were conducted under no-load conditions, ensuring steady-state operation of the battery pack.

6.2. Preparation of initial conditions

To ensure repeatability of the measurements, a defined procedure for the preparation of initial cell conditions was applied. All battery cells were first connected in parallel and charged using a constant-current constant-voltage (CCCV) method. The charging process was performed with a current of 6 A for 10 min, followed by 15 A in the

remaining constant-current phase. The charging process was terminated during the constant-voltage phase when the current dropped to 0.5–0.7 A. At the end of the charging process, all cells reached a voltage of approximately 3.6 V. After charging, the cells were left to rest for 10 min.

Subsequently, the cells were reconfigured into a series connection and a controlled imbalance was introduced using a discharge unit. The cells were discharged through resistive loads corresponding to a current of approximately 1.5 A, with defined time intervals. During the first 180 s, all cells were discharged simultaneously, which corresponds to passive balancing behaviour, as all series-connected cells were connected to a resistor in parallel. During this stage, 1.8 A was drawn from the entire battery pack.

After 180 s, the highest cell was disconnected from the discharge process. The same procedure was then applied to the remaining cells, where 1.8 A was discharged for an additional 720 s. After this period, all cells except the lowest one were disconnected. The remaining time of 1,200 s corresponds to the discharge of only the lowest cell with a current of 1.5 A.

The highest cell was, therefore, discharged for 180 s, most of the cells for 900 s, and the lowest cell for 2,100 s. This approach provides a simple and repeatable method for generating a controlled imbalance between cells.

After the discharge process, the resulting cell voltages were approximately 3.33 V for the highest cell, 3.29 V for the remaining cells, and 3.16 V for the lowest cell. The battery pack was then left in a resting state for an additional 10 min before the balancing process was initiated. After the 10-min resting period, the voltage of the lowest cell increased to approximately 3.21 V.

6.3. Test scenarios and balancing time results

After preparation of the initial conditions, the battery pack was connected to the balancer and the balancing process was initiated. The measurements were carried out over a period of approximately 4 h, during which the node current waveforms were recorded using an oscilloscope. At the same time, the cell voltages were measured at 1-s intervals by the control unit and stored on an SD card.

Three experimental configurations were defined to analyse the influence of cell position on the balancing process. In all cases, the same physical cells were used as the highest and lowest cells, while only their position within the battery pack was changed. The highest cell was always cell 1, and the lowest cell was always cell 2, which was relocated within the battery pack for each test scenario.

Each test configuration required approximately 6 h to complete, including the initialisation procedure, and was carried out three times under identical conditions. The reported balancing times represent the arithmetic mean of the three repetitions. The definition of individual test scenarios, corresponding measurement points, and measured average balancing times for all investigated topologies are summarised in Table 3.

Table 3. Definition of test scenarios with corresponding measurement points, topology, and balancing time needed to reach a 50 mV difference between the highest and the lowest cell.

Topology	Test	Code	Highest cell	Lowest cell	R1 (node)	R2 (node)	R3 (node)	R4 (capacitor)	Average balancing time to 50 mV difference [s]
SC	T1.1	1H2L	Cell 1	Cell 2	Node 2	Node 3	Node 4	C11	4,697
SC	T2.1	1H6L	Cell 1	Cell 6	Node 6	Node 7	Node 8	C6	8,969
SC	T3.1	1H12L	Cell 1	Cell 12	Node 11	Node 12	Node 13	C1	8,730
DTSC	T1.2	1H2L	Cell 1	Cell 2	Node 2	Node 3	Node 4	C21	5,216
DTSC	T2.2	1H6L	Cell 1	Cell 6	Node 6	Node 7	Node 8	C14	6,845
DTSC	T3.2	1H12L	Cell 1	Cell 12	Node 11	Node 12	Node 13	C12	8,540
DTSCAC	T1.3	1H2L	Cell 1	Cell 2	Node 2	Node 3	Node 4	C22	5,659
DTSCAC	T2.3	1H6L	Cell 1	Cell 6	Node 6	Node 7	Node 8	C22	9,300
DTSCAC	T3.3	1H12L	Cell 1	Cell 12	Node 11	Node 12	Node 13	C22	8,868

DTSC, double-tiered switched-capacitor; DTSCAC, double-tiered switched-capacitor with an additional capacitor; SC, switched-capacitor.

The balancing process was considered complete when the voltage difference between the highest and the lowest cell dropped below 50 mV. The voltage equalisation for all investigated topologies and test scenarios is shown in Figures 5–7.

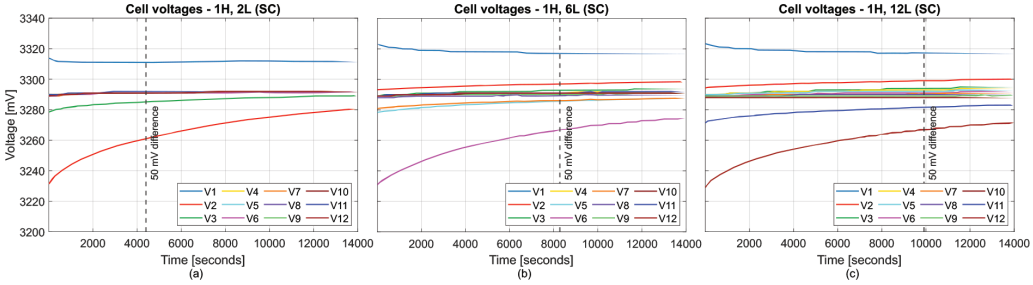

Figure 5. Voltage equalisation of 12S1P battery pack during balancing with SC topology: (a) Test T1.1, (b) Test T2.1, (c) Test T3.1. SC, switched-capacitor.

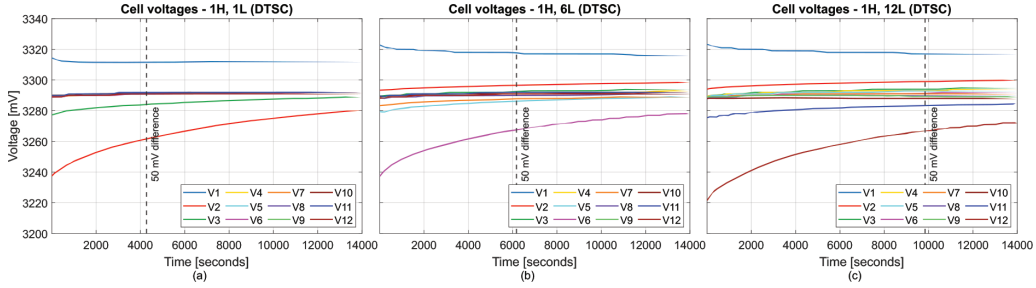

Figure 6. Voltage equalisation of 12S1P battery pack during balancing with DTSC topology: (a) Test T1.2, (b) Test T2.2, (c) Test T3.2. DTSC, double-tiered switched-capacitor.

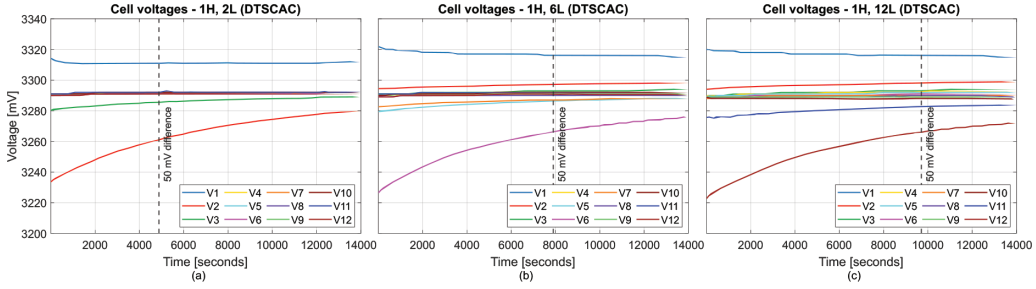

Figure 7. Voltage equalisation of 12S1P battery pack during balancing with DTSCAC topology: (a) Test T1.3, (b) Test T2.3, (c) Test T3.3. DTSCAC, double-tiered switched-capacitor with an additional capacitor.

The notations T1.*x*, T2.*x*, and T3.*x* define the cell configurations, while the index *x* denotes the balancing topologies (SC, DTSC, DTSCAC). The results summarised in Table 3 show that the DTSC topology generally achieves shorter balancing times compared to the SC topology under identical initial conditions. The most significant improvement is observed in Test T2, where the distance between the cells is moderate. In contrast, the DTSCAC topology does not consistently improve balancing performance and, in some cases, results in longer balancing times compared to DTSC. In general, the balancing time increases with the distance between the highest and lowest cells, although for the SC and DTSCAC topologies, the times at moderate and large distances are comparable.

6.4. Node current waveforms

The current measurements were focused on analysing the charge transfer behaviour in the vicinity of the lowest cell. For this purpose, several measurement points were defined within the battery pack corresponding to selected electrical nodes shown in Figure 2.

The battery pack wiring can be interpreted as a sequence of nodes, where each node represents the connection point between two adjacent cells. The negative terminal of the battery pack corresponds to the first node, and each subsequent node represents the cumulative voltage of the cells up to that point.

Currents were measured in selected conductors around the lowest cell, named as R1, R2, and R3, representing adjacent nodes in the battery structure. In addition, the capacitor current (R4) was measured, representing the

primary charge transfer path in the balancing circuit. To distinguish between individual test configurations, the measurement points are indexed using an additional identifier, where, for example, R1.1, R2.1, and R3.1 correspond to tests T1, T2, and T3. The exact measurement positions were selected according to the location of the lowest cell in each test configuration. The measured current waveforms for individual test configurations and balancing topologies are shown in Figures 8–10.

In the presented waveforms, a positive current direction corresponds to charging of the battery cell or capacitor, while a negative current direction indicates discharge. The observed current waveforms follow the periodic switching behaviour of the balancer and reflect differences in topology and cell position.

All current measurements were performed using a high-bandwidth measurement setup consisting of a Tektronix TCPA300 current probe amplifier and a compatible current probe TCP312. The probe was connected to a digital oscilloscope MSO4034.

In capacitor-based switching circuits, the current at each transition is determined by the voltage difference between the connected elements and the total loop resistance, which, in this case, comprises the on-state resistance of the MOSFET switches, the equivalent series resistance (ESR) of the balancing capacitors, the internal resistance of the battery cells, and the conductor resistance. Since the intercell voltage differences are small, typically of the order of tens of millivolts, the resulting transient currents remain low throughout the balancing process.

The waveforms in Figures 8–10 also show brief current spikes at the switching transitions, arising from the switching of the MOSFET transistors in combination with the parasitic inductance of the measurement wiring, which includes extended leads and jumper connections used to access multiple nodes across the experimental

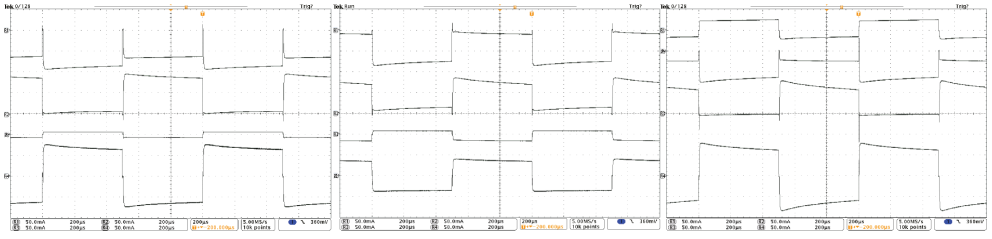

Figure 8. Node current waveforms for SC topology: (left) Test T1, (middle) Test T2, (right) Test T3 – nodes described in Table 3. SC, switched-capacitor.

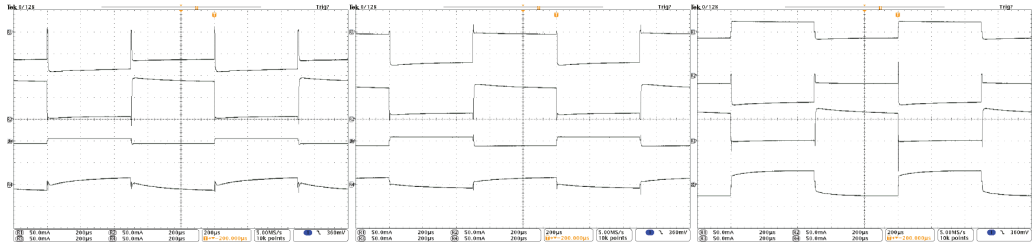

Figure 9. Node current waveforms for DTSC topology: (left) Test T1, (middle) Test T2, (right) Test T3 – nodes described in Table 3. DTSC, double-tiered switched-capacitor.

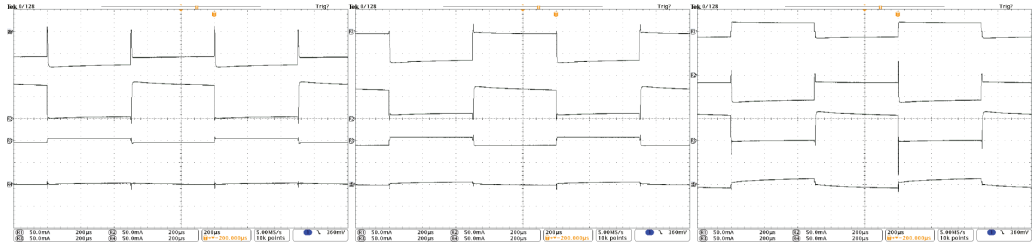

Figure 10. Node current waveforms for DTSCAC topology: (left) Test T1, (middle) Test T2, (right) Test T3 – nodes described in Table 3. DTSCAC, double-tiered switched-capacitor with an additional capacitor.

setup. These spikes represent switching noise and are not related to the balancing current itself. The node current measurements were used to identify the direction of charge flow and the average current magnitude at each node, providing insight into how charge is distributed through the pack during balancing.

6.5. Discussion of results

The results presented in the previous subsections demonstrate that both the selected topology and the relative position of the highest and lowest cells have a significant influence on the balancing process. In general, the balancing time increases with the distance between the cells, with the shortest times achieved for adjacent cells. This trend is most pronounced for the DTSC topology, while for the SC and DTSCAC topologies, the balancing times at moderate and large distances are comparable. This result is consistent with the sequential nature of charge transfer in capacitor-based balancing systems, where energy is transferred step-by-step through intermediate cells.

The performance of the three topologies varies considerably depending on the distance between the unbalanced cells. For adjacent cells (Test T1), the SC topology achieves the shortest balancing time of 4,697 s, while DTSC and DTSCAC require 5,216 s and 5,659 s, respectively. This indicates that when the imbalance is localised between neighbouring cells, the direct adjacent-cell transfer of the SC topology is the most effective, and the additional capacitive paths of the multi-tier configurations provide no advantage. As the distance increases to a moderate level (T2), the DTSC topology becomes clearly superior, achieving 6,845 s compared to 8,969 s for SC, a reduction of approximately 24%. This is the most significant performance difference observed in the study and confirms that the second tier accelerates charge redistribution when the transfer would otherwise require several intermediate steps. For the most distant configuration (Test T3), DTSC again achieves the shortest time at 8,540 s, with SC and DTSCAC close behind at 8,730 s and 8,868 s. For the SC and DTSCAC topologies, the balancing time at the moderate distance (Test T2) is marginally longer than at the large distance (Test T3). This difference is only a few per cent and lies within the measurement variability of the repeated tests, so it is not regarded as significant.

The DTSCAC configuration does not outperform either SC or DTSC in any of the tested scenarios. In this topology, capacitor C22 alternately connects across the first 11 cells (cells 1–11) and the last 11 cells (cells 2–12). Because these two spans differ only in cells 1 and 12, the voltage difference that drives the charge transfer through C22 corresponds to the difference between these two outermost cells alone, which remains very small throughout the balancing process. The charge transferred by C22 in each cycle is, therefore, minimal, and the additional capacitor contributes little to the equalisation in any configuration. Since the results show no measurable benefit from this extension, the DTSCAC topology does not appear to be a promising direction for further development.

The analysis of node current waveforms supports these observations. The measured waveforms show that the distribution of current within the battery pack changes depending on both the topology and the position of the cells. In the SC configuration, the current flow is concentrated locally between neighbouring cells, while in the DTSC configuration, the current is distributed across a larger portion of the battery pack. This behaviour reflects the availability of additional charge transfer paths in multi-tier configurations.

Overall, the results demonstrate that the choice of topology has a significant impact on balancing performance and that the DTSC configuration provides a good compromise between complexity and efficiency. At the same time, the results highlight that further extension of the topology does not necessarily lead to improved performance and must be evaluated carefully for a given application.

6.6. Limitations, additional considerations, and future work

The experimental platform was designed primarily to compare balancing time and characterise charge-transfer behaviour, rather than quantify conversion efficiency or power losses directly. As an indirect check, the sum of the cell voltages was monitored during an extended 14-h balancing run and remained essentially constant, changing from approximately 39.45–39.53 V. This confirms that the balancer redistributes charge rather than draining the pack. The small increase is attributed to cell relaxation and the open circuit voltage (OCV) characteristic of lithium ion phosphate (LFP) chemistry. A direct evaluation of these quantities is not straightforward with the present hardware, as it would require the simultaneous measurement of the small balancing currents at all cell nodes throughout the process.

Voltage measurements relied on the Infineon TLE9012DQU battery-monitoring IC, while node currents were captured using a Tektronix TCPA300/TCP312 probe and MSO4034 oscilloscope. The accuracy of both measurements follows from the specifications of these instruments.

Switching activity of the balancing circuit was found to influence the pack output voltage. Measurements with the oscilloscope showed transient oscillations of approximately ±4 V and 530 ns duration at each switching event, occurring at a rate of approximately 2 kHz for the 1 kHz switching frequency. The amplitude of these oscillations is a consequence of the parasitic inductance of the prototype wiring and would be substantially reduced in a compact PCB design. A preliminary test with a 31 Ω resistive load confirmed that the balancing system operates correctly while the pack supplies an external current of approximately 1 A. A full characterisation under dynamic load conditions representative of electric vehicle applications is planned for future work.

7. Conclusion

This paper presented an experimental comparison of capacitor-based active cell-balancing topologies implemented on a 12S1P lithium-ion battery pack. The study focused on evaluating the balancing performance of single-tier SC, DTSC, and extended DTSCAC configurations under identical initial conditions.

The results show that the DTSC topology generally achieves shorter balancing times compared to the SC topology, particularly in cases where the distance between the highest and the lowest cells is moderate. In contrast, the DTSCAC configuration does not provide consistent improvement and, in some cases, results in longer balancing times than the DTSC. This indicates that increasing the number of capacitive paths does not necessarily lead to improved balancing performance.

In general, the balancing time increases with the distance between the cells, confirming the influence of cell position on the balancing process. The analysis of current waveforms further supports these observations, showing differences in current distribution depending on both topology and cell arrangement.

The results demonstrate that the choice of balancing topology has a significant impact on performance and that the DTSC configuration provides a favourable compromise between complexity and effectiveness. The results also demonstrate that increasing circuit complexity does not necessarily lead to improved balancing performance. At the same time, the study highlights the importance of careful topology design, as additional circuit elements do not always result in improved behaviour.

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