

Diode Rectifier with Improved Quality Indicators for Electrical Energy

Research paper

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Received: 08 February, 2026; Received in the revised form: 30 April, 2026; Accepted: 26 May, 2026

Abstract: In this work, we present a three-phase diode bridge rectifier with a power line current close to a sinusoidal shape. To benefit from this approach, a solution called 'current modulation' is used in the DC link of the rectifier. The main advantage of this system is that the power supplied to the current modulation stage is only a small percentage of the entire power system, meaning that this solution is especially attractive in the case of high-output power systems, for example, for supplying electrical traction. The essential aspect of the current modulation stage is a wide-pass band power electronics controlled current source (VCCS), which is based on a dual-channel (interleaved) topology. The control algorithm for the current modulation stage also takes into consideration the impact of aliasing phenomena on the stability of the system, and uses a control method proposed by the authors. This work contains a general description of the operation of this rectifier and presents basics of operation for the current modulation stage. Selected results from both a simulation of the rectifier and an experimental model are included.

Keywords: diode rectifier • electrical traction • multi-channel inverter • rectifier • quality of electricity

1. Introduction

The power rectifier is one of the most widely used types of power electronic converters. Unfortunately, distortion of currents and voltages in widely used power lines can arise from the operation of standard diode- and thyristor-based rectifiers, leading to serious problems in electrical energy systems. Hence, improving the quality of the input (power-line) current of a rectifier system is essential (IEEE Std 1159, 2009; Masetti, 2010). One existing solution is the use of rectifiers equipped with active or passive filters (Adrikowski et al., 2017; Beres et al., 2016; Gwóźdź, 2013; Herman et al., 2024; Rashid, 2018a; Siwczyński and Jaraczewski, 2012). This approach relies on a switch-mode rectifier built with a transistor inverter operating at a switching frequency much higher than the grid voltage frequency (Ebadpour, 2024; Rashid, 2018a). Other proposed solutions employ PFC converters with multilevel topologies (Wu et al., 2015). To correct the waveform of the grid current, a rectifier can also be constructed using thyristors or diodes interconnected through coupled inductors (Iwaszkiewicz et al., 2019; Mysiak and Strzelecki, 2011). Another option is a system incorporating a voltage modulator in the DC link, built with semi-controlled devices such as thyristors and a dedicated multi-tap inductor (Rashid, 2018a). However, all of these devices are relatively expensive. Therefore, this paper presents an alternative power-conversion scheme capable of shaping the power-line current towards a sinusoidal waveform. The proposed approach is based on current modulation in the rectifier's DC link. The operating principles of this system have been described in detail in Choi et al. (1996); Krystkowiak and Gwóźdź (2011); Supronowicz and Strzelecki (1998); only a concise summary is provided here for completeness.

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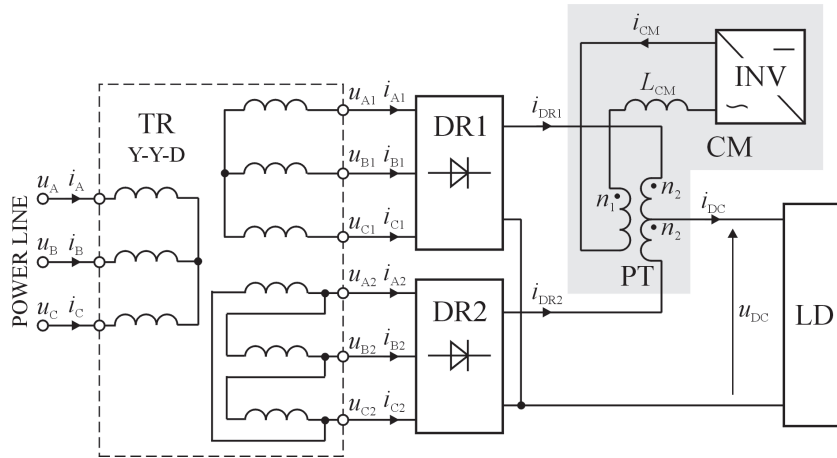


Figure 1. Block diagram showing the proposed three-phase diode rectifier system with current modulator block in the DC link.

The entire system (see Figure 1) is built with two coupled six-pulse diode bridge rectifiers (DR1 and DR2), which are supplied by a three-phase, three-winding power transformer with a ‘star-star-delta’ connection (shown as the TR block in Figure 1). In this way, a phase shift of 30 electrical degrees in the transformer’s output voltage is obtained. The DC link of the system includes a dedicated power electronics converter, called the ‘current modulator’, (shown as CM in Figure 1), which is responsible for the appropriate shaping of the rectifiers’ supply currents. The current modulation stage operates as a wide-band power electronics controlled current source, and is connected to the DC link of the rectifiers via a pulse (i.e. wide-pass band) transformer (the PT block), with two taps on the primary side. The solution presented here makes it possible to visibly improve the quality of the rectifier input currents, i.e. i_A , i_B , and i_C , by bringing their waveforms close to a sinusoidal shape.

To determine the desired shape of the current at the CM block, i_{CM} , some assumptions were made, as follows: the shape of the power source’s EMF is sinusoidal, the power source is symmetrical, and the power delivered to the load, P_{DC} , is the power, P_L , associated with the basic harmonic of the currents drawn from the power source. Based on these assumptions, the following equation was formulated:

$$3U_A I_A = U_{DC} I_{DC}, \quad (1)$$

where U_A , I_A are the RMS values of the phase voltage and current of the power supply source, and U_{DC} , I_{DC} are the average values of the voltage and current in the DC link of the rectifier.

When the voltage drops at the diodes and the power losses in the DC link, caused by its parasitic elements, were neglected, the voltage’s value at the output of the rectifiers is as follows:

$$U_{DC} = \frac{3\sqrt{6}}{\pi} U_A. \quad (2)$$

From Eqs (1) and (2), and assuming that the current modulation stage is turned on, the value of the power source current can be calculated using the following formula:

$$I_A = \frac{\sqrt{6}}{\pi} \sqrt{2} I_{DC} \sin(\omega_L t) = \frac{2\sqrt{3}}{\pi} I_{DC} \sin(\omega_L t), \quad (3)$$

where ω_L is the frequency of the fundamental voltage harmonic in the power grid.

It is also assumed here that:

- The magnetic circuit of the pulse transformer is unsaturated, $i_{DR1} - i_{DR2} = n_{PT} i_{CM}$, where n_{PT} is the turns ratio for the pulse transformer windings; and
- The rectifiers’ output currents are equal to each other, $I_{D1} = I_{D2}$, and their sum is I_{DC} .

From Eq. (3) and the fact that the supply current, in a given source phase, is the sum of the phase currents of the 'star', 'delta' windings, we obtain:

$$\frac{2\sqrt{3}}{\pi} I_{DC} \sin(\omega_L t) = i_{A1} \left(1 + 2n_{PT} \frac{i_{CM}}{I_{DC}} \right) + i_{A2} \left(1 - 2n_{PT} \frac{i_{CM}}{I_{DC}} \right), \quad (4)$$

Solving Eq. (4) with respect to i_{CM} gives the final formula defining the desired shape of the current at the modulator output. For a given phase of the line powering the system, this formula has the following form:

$$i_{CM} = \frac{I_{DC}}{2n_{PT}} \frac{\frac{2\sqrt{3}}{\pi} I_{DC} \sin(\omega_L t) - (i_{A1} + \sqrt{3}i_{A2})}{i_{A1} - \sqrt{3}i_{A2}}, \quad (5)$$

In this way, the waveforms of the supply currents of both rectifiers can be modified, and as a consequence, the resultant waveforms of the transformer supply currents, i_A , i_B , and i_C , are also modified towards a sinusoidal shape. The analysis in Choi et al. (1996), Supronowicz and Strzelecki (1998) indicates that the estimated power of the current modulation stage is only about 2.35% of the total power at the output of the DC link, representing a significant advantage of the solution presented here. However, for a three-phase power device, the waveform given in Eq. (5) needs to be replaced by a waveform with the same phase shift, with respect to the voltage in a given phase; otherwise, the current in the two phases of the power line shall be distorted from the desired sinusoidal waveform. This fact, which is essential for the proper operation of the proposed system, was omitted from previous works (Choi et al., 1996; Supronowicz and Strzelecki, 1998) and is clearly emphasised here. As a consequence, the fundamental frequency of the current at the modulator output should be six times the power line frequency, which here is 300 Hz. A current at the modulator output with a triangular shape was therefore used (Choi et al., 1996; Supronowicz and Strzelecki, 1998), as this is close to the current defined in Eq. (5) (see Figure 2) and is convenient for use. This modified waveform of the current at the modulator output is given by the following time-domain equation:

$$i_{CM} = \sum_i \left\{ \left[12 \frac{I_{DC}}{T_L} \left(t - i \frac{T_L}{6} \right) - \frac{I_{DC}}{2} \right] \text{rect} \left(t - i \frac{T_L}{6} \right) + \left[-12 \frac{I_{DC}}{T_L} \left(t - \frac{T_L}{12} (2i+1) \right) - \frac{I_{DC}}{2} \right] \text{rect} \left(t - \frac{T_L}{12} (2i+1) \right) \right\} \quad (6)$$

where T_L is the period of the voltage in the power line, and $\text{rect}(t - \Delta T) = 1(t) - 1(t - \Delta T)$, while $1(t)$ is a Heaviside step function.

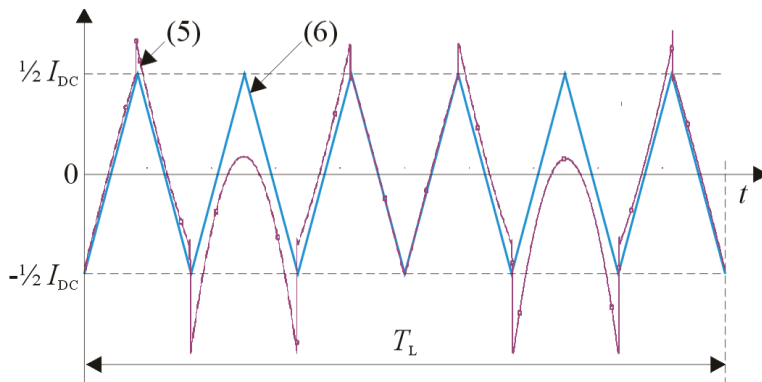


Figure 2. Shape of the theoretical current at the modulator output given in Eq. (5) (shown in red), and the current with a triangular shape given in Eq. (6) (shown in blue).

It is worth noting, however, that Eq. (6) is not supported by formal optimisation in the sense of the possibility of obtaining minimal distortions of the line currents from a sinusoidal waveform.

When Eq. (5) is replaced by Eq. (6), there is only minimal deterioration of the *THD* factor for the rectifier supply currents (Krystkowiak and Gwózdź, 2011; Supronowicz and Strzelecki, 1998). If the power line is symmetrical, the

value of *THD* factor for the power line current (i.e. at the input to TR) is about 1% in this case (Krystkowiak and Gwózdź, 2011; Supronowicz and Strzelecki, 1998). Thus, the structure of the current modulation stage should include a wide-pass band controlled current source (VCCS block), to precisely map the current at the modulator output to the desired signal for the modulator, u_{ref} . This is an essential requirement for the proper operation of the entire rectifier system, since it directly determines the quality of input (line) currents.

Initially, a standard single-channel topology was implemented in the current modulation stage (Krystkowiak and Gwózdź, 2011), which formed part of the laboratory setup of the rectifier system. However, the main focus of the current work involves the use of a power electronics-controlled current source in the modulator, which is in line with a multi-channel converters topology (Erickson and Maksimovic, 2001; Rashid, 2018b; Yang et al., 2015). This approach offers the benefits described in the following text, which is divided into four sections. Section 2 presents a basic description of a wide-band power electronics current source, in line with a multi-channel topology. Section 3 introduces the simulation model of the rectifier system. Section 4 describes selected laboratory tests of rectifier prototype, and Section 5 draws some conclusions.

2. Power Electronics Current Source Using Dual-Channel Topology

Figure 3 shows VCCS block diagram. This is using the conception of a dual-channel (interleaved) topology. Thus, the converter's total output current, i_L , is proportional to the sum of the currents, flowing in its individual channels, giving $i_L = \sum_{i=0}^{M-1} i_{L,i}$, where number of converter channels is M .

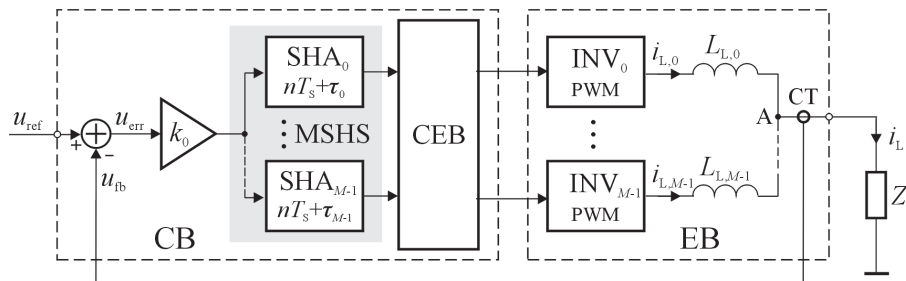


Figure 3. VCCS block diagram, using a dual-channel topology. CB, controller block; CEB, currents equalisation block; CT, current transducer; EB, execution block; MSHS, multichannel sample-and-hold amplifier block; VCCS, wide-pass band controlled current source.

The VCCS is a device that operates in a closed, voltage-type, negative feedback loop, meaning that system stability may be a problem. The individual inverters in an execution block (EB) of the current source are controlled in the PWM mode, with a constant value of the carrier frequency. One of the basic blocks of the controlled current source is a passive low-pass filter, which is included at the output of the current source power stage and consists of a set of inductors (in the number of M), connected in a quasi-parallel manner. This filter fulfils two basic functions: (I) it obtains a suitable value of the output impedance of the current source, and (II) it minimises the magnitude of the PWM signal components in the current source output current, thereby making it possible for the converter to meet the requirements for electromagnetic compatibility more easily compared to a current source with the standard topology (Erickson and Maksimovic, 2001; Rashid, 2018b).

The structure of the VCCS used in both the simulation and experimental models was built on three main blocks: the controller block (CB), the EB, and the current equalisation block (CEB), which is explained in Section 3. The CB consists of a P-type current regulator (with a gain factor k_0) and the multichannel sample-and-hold amplifier block (MSHS). The operation rules for the MSHS were presented in Gwózdź (2011). The EB consists of M half-bridge inverters, controlled in the PWM mode, and a set of inductors that are included at the outputs of these inverters. The EB is loaded by an impedance Z_L , where $Z_L = j\omega L_L + R_L$. The VCCS is controlled by the desired signal, u_{ref} , at the input of the CB.

For technical and economical reasons, a dual-channel converter ($M = 2$) was chosen for the VCCS (see Figure 4). In this particular case involving the use of the VCCS as a part of a rectifier system, its electrical structure was slightly modified from Figure 3. This was necessary because the pulse transformer in this system is implemented using a so called 'virtual ground'. This led to the use of a two dual-channel inverter in the EB.

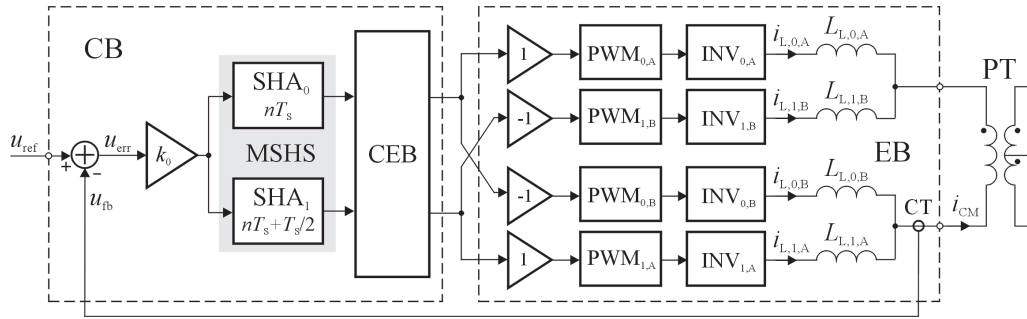


Figure 4. Block diagram of the current source in the dual-channel version, operating as a driver of the pulse transformer. CB, controller block; CEB, currents equalisation block; CT, current transducer; EB, execution block; MSHS, multichannel sample-and-hold amplifier block.

The CB therefore includes the following internal sub-blocks:

- A signal adder (A), which produces the error signal: $u_{\text{err}} = u_{\text{ref}} - u_{\text{fb}}$;
- A P-type current regulator, gain factor k_0 ;
- An order-2 MSHS, consisting of two sample-and-hold amplifiers connected in a quasi-parallel manner (Choi et al., 1996).

The EB includes the following internal sub-blocks:

- Four half-bridge type inverters;
- Four output filters ($L_{L,i,A/B}$: $i = 0, 1$);
- A current transducer (CT) to produce the feedback voltage, u_{fb} , which is proportional to the VCCS output current, i_L , where the CT is characterised by the transfer factor, r_{CT} , giving: $u_{\text{fb}} = r_{\text{CT}} i_L$.

The sampling moments and PWM signals in the individual channels of the converter were shifted relative to each other by a time $\frac{T_s}{2}$, where T_s is the signal sampling period. Therefore, from the point of view of such system stability, the converter ‘transfer function’ is more favourable to modification (Francis and Georgiou, 1988; Mirkin, 2005).

The type of modulation used in the PWM modulators was two-sided and symmetric. The load on the VCCS (i.e. the pulse transformer) was included in the circuit in a differential manner, meaning that voltages at the output of the inverter pair, $\text{INV}_{0,A}/\text{INV}_{0,B}$, were in anti-phase relative to each other. A similar situation applied at the voltages at the output of the inverter pair $\text{INV}_{1,A}/\text{INV}_{1,B}$. Since $M = 2$, the PWM carrier signals in these particular inverter pairs, i.e. $\text{INV}_{0,A}/\text{INV}_{0,B}$ and $\text{INV}_{1,A}/\text{INV}_{1,B}$, were shifted relative to each other by a time $\frac{T_C}{2}$, where $T_C = T_s$.

Thus, the important aspect of the operation of the current modulator stage is the assurance of its stability. A criterion for the asymptotic stability of the system, which was taken into account in this work, relates to a phenomenon of the signal’s spectrum aliasing effects, which occurs in real systems, involving sampled data. This phenomenon is not usually considered (Francis and Georgiou, 1988; Kaczorek et al., 2020; Kaźmierkowski et al., 2003). A full mathematical model of a control system for a dual-channel topology that is suitable for a stability analysis of this type was proposed in Gwózdź (2011). This analysis was in line with an extension of the Whittaker–Kotelnikov–Shannon sampling theorem known as the generalised sampling expansion, which was formulated by Papoulis (1977). The VCCS stability analysis given in Gwózdź (2011) yields the following formula for the maximal value of the current regulator gain:

$$k_{0,\text{max}} < \begin{cases} \frac{L}{r_{\text{CT}} T_s} & : M = 1 \\ 2 - \frac{L}{r_{\text{CT}} T_s} & : M = 2 \end{cases} \quad (7)$$

where L is the total load inductance (resistances are omitted from this formula).

So, the maximal theoretical value of the current regulator gain factor for the dual-channel converter is twice the value for a single-channel converter. This feature has a very valuable impact on the performance of the VCCS, since a control algorithm allows for a more accurate mapping of the VCCS output current in the desired signal.

3. Tests of the Simulation Model of the System

All tests were conducted in the ORCAD/PSPICE environment. The simulation model was 'powered' by a three-phase, 230V/50 Hz line, and the rated power delivered to the load was 6 kW. In general, the values of all parameters for this model were very close to those of the laboratory setup, and are listed in the following section. The common problem for the interleaved inverter topology depends on needs of equalisation currents in individual converter's channels. This problem was solved on the basis of the control algorithm, included in the CEB (see Figures 3 and 4), which was presented in the previous work (Gwóźdz, 2018). In result, in relation to both channels, the current spread did not exceed 3% (for the simulation model) and 5% (for the experimental model, see Section 4) of their instantaneous values.

Figure 5 shows the selected waveforms for the simulation model for the target shape of the desired signal (i.e. triangular), with a magnified section. These waveforms are related to the two cases for the order of the MSHS, i.e. $M = 1$ and $M = 2$. The value of the PWM signal period is $T_C = 0.1$ ms, while the rated magnitude of the desired signal is $A_{ref,n} = 10$ A. The value of the inductor in an individual channel of the converter is $L_{EM,f} = 1.25$ mH.

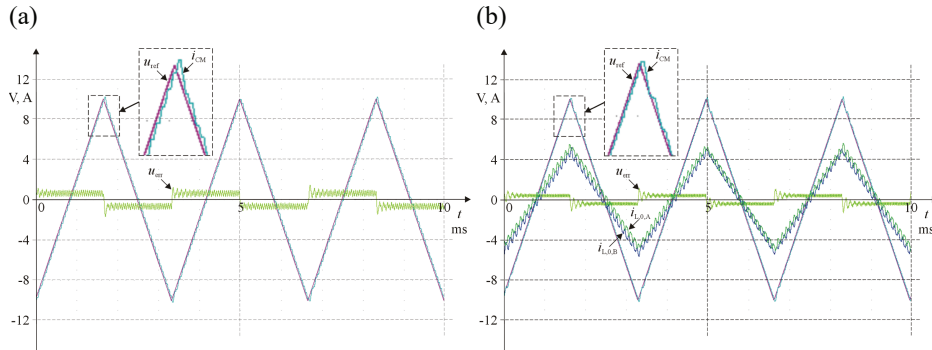


Figure 5. The measured signals for the simulation model of the current modulation stage, with desired signal (red), current at the modulator output (blue), error signal (green), for (a) the single-channel VCCS; (b) the two-channel VCCS, with currents in the individual channels. VCCS, wide-pass band controlled current source.

For the dual-channel VCCS, the shapes of the current at the modulator output and the desired signal almost coincide, whereas for the single-channel VCCS, these signals clearly differ from each other. As is the characteristic for interleaved converters, the first pulse modulation component of the current at the modulator output for the VCCS in the dual-channel version was set at a frequency of $\frac{4}{T_C}$ rather than $\frac{2}{T_C}$: $M = 1$ (Erickson and Maksimovic, 2001; Rashid, 2018b). The magnitude of this component is more than three times lower than for a single-channel topology, representing a great advantage of the interleaved topology.

An adequate and reliable criterion for assessing the quality of a converter's output signal is the converter control error, defined as follows (Kaczorek et al., 2020; Kaźmierkowski et al., 2003):

$$\varepsilon_{CTR} = \frac{\sqrt{|u_{ctr}|^2}}{\sqrt{|u_{ref}|^2}} 100\% = \frac{\sqrt{|u_{ref} - u_{fb}|^2}}{\sqrt{|u_{ref}|^2}} 100\%. \quad (8)$$

Assuming nominal conditions of operation for the simulation model, the values of this factor were obtained when the power delivered to the load was the rated values for $\varepsilon_{CTR} = 5.88\%$: $M = 1$ and $\varepsilon_{CTR} = 3.63\%$: $M = 2$. In line with this criterion, we find that the dual-channel VCCS makes it possible to improve the quality of the current at the modulator output by about 62%, on average, compared to the single-channel version.

The impact of the number of converter channels on the quality of the supply current was evaluated based on of the error ε_r . This error is related to the difference between the current waveform in a given power grid phase and that of its first harmonics, in a similar way to the converter control error. The value of this error is a function of the

power delivered to the load, P_{DC} , and the number of converter channels, M , as $\varepsilon_{i,M} = f\left(\frac{P_{DC}}{P_{DC,n}}\right)$: $M = 1, 2$, where $P_{DC,n}$ is the rated power delivered to the load.

A graph of this function showing the reciprocal relationship between the error functions (i.e. $\frac{\varepsilon_{i,2}}{\varepsilon_{i,1}}$) vs. the relative power delivered to the load is shown in Figure 6.

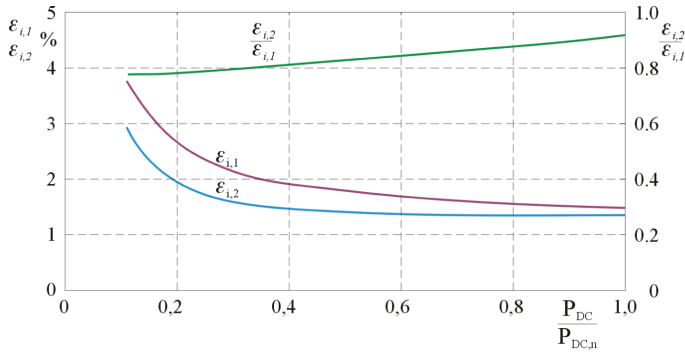


Figure 6. Curves for error functions for the one- and dual-channel versions of the VCCS and its reciprocal relationship vs. the relative power delivered to the load. VCCS, wide-pass band controlled current source.

Figure 7 shows additional examples of the waveforms obtained from the simulation model, where: (a) the current-modulation stage was disabled and the power delivered to the load was the rated value; (b) the

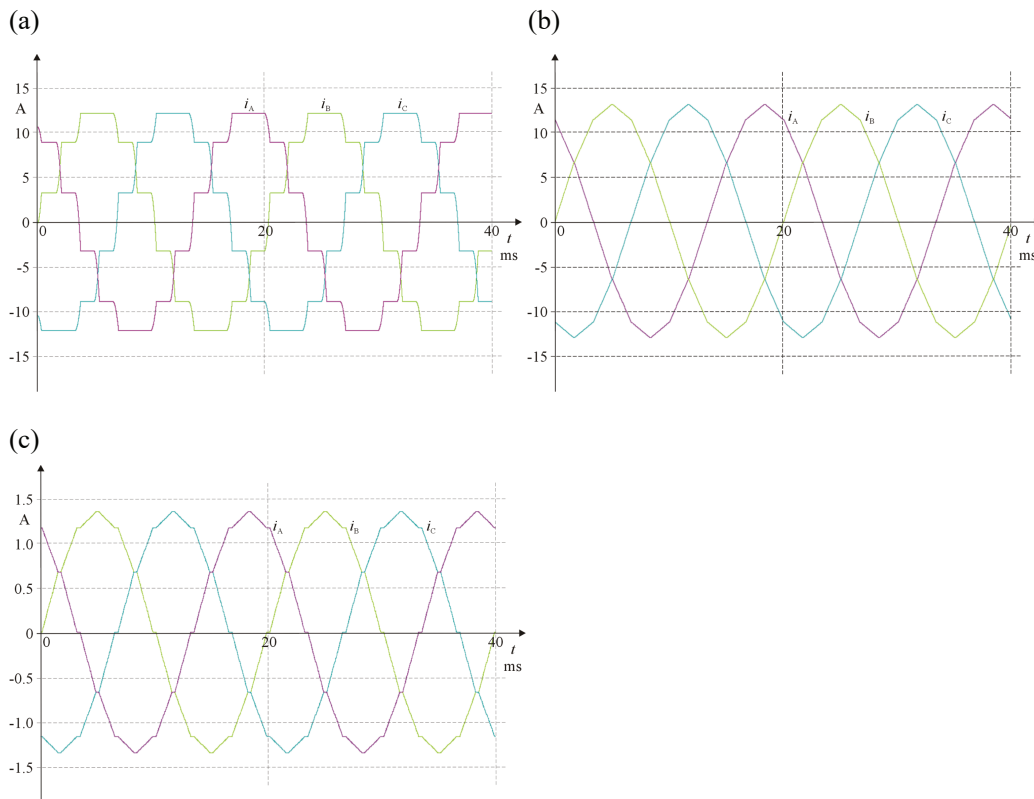


Figure 7. The measured signals for the supply currents in the simulated rectifier model.

current-modulation stage was enabled and the power delivered to the load was the rated value; and (c) the current-modulation stage was enabled and the power delivered to the load was 10% of the rated value.

When the current modulation stage was disabled, the value of THD for the supply current (in the given phase) was approximately 11.0% (measured in the 5 kHz band). This value is close to the typical value for a 12-pulse diode rectifier (Rashid, 2018b; Supronowicz and Strzelecki, 1998), but it depends on the operating conditions for the power line. ***When the current modulation stage was enabled, the deformation in the supply current was lower by one, that is, when the power delivered to the load was the rated value, the $THD = 1.35\%$, whereas when the power delivered to the load was 10% of the rated value, the $THD = 2.93\%$. The overall quality of the supply current increased by about 10.8%–28.3% when the dual-channel topology in the CM block was used, compared to a standard topology.

4. Laboratory Tests of the Rectifier System

A full laboratory setup of the rectifier system was then investigated, see Figure 8. The general aim of this study was to validate the theoretical assumptions and research results for the simulated rectifier model, primarily in relation to the quality of the modulator output current and the power line (transformer input) currents.

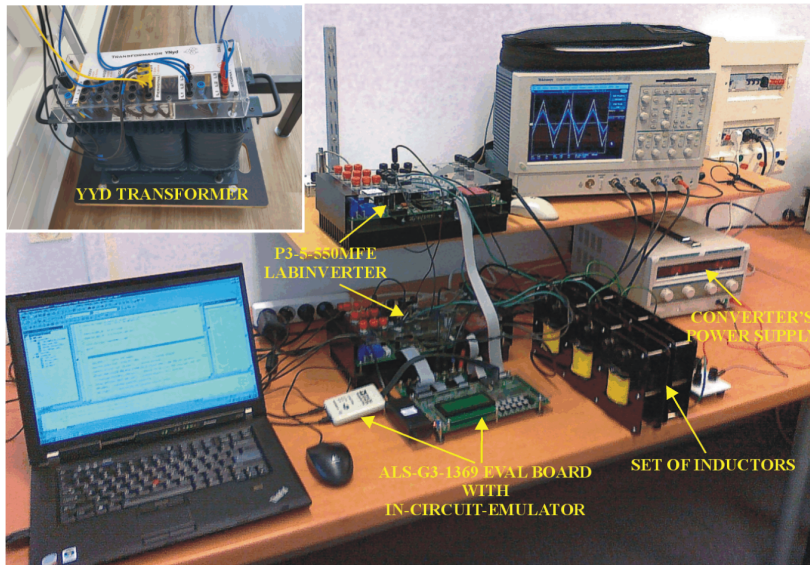


Figure 8. The general view of the laboratory setup.

Table 1 presents the values of the fundamental parameters of the laboratory setup.

Table 1. Parameters of the laboratory setup.

Parameters	Values
Power supply	230V, 50 Hz
Rated power delivered to the load	6 kW
Rated current magnitude at the modulator output	10 A
Voltage in the current modulation stage (DC rails)	60V
Coil inductance in an individual channel of the VCCS	1.25 mH
Frequency of the PWM signal in the VCCS execution unit	10 kHz
Frequency of signal sampling in the VCCS controller unit	10 kHz

VCCS, wide-pass band controlled current source.

The controller unit in the laboratory setup was the evaluation board with an ADSP-21369 SHARC® DSP (Analog Devices, Inc.). The execution unit used two power electronics converters (type P3-5-550MFE LABINVERTER) equipped with IPM/IGBTs (from Mitsubishi Electric). This type of converter was specially developed for advanced laboratory applications, related mainly to research works.

Investigations of the laboratory setup were carried out using values for the magnitude of the current modulation stage in the range 10%–100% in relation to the rated value. Converter configurations $M = 1$ and $M = 2$ were also tested. The solution for synchronising the desired signal of the current modulation stage with the line voltage waveform, which is very important for the correct operation of such systems, was a method described by the present author in Gwózdź and Ciepliński (2021). The main features of this algorithm are their exceptional resistance to voltage harmonic distortions in the power line and the very high accuracy of the synchronisation process itself.

Figure 9 shows chosen waveforms for the laboratory setup of the current modulation stage, with magnified sections of these currents. These waveforms represent the case where the desired signal for the modulator is the rated value.

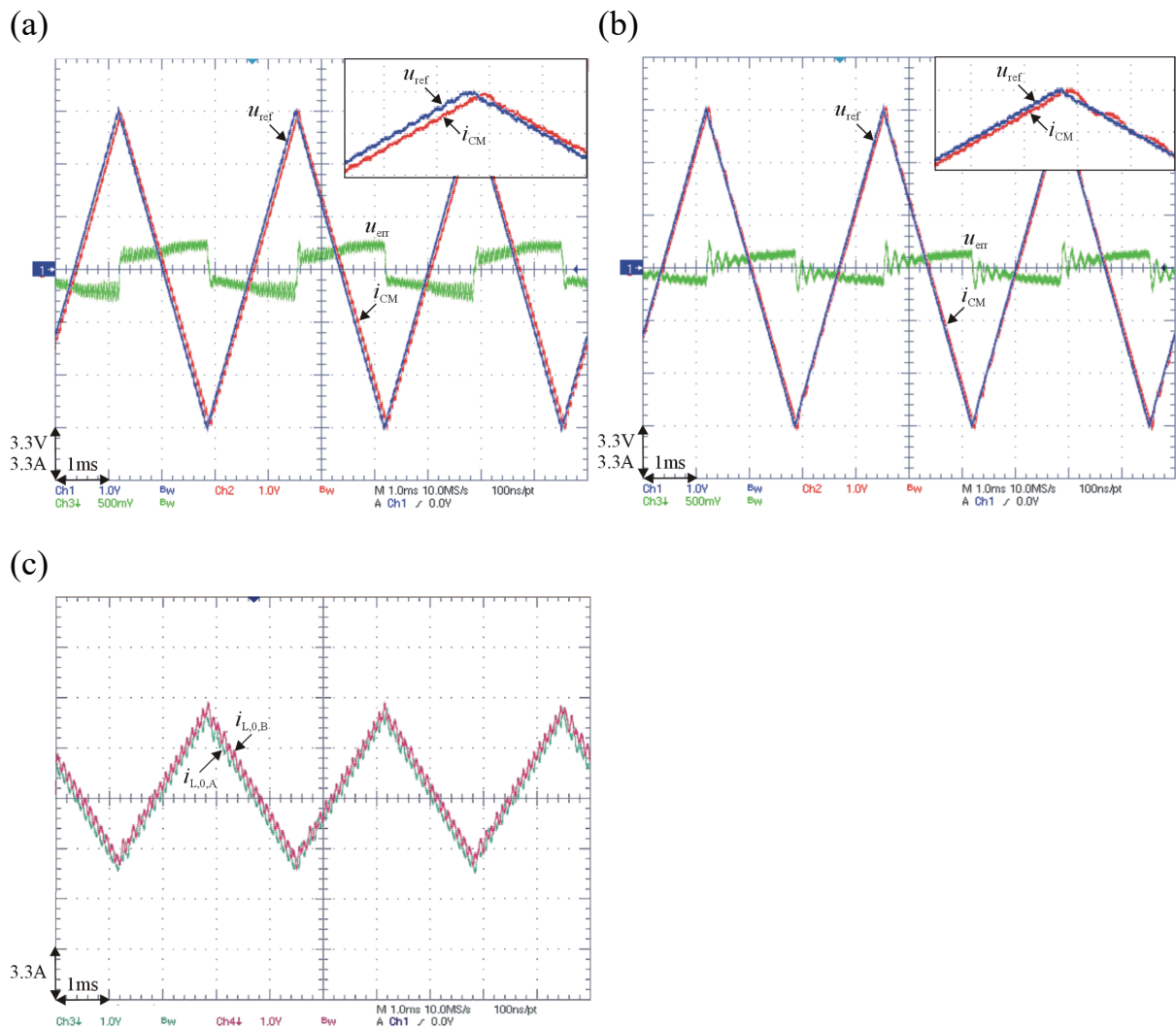


Figure 9. The measured signals for the laboratory setup of the current modulation stage for: (a) a single-channel VCCS, (b) the proposed dual-channel VCCS, showing the reference voltage (blue), current at the modulator output (red), error signal (green), and (c) currents in the individual converter's channels for the proposed dual-channel VCCS (horizontal axis: 1 ms/div, vertical axis: 3.3V/div, 3.3 A/div). VCCS, wide-pass band controlled current source.

In line with the assumption of nominal conditions for the operation of the laboratory setup, the values of the control errors were obtained as follows: $\varepsilon_{CTR} = 9.8\%$ for $M = 1$ and $\varepsilon_{CTR} = 5.9\%$ for $M = 2$. Thus, in regard to the control error criterion, the dual-channel current source makes it possible to improve the quality of the current by about 60% compared to the single-channel VCCS.

Figure 10 shows the line current for the rectifier system and its spectrum. The value of the power delivered to the load was very close to the rated value, and the current modulation stage operated in the dual-channel mode.

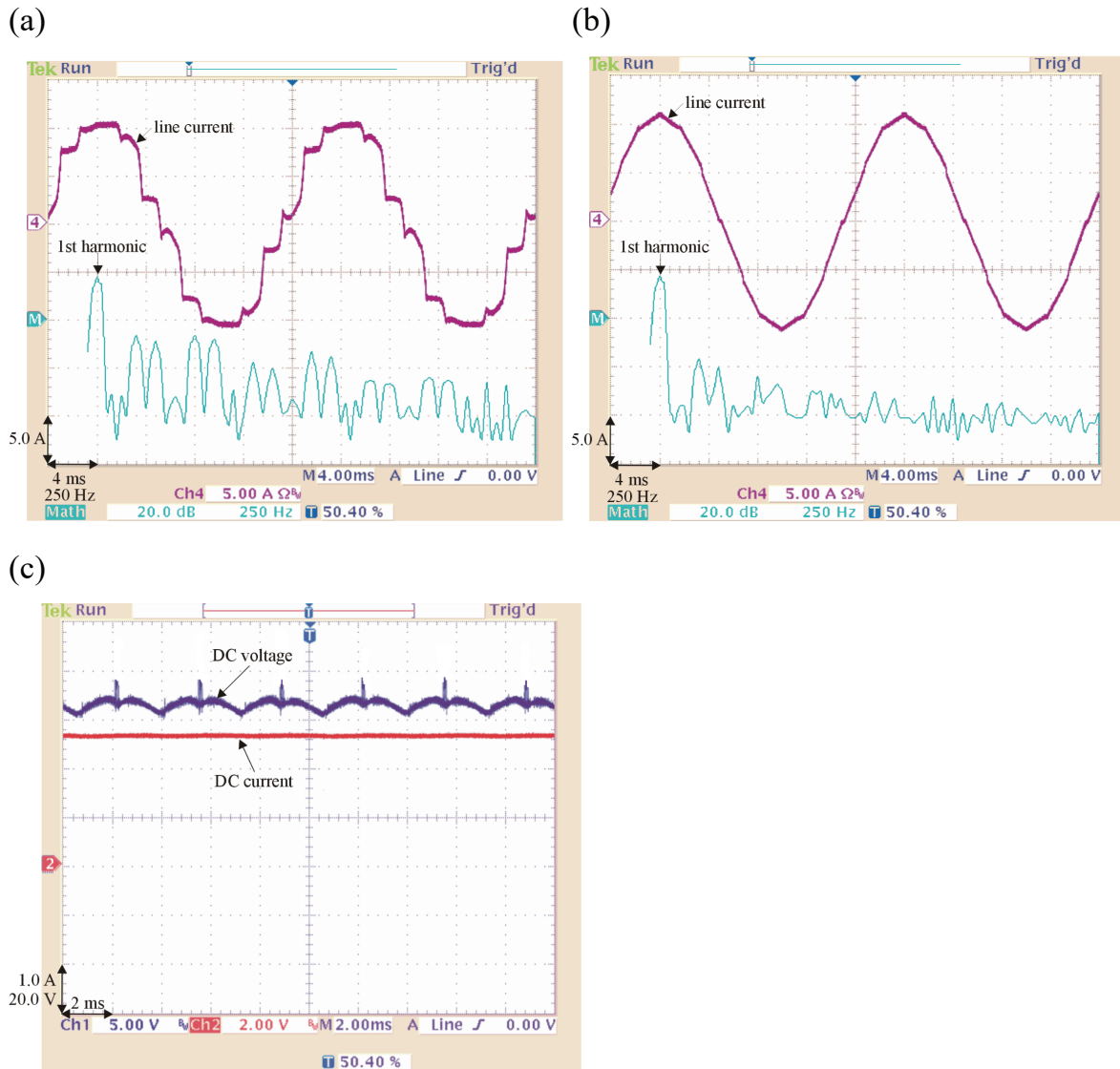


Figure 10. The measured signals of the line current in the laboratory setup of the rectifier system (red) and its spectrum (blue), with the current modulation stage: (a) turned off; (b) turned on (horizontal axis: 4 ms/div (waveform) and 250 Hz/div (spectrum), vertical axis: 5 A/div (waveform) and 5 A/div (spectrum)), and (c) turned-on – magnified portion of current (red) and voltage (blue) in the DC output circuit (horizontal axis: 2 ms/div, vertical axis: 1 A/div, 20V/div).

An analysis of the system shows the following values of its most characteristic parameter, that is, the *THD* of the power line current(-s):

- current modulator stage turned off: $THD = 11.6\%$,
- current modulator stage activated in the single-channel mode: $THD = 2.50\%$,
- current modulator stage activated in the dual-channel mode: $THD = 2.25\%$.

It can also be seen that the values of all the registered higher harmonics of this current are substantially lowered, by approximately 1.5–2.5 times, compared to a standard 12-pulse diode rectifier. Nevertheless, the given values differ from the theoretical ones, which is mainly because the ‘soft’ laboratory power line was applied as opposed to the simulation model (see Figures 7a and 10a); the simulation model was intended to verify the ‘clearly’ theoretical assumptions of the rectifier system operation.

5. Conclusion

This study has presented an alternative scheme leading to an increase in the quality of the supply current for a diode rectifier. To obtain this effect, current modulation was applied to the common DC link consisting of two six-pulse diode bridge rectifiers. To achieve this, the current modulation stage was a wide-band power electronics-controlled current source, equipped with a dual-channel topology, in its power stage. The control algorithm took into consideration aliasing effects, which occur in a sampled-data system and can have a strong influence on the stability of the system. This made it possible to maximise the effective gain of the regulator, and hence to achieve better mapping of the current at the modulator output in the desired signal. As the final result, the value of the *THD* for the supply current was significantly lowered compared to a standard 12-pulse diode rectifier. This finding offers the opportunity to reduce power losses in the transformer supplying both rectifiers.

In the case of the VCCS operating in the dual-channel version, the pulse modulation component in the current at the modulator output is set at a frequency that is twice as high as that of the single-channel version, and its magnitude is about three times lower. It is therefore expected that the dual-channel topology shall be able to meet the requirements for electromagnetic compatibility more easily compared to single-channel version, due to the much lower level of electromagnetic interference generated. However, a precise assessment of this phenomenon would require further research. It is also worth noting that the results of laboratory tests clearly confirmed the results of simulation model tests of individual system blocks, thus proving the correctness of the assumptions behind the design of these models. The solution described here for a rectifier system is particularly attractive in the case of high-power systems, since in practice, the power of the current modulation stage is only a few percent of the total power delivered to the load. Hence, the increased complexity of the proposed system is expected to have only a minimal impact on the overall cost of the rectifier. An additional advantage of this device is that in the event of a modulator failure, the system can continue to operate as a conventional 12-pulse diode rectifier.

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