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FPGA-Based Custom Hardware-in-the-Loop Emulation of High-Power Induction Motor Drives with Sub-Microsecond Resolution Using NI LabVIEW FPGA

Research paper

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Abstract: This paper presents the development and experimental validation of a custom Field-Programmable Gate Array (FPGA)-based hardware-in-the-loop (HIL) emulator for high-power induction motor drives. The proposed system enables real-time emulation of a variable-frequency drive consisting of a diode rectifier, a two-level voltage source inverter (VSI), and a 215 HP induction machine. The emulator is implemented on an NI PCIe-7857R FPGA platform using LabVIEW FPGA and fixed-point arithmetic optimised for Kintex-7 resources. A key contribution of this work is the achievement of a 100 ns real-time simulation time step for the converter and machine models, enabling accurate representation of fast switching dynamics while avoiding aliasing effects typically encountered in HIL systems. A multi-rate architecture is adopted to allocate appropriate sampling frequencies to different subsystems, improving computational efficiency and stability. Experimental results obtained from a closed-loop setup with an sbRIO-based controller demonstrate accurate emulation of inverter operation, induction machine dynamics, and controller interactions. The developed platform also enables detailed investigation of switching phenomena, such as voltage spikes, dead-time effects, and current ripple. Comparative validation with a Typhoon HIL 602+ platform confirms similar dynamic behaviour and harmonic performance, demonstrating that the proposed low-cost FPGA-based solution provides a flexible and high-fidelity alternative for real-time power electronics research and controller development.

Keywords: *LabVIEW FPGA • field-programmable gate array • power electronics • Real-Time emulator • hardware-in-the-loop*

1. Introduction

Hardware-in-the-loop (HIL) simulation is essential for safe and cost-effective development of power electronics systems, especially in high-power and rotating applications. Similar to Digital Twin concepts (Chen et al., 2023), HIL by emulating system components, reduces risks and streamlines development. Consequently, a wide range of commercial and industrial HIL systems are available for simulating complex systems, such as power electronics, converters, machines, power plants, and microgrids (Amin et al., 2019; Menga et al., 2025).

HIL setups are often tailored for intricate control board testing, particularly those involving complex finite-state machine (FSM) computations (Bun et al., 2011). Commercially available real-time HIL platforms, such as those from Typhoon (Iranian et al., 2022), Speedgoat (Lee and Choi, 2021), dSPACE (Aydin and Gulec, 2014), RTDS (Arraño-Vargas et al., 2024), and Opal-RT (Kotsampopoulos et al., 2018), are widely utilised in power systems and power electronics for HIL emulation and rapid prototyping (K. R. Alla and P. Pillay, 2026). Additionally, custom-designed HIL systems utilising FPGAs as real-time simulators (Iranian et al., 2022; Montano et al., 2017), as well as digital real-time solutions based on standard PC architectures such as NI PXI and PCIe systems, cater to both HIL applications and broader real-time power system simulations (Iranian et al., 2025).

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Commercial HIL systems are integral to validating research across various domains. For instance, Wang et al. (2022) utilised a dSPACE 1103 HIL system to validate novel phase-locked loops (PLLs) and frequency-locked loops (FLLs), demonstrating their accuracy in induction machine drive speed estimation during dynamic operations. Similarly, Nasab et al. (2024) showcased the broad utility of digital real-time systems in transmission power systems, using a combination of ABB's Unitrol 1020 and OPAL-RT to evaluate wide area damping controller (WADC) responses to power system stabiliser (PSS) interactions, examining both local and inter-area oscillations. Furthermore, Hu et al. (2023) employed a Typhoon 602+ system to compare control strategies for a double feed induction generator (DFIG), validating the broadband passivity enhancement effect of direct power control (DPC) with a filter. Their 1.5 MW DFIG model was controlled using a TMS320F28335-Spartan6 XC6SLX16 Digital Signal Processor (DSP) + FPGA control board, highlighting the diverse applications and capabilities of commercial HIL platforms.

Although commercial HIL platforms are widely used, custom HIL systems offer tailored solutions for specialised applications by providing flexible, scalable, and precise simulation capabilities—especially when certain case studies cannot be implemented due to limitations in predefined blocks of commercial tools (Šlapák et al., 2023). Some, such as Chowdhury and Sütő (2022), utilise affordable FPGA boards for rapid emulation of a simple model of an active front-end rectifier, reaching 40 ns time steps. For more complex systems, Iranian et al. (2014) explore cost-effective PC-based real-time targets, though their approach is constrained to time steps around 1 ms due to limited computational hardware resources—making it unsuitable for detailed converter-level studies. Dedicated hardware platforms, such as NI PXI used in Parizad et al. (2019), offer improved performance with time steps around 150 µs, yet still fall short of switch-level modelling. A more advanced custom HIL system proposed by Iranian et al. (2022) achieved a 5 µs time step using a DFIG model with fourth-order Runge–Kutta integration, but this still lags behind commercial benchmarks such as Typhoon HIL 602+ (500 ns) and Opal-RT OP5707 (145 ns) (Bai et al., 2024), which are better suited for high-fidelity real-time power electronics emulation.

As depicted in Figure 1, this manuscript introduces a novel and robust custom-designed HIL system engineered to achieve exceptionally low time steps. This performance is obtained through the unique combination of readily available PC hardware with an affordable, high-performance NI PCIe 7857R card for real-time processing. The reduction in time step significantly enhances the accuracy and stability of Ordinary Differential Equation (ODE) solutions, while also enabling the use of simpler integration methods such as the forward Euler solver by minimising numerical error and reducing overall computational cost. Furthermore, this enables the use of significantly higher switching frequencies for power inverters, facilitating the integration of high-speed GaN and SiC switches. This capability represents a significant advancement, as it allows for more accurate and realistic emulation of modern power electronic systems, which increasingly rely on these fast-switching devices.

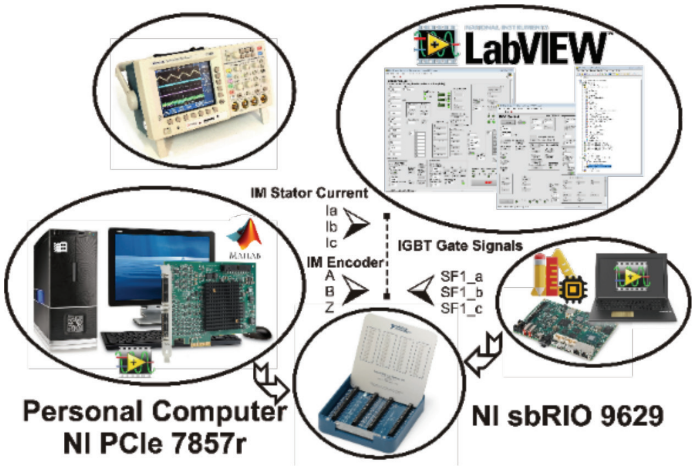

Figure 1. Scheme of HIL and RTS's configuration. HIL, hardware-in-the-loop.

Traditional HIL systems face challenges related to the proximity of input sampling frequency and switching frequency, which can induce sideband artefacts and undermine model reliability. Although oversampling techniques such as global gate drive signal oversampling (Osório et al., 2021) and integration oversampling (Zamiri et al.,

2023) have been proposed to mitigate these effects, they introduce additional computational complexity and implementation overhead.

Table 1 provides an updated comparison of the proposed system with representative commercial HIL platforms, including their latest achievable time-step capabilities. As shown, recent FPGA-based commercial solutions—particularly modular and multi-FPGA architectures such as OPAL-RT—can achieve sub-100 ns time steps under optimised configurations. However, most commercially available platforms typically operate in the range of hundreds of nanoseconds–microseconds, depending on model complexity and hardware structure.

Table 1. Non-modular custom made and commercial real-time HIL platform comparison.

Feature/ platform	Proposed HIL (Personal Computer + NI PCIe-7857R)	Typhoon HIL 602 +	PLECS RT Box 3	dSPACE DS1103	OPAL-RT OP1103	RTDS NovaCor Light
Primary use case	Flexible R&D, custom high-speed I/O, signal processing, HIL, and control prototyping.	Power electronics & microgrids HIL, motor drive testing.	Power electronics HIL, PLECS model deployment.	General-purpose HIL, automotive, motor control, and Power electronics HIL.	EMT simulation, Power electronics HIL, power systems.	Power grid real-time simulation, Power electronics HIL (utility-scale EMT).
Core hardware	X86 CPU + FPGA: Xilinx Kintex-7, customizable I/O via Flex-RIO adapter modules.	Custom multi-core CPU + Xilinx Ultra-Scale + FPGA, integrated analog/ digital I/O.	Intel CPU + Xilinx Zynq FPGA, modular I/O.	PowerPC + FPGA (older tech), modular I/O boards.	Intel Xeon/FPGA (heterogeneous), PCIe-based I/O.	Proprietary multi-core-processor hardware with dedicated I/O cards.
Software tool chain	LabVIEW and LabVIEW FPGA Also, MATLAB-Simulink HDL Coder.	Typhoon HIL SCADA, schematic editor, model libraries. (Limited to provided elements)	PLECS RT (standalone or with MATLAB), Coder.	Control-Desk, RTI, MATLAB/ Simulink integration.	OPAL-RT HYPERSIM, ePHASORSIM, RT-LAB, MATLAB/ Simulink.	RSCAD (proprietary), comprehensive power system library. (Limited to provided elements)
Typical latency/ Time step	100 ns–1 μs (FPGA loop). 20 μs (CPU).	250 ns–5 μs (FPGA), 50 μs (CPU).	1–10 μs (FPGA).	1–10 μs (FPGA), 50–100 μs (CPU).	10–50 μs (CPU-FPGA).	2–50 μs (depending on model size).
I/O & signal interfaces	Integrated: 8–8 analog I/O, 96 digital I/O, PWM, encoder, relay, current/voltage sources. and also Modular: AI/AO, DI/DO	Integrated: 16–32 analog I/O, 64+ digital I/O, PWM, encoder, relay, current/voltage sources.	Modular: analog, digital, PWM, encoder, resolver, CAN, Ethernet.	Modular boards: AI/AO, DI/DO, PWM, encoder, CAN, serial.	Modular: analog, digital, fiber optic (GTFPGA), Gigabit transceivers.	Proprietary I/O cards: analog, digital, GTNET (Ethernet) for PMU, IEC 61850, etc.
Software cost	High: LabVIEW FPGA ($5k), LabVIEW RT ($3k), additional toolkits.	Typhoon control centre licence ($15k).	PLECS RT licence ($20k), PLECS Coder extra.	High: Control-Desk, RTI, etc. ($30k in licences).	High: RT-LAB/ HYPERSIM licences ($40k).	Very High: RSCAD software licence ($65k).
Hardware cost (Approx)	$10k	$20k	$30k (depending on I/O).	$35k (base unit + I/O).	$70k (depending on configuration).	$200k (system + software).
Total rough system cost	$18k	$35k	$50k	$65k	$110k	$265k
Ecosystem & integration	National Instruments ecosystem and MATLAB/Simulink co-simulation	Standalone and modular; Typhoon HIL schematic-based.	Tight PLECS integration, some Simulink.	Deep MATLAB/ Simulink integration.	MATLAB/ Simulink, OPAL-RT-specific tools.	Specialized power system protocols (IEC 61850, DNP3, etc.).
Learning curve	Low (requires LabVIEW Graphical FPGA programming).	Moderate (schematic-based, but detailed).	Low (if using PLECS), moderate for custom models.	Moderate (Simulink users adapt easily).	Steep (specialized EMT knowledge).	Very steep (power system expertise required).
Min. time step (FPGA)	100 ns	200–500 ns	200 ns–1 μs	200 ns–1 μs	<100 ns (multi-FPGA configuration)	>1 μs

EMT, electromagnetic transient; HIL, hardware-in-the-loop; RTI, real-time interface.

In contrast, the proposed Controller Hardware-in-the-Loop (CHIL) system achieves a 100 ns simulation time step for a complete *dq*-frame model of a high-power induction motor drive, including the rectifier and two-level inverter, without relying on oversampling techniques. Importantly, this performance is obtained using a single-FPGA, non-modular architecture, as reflected in Table 1, which differentiates it from commercial solutions that often depend on multi-FPGA or heterogeneous processing frameworks to reach similar temporal resolution.

This reduced time step enables accurate representation of fast switching dynamics while maintaining computational efficiency through the use of a single-step Euler solver. Furthermore, it supports input sampling frequencies up to 1 MHz, allowing reliable interaction with high-speed controllers and reducing low-frequency oscillations, as demonstrated in a previous work (Zamiri et al., 2022).

It should be noted that these values depend on hardware configuration and model complexity. In particular, sub-100 ns time steps in commercial platforms are typically achieved using multi-FPGA architectures, whereas the proposed system achieves 100 ns using a single-FPGA implementation. To ensure a fair comparison, the systems included in Table 1 were selected based on comparable hardware categories and application domains. The results highlight that the proposed platform achieves competitive time resolution with significantly simpler architecture and lower cost, making it a practical alternative for high-fidelity real-time emulation of power electronic systems.

LabVIEW's flexibility is strategically exploited to address the specific requirements of each subsystem. For the induction machine and inverter models, High-Throughput Math Functions (HTMF) are employed to enable efficient fixed-point computations using single-cycle timed loops and pipelining, thereby satisfying strict timing constraints. In contrast, the rectifier is implemented using a synthesisable VHDL IP core generated via MATLAB/Simulink Hardware Description Language (HDL) Coder (Sanchez et al., 2012).

This hybrid implementation approach offers two main advantages: first, it accelerates development by reusing validated models, and second, it enhances real-time performance by assigning each subsystem to the most suitable implementation method. Unlike many commercial HIL platforms, which may impose limitations on solver selection or modelling flexibility, the proposed architecture leverages FPGA parallelism to achieve higher computational throughput and customisation. As a result, the combination of graphical programming and IP core integration enables high-fidelity real-time simulation of complex power electronic systems.

The main contributions of this work can be summarised as follows:

1. Development of a custom FPGA-based HIL system capable of achieving a 100 ns simulation time step for a complete *dq*-frame induction motor drive model, including rectifier and inverter stages.
2. Implementation of a multi-rate real-time architecture that balances computational efficiency and accuracy without relying on oversampling techniques.
3. Realisation of the system using a single-FPGA, non-modular, and cost-effective hardware platform, in contrast to commercial multi-FPGA solutions.
4. Experimental validation through a closed-loop setup, including detailed analysis of switching dynamics, torque response, and comparison with a commercial Typhoon HIL 602+ platform.

This paper proceeds with the following structure: Section II details the electrical models of the induction machine and its drive system. Section III outlines the real-time system architecture. Section IV describes the inverter's control design. Section V presents the experimental findings from the developed real-time FPGA-based HIL system. Section VI offers a comparative analysis between the implemented NI HIL system and Typhoon HIL602+ . Finally, Section VII summarises the conclusions drawn from this work.

2. Mathematical Modelling of Induction Machine and Variable Frequency Drive

This research creates a real-time simulation of a 215 HP induction motor and its drive system. Using mathematical models of the electrical components, the simulation is built in MATLAB/Simulink and LabVIEW FPGA, creating a real-time hardware-in-the-loop (RT-HIL) emulation platform. The motor is a standard single squirrel-cage type, and its drive includes a diode rectifier and a voltage source inverter (VSI). Figure 2 provides a visual representation of the block diagram depicting the induction machine and its drive system.COMP: Please hyphenate 'FPGA based controller' inside Fig. 2.

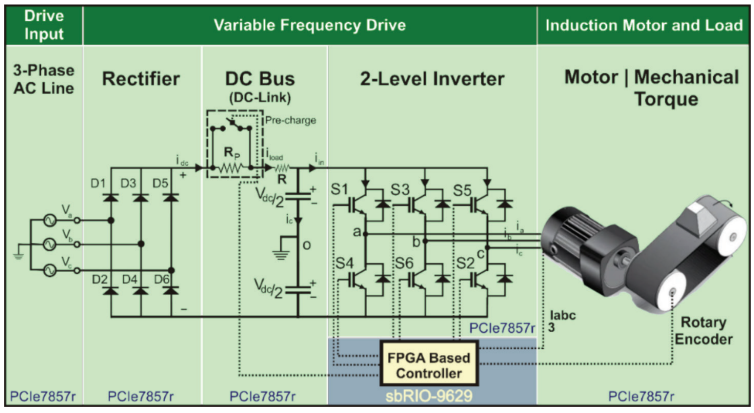

Figure 2. Overall model of 215 HP induction motor and its variable speed inverter setup.

2.1. Grid side rectifier

Figure 3 illustrates a three-phase full bridge diode rectifier (Zamiri et al., 2022) that generates a pulsating DC voltage with a six-pulse ripple (Lander, 1993). To reduce this ripple and improve DC output quality, filtering techniques such as RC circuits are used. The resulting capacitor voltage, known as the DC-link voltage, provides the DC power for the inverter stage, which drives the induction motor's stator windings.

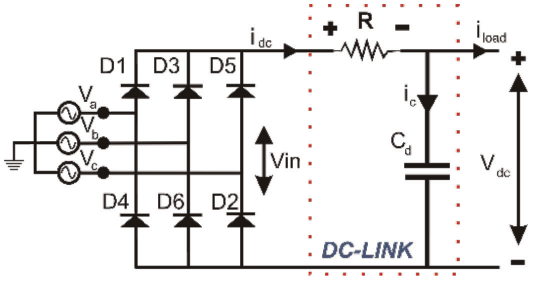

Figure 3. Three phase diode rectifier circuit topology.

The DC-link voltage is calculated using the following equations, derived from the equivalent circuit of the diode rectifier.

$$\frac{dV_{dc}}{dt} = \frac{1}{C_d}\left[\left(\frac{V_{in}}{R} - \frac{V_{dc}}{R} - i_{load}\right)\right] \tag{1}$$

Eq. (1) describes the pulsating DC voltage (V_{in}) at the rectifier output. R represents the total resistance of the DC-link, including the capacitor and the two diodes conducting at each moment. The load current, initially labelled i_{load}, is later redefined as i_{in} in part (B).

2.2. Stator side inverter

Figure 4 presents the schematic diagram of the VSI under investigation. A switching frequency of 5.7 kHz was employed in this study. Additional switching frequency and time-step conditions are analysed later in the experimental section. The following equations describe the input-output relationship, derived from the system's transfer function (TF) and considering dependent and independent variables (Byoung-Kuk and Ehsani, 2001),

$$[v_{ab},\ v_{bc}, v_{ca}] = TF \cdot V_{dc} \tag{2}$$

$$I_{in} = TF \cdot [I_a,\ I_b, I_c]^T \tag{3}$$

$$TF = [SF_1, SF_2] \tag{4}$$

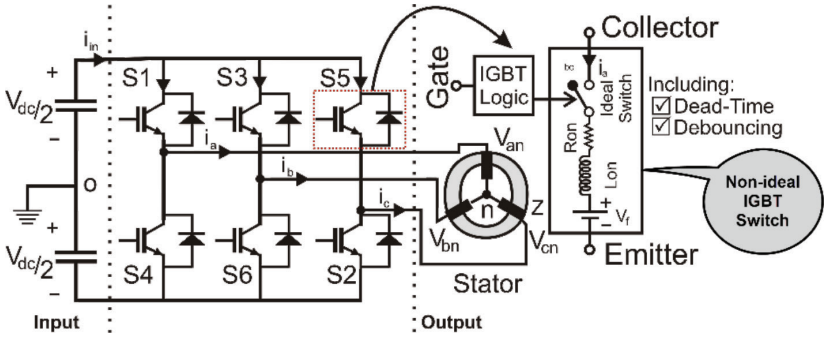

Figure 4. Circuit configuration of the presented VSI. VSI, voltage source inverter.

The control logic embedded in the FPGA of the control board dictates the switching functions (SF_x) of the HIL system. This control logic produces gate signals that drive the switches of the stator-side VSI. Consequently, the output voltages of the rotor-side VSI, namely V_{ao}, V_{bo} and V_{co}, can be represented as:

$$\begin{aligned} V_{ao} &= \left(\frac{V_{dc}}{2}\cdot SF_{1-a}\right) + L_{on}\cdot\frac{d\left(i_a\cdot SF_{2-a}\right)}{dt} - \left(R_{on}\cdot\left(i_a\cdot SF_{2-a}\right)+V_f\right) \\ V_{bo} &= \left(\frac{V_{dc}}{2}\cdot SF_{1-b}\right) + L_{on}\cdot\frac{d\left(i_b\cdot SF_{2-b}\right)}{dt} - \left(R_{on}\cdot\left(i_b\cdot SF_{2-b}\right)+V_f\right) \\ V_{co} &= \left(\frac{V_{dc}}{2}\cdot SF_{1-c}\right) + L_{on}\cdot\frac{d\left(i_c\cdot SF_{2-c}\right)}{dt} - \left(R_{on}\cdot\left(i_c\cdot SF_{2-c}\right)+V_f\right) \end{aligned} \tag{5}$$

This paper utilises signals SF_1 (+1 and −1 depending on the switch state in each leg (*a*, *b*, *c*) and SF_2 (+1 and 0 represent the voltage across the switching devices) acquired from the control board's digital I/Os (IGBT Gate Signals). They combined a non-ideal Insulated Gate Bipolar Transistor (IGBT) switch model that encompasses the output voltages V_{ao}, V_{bo}, and V_{co}, which are subsequently used to derive the inverter's line-to-line and phase voltages. By incorporating load currents, the switch currents are determined. The on-state resistance (R_{on}) and inductance (L_{on}) of the utilised IGBTs are considered, along with *Vf* and the forward voltage drop of the internal diode within the IGBT.

Given the system's operation at low frequencies with rapid sampling, the Euler method provides sufficient accuracy, as established in studies on equation discretisation (Comanescu, 2012). Consequently, the forward Euler method was implemented to approximate the current's rate of change, a critical factor in load control. This choice simplifies the process, avoiding the complexities of more advanced techniques such as zero-order hold (ZOH) or Tustin (Yanarates et al., 2023; Yushkova et al., 2021). The formula for this derivative is detailed in Eq. (6).

$$\frac{d\vec{i}_{abc}}{dt} = \frac{i_{abc}\left(k+1\right) - i_{abc}\left(k\right)}{T_s} \tag{6}$$

Where T_s is the simulation time step. The inverter line to line voltages are expressed as:

$$\begin{aligned} V_{ab} &= V_{ao} - V_{bo} \\ V_{bc} &= V_{bo} - V_{co} \\ V_{ca} &= V_{co} - V_{ao} \end{aligned} \tag{7}$$

Calculation of the inverter's phase voltage is achieved through:

$$V_{no} = \frac{1}{3}\left(V_{ao} + V_{bo} + V_{co}\right) \tag{8}$$

The phase voltages are given by:

$$\begin{aligned} V_{an} &= V_{ao} - V_{no} \\ V_{bn} &= V_{bo} - V_{no} \\ V_{cn} &= V_{co} - V_{no} \end{aligned} \tag{9}$$

To determine the load currents (I_a, I_b, I_c), consider that the load comprises the resistance and inductance of the induction machine's stator. These currents are subsequently calculated within the model of the presented asymmetric machine. Importantly, the IGBT switch currents are derived by multiplying the calculated load currents by SF2.

$$\begin{aligned} I_{s1} &= i_a \cdot SF_{2-a} \\ I_{s3} &= i_b \cdot SF_{2-b} \\ I_{s5} &= i_c \cdot SF_{2-c} \end{aligned} \tag{10}$$

Finally, the inverter input current (i_{in} *or* i_{load}) is derived from the switching currents using the following equations:

$$\begin{aligned} i_{in} &= i_{load} = I_{s1} + I_{s3} + I_{s5} \\ i_{in} &= I_a \cdot SF_{2-a} + I_b \cdot SF_{2-b} + I_c \cdot SF_{2-c} \end{aligned} \tag{11}$$

2.3. Induction machine in stationary reference frames

The dynamic state-space equations of the induction machine can be derived from its dynamic equivalent circuit (Ong, 1998), as illustrated in Figure 5. The inverter's output voltage space vector, expressed in the dq^s reference frame combined with the Euler method detailed in Eq. (6) for equation discretisation, is mathematically described by:

$$\begin{bmatrix} V^s_{qs} \\ V^s_{ds} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \tag{12}$$

$$\frac{d\Psi^s_{qs}}{dt} = \frac{\Psi^s_{qs}(k+1) - \Psi^s_{qs}(k)}{T_s} = \omega_b \left[V^s_{qs} + \frac{R_s}{X_{ls}} \left(\Psi^s_{mq} - \Psi^s_{qs} \right) \right] \tag{13}$$

$$\frac{d\Psi^s_{ds}}{dt} = \frac{\Psi^s_{ds}(k+1) - \Psi^s_{ds}(k)}{T_s} = \omega_b \left[V^s_{ds} + \frac{R_s}{X_{ls}} \left(\Psi^s_{md} - \Psi^s_{ds} \right) \right] \tag{14}$$

$$i_{os} = \frac{\omega_b}{X_{ls}} \left(v_{os} - i_{os} R_s \right) \tag{15}$$

$$\frac{d\Psi'^s_{qr}}{dt} = \frac{\Psi'^s_{qr}(k+1) - \Psi'^s_{qr}(k)}{T_s} = \omega_b \left[\frac{\omega_r}{\omega_b} \Psi'^s_{dr} + \frac{R'_r}{X'_{lr}} \left(\Psi^s_{mq} - \Psi'^s_{qr} \right) \right] \tag{16}$$

$$\frac{d\Psi'^s_{dr}}{dt} = \frac{\Psi'^s_{dr}(k+1) - \Psi'^s_{dr}(k)}{T_s} = \omega_b \left[\frac{-\omega_r}{\omega_b} \Psi'^s_{qr} + \frac{R'_r}{X'_{lr}} \left(\Psi^s_{md} - \Psi'^s_{dr} \right) \right] \tag{17}$$

$$i'_{\mathrm{or}} = \frac{\omega_b}{X'_{lr}} \left(v'_{or} - i'_{or} R'_r \right) \tag{18}$$

$$\Psi^s_{mq} = X_m \left(\frac{\Psi^s_{qs}}{X_{ls}} + \frac{\Psi'^s_{qr}}{X'_{lr}} \right) \tag{19}$$

$$\Psi^s_{md} = X_m \left(\frac{\Psi^s_{ds}}{X_{ls}} + \frac{\Psi'^s_{dr}}{X'_{lr}} \right) \tag{20}$$

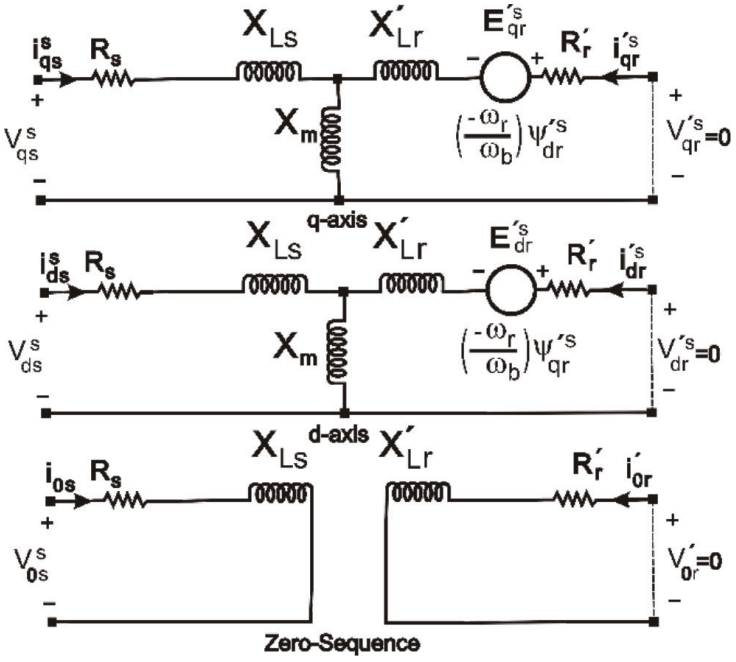

Figure 5. The equivalent circuit of a squirrel-cage induction machine in stationary *dq* coordinates.

where the stator current and rotor current are expressed as:

$$i^s_{qs} = 1/X_{ls}\left(\Psi^s_{qs} - \Psi^s_{mq}\right) \tag{21}$$

$$i^s_{ds} = 1/X_{ls}\left(\Psi^s_{ds} - \Psi^s_{md}\right) \tag{22}$$

$$i'^s_{qr} = 1/X'_{lr}\left(\Psi'^s_{qr} - \Psi^s_{mq}\right) \tag{23}$$

$$i'^s_{dr} = 1/X'_{lr}\left(\Psi'^s_{dr} - \Psi^s_{md}\right) \tag{24}$$

and the electromagnetic torque in per-unit, active and reactive power of stator and rotor can be calculated as follows:

$$T_e = \frac{3}{2}\frac{P}{2\cdot\omega_b}\left(\Psi^s_{ds}\cdot i^s_{qs} - \Psi^s_{qs}\cdot i^s_{ds}\right) \tag{25}$$

The equation of motion, when expressed in per unit values based on the machine's own base power and voltage, can be represented as:

$$2H\frac{d(\omega_r/\omega_B)}{dt} = T_{\text{em}+}T_{\text{mech}} - T_{\text{damp}} \tag{26}$$

Where *H* is inertia constant. This dimensionless parameter represents the ratio of the kinetic energy stored in the rotating mass at base speed to the machine's rated power. Table 2 details the squirrel-cage induction machine parameters.

$$H = \frac{j\omega^2_{bm}}{2S_b} \tag{27}$$

Table 2. The parameters of the studied squirrel-cage induction machine.

Parameter	Symbol	Value
Nominal power	P_n	160 KW
Voltage (line to line)	V_n	400 V
Nominal frequency	F	50 Hz
Pole	P	4
Speed	N	1500 RPM
Magnetizing inductance	X_m	0.0236 H
Stator resistor	R_s	0.0138 Ω
Rotor resistor	$R_r^{'}$	0.0077 Ω
Base angular speed	ω_b	314.1593 *rad/s*
Stator inductance	X_{ls}	0.0487 H
Rotor inductance	$X_{lr}^{'}$	0.0478 H
Inertia	H	0.1901

3. Real-Time System Architecture and Timing

A cost-effective RT-HIL system for induction machine and drive research can be built using a standard PC with an NI R-Series PCIe multifunction I/O device, such as the NI PCIe 7857R. This approach offers a high-performance, affordable solution for custom HIL applications. LabVIEW's graphical interface provides a flexible platform for real-time modelling on NI R-Series cards. The LabVIEW FPGA module enables engineers to either develop custom algorithms or incorporate existing IP cores, optimising performance on Xilinx FPGAs and fostering code reuse.

Figure 6 illustrates the system, featuring a single squirrel-cage induction machine with a rotary encoder and an IGBT-based VSI implemented in LabVIEW FPGA. A hybrid modelling approach is employed, where the customisable design capabilities, the three-phase AC line, pre-charge, and diode rectifier are initially modelled in MATLAB/Simulink using HDL Coder, and the resulting VHDL code is integrated into LabVIEW FPGA via IP Integration for Kintex 7 FPGA synthesis. Unlike typical commercial HIL systems relying solely on MATLAB/Simulink models (Saran et al., 2008), this study combines LabVIEW FPGA and MATLAB/Simulink, using fixed-point variables for equations from Section II. LabVIEW FPGA facilitates custom hardware logic development and debugging (Iranian et al., 2025), while MATLAB Simulink with HDL Coder generates synthesisable hardware description languages (Iranian et al., 2022).

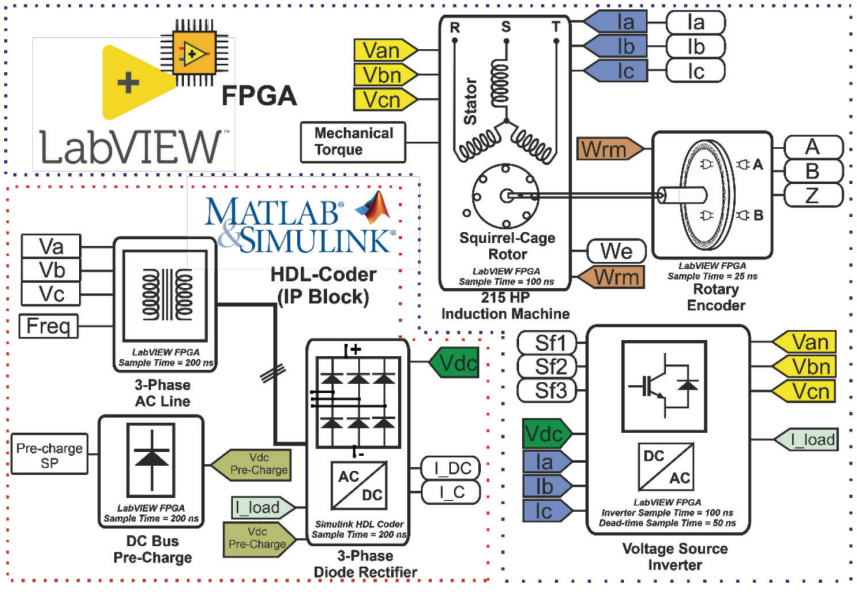

Figure 6. Block diagram of the presented model in LabVIEW FPGA and MATLAB/Simulink.

The FPGA implementation employs a multi-rate architecture based on parallel timed loops to optimise performance. An initial critical path analysis determined the minimum achievable time step, facilitating the assignment of tailored operating frequencies to each subsystem. Aliasing effects are mitigated through the combined use of a sufficiently small simulation time step and appropriate sampling frequency selection. Specifically, the 100 ns time step ensures that the sampling frequency is significantly higher than the converter switching frequency and its associated harmonics, thereby satisfying the Nyquist–Shannon sampling criterion and preventing the misinterpretation of high-frequency components. In addition, fast dynamic subsystems such as the induction machine and inverter operate at 10 MHz (100 ns), while slower subsystems such as the AC line and diode rectifier operate at 5 MHz (200 ns). The encoder simulator operates at 40 MHz (25 ns) to provide high-fidelity rotor speed signals, the analogue output at 1 MHz (1000 ns), and dead-time/debouncing processes at 20 MHz (50 ns). This hierarchical sampling strategy prevents spectral overlap between switching harmonics and control signals, enabling accurate representation of fast switching dynamics while maintaining computational efficiency, without the need for additional oversampling techniques.

The clock frequency of the Kintex-7 FPGA (40 MHz) and the critical path delay of the models dictate the minimum achievable time step. In this study, a 100 ns time step was determined to be the minimum for the induction machine, which exhibits the most computationally intensive dynamics. In addition, this time step provides sufficiently high temporal resolution relative to the converter switching frequency and its associated harmonics, ensuring accurate representation of fast switching dynamics.

This relatively small time step enables the application of Euler's method—a first-order, explicit numerical procedure—for solving the ODEs governing the induction machine's behaviour. This reduced time step also mitigates potential numerical instability of the fixed-step forward Euler solver, particularly in stiff systems.

For comparative analysis, the fourth-order Runge–Kutta (RK4) method was also implemented. While RK4 offers improved accuracy and stability compared to Euler's method, it requires increased computational resources for concurrent execution or a larger effective sampling time in sequential implementation (Iranian et al., 2025). To provide a comparison with other numerical solvers, the induction machine's stator current tracking accuracy at 300 A (amplitude) was evaluated using the switch-based mean absolute error (SMAE), computed over an 80 ms period under identical test conditions. The SMAE values were 5.6839 A for the Euler method and 5.6723 A for RK4, reflecting a marginal accuracy improvement of 0.204% for RK4. Given the emphasis on computational efficiency, this minor enhancement is considered negligible. A comparative visualisation of stator current errors and their difference for both solvers over 4 cycles (80 ms) is presented in Figure 7. In addition, intermediate numerical methods such as second-order Runge–Kutta (RK2) or trapezoidal integration would be expected to yield results between those obtained with Euler (first-order) and RK4 (fourth-order). However, these methods also require increased computational resources compared to Euler, making them less suitable for real-time FPGA implementation under strict timing constraints (Yushkova et al., 2021).

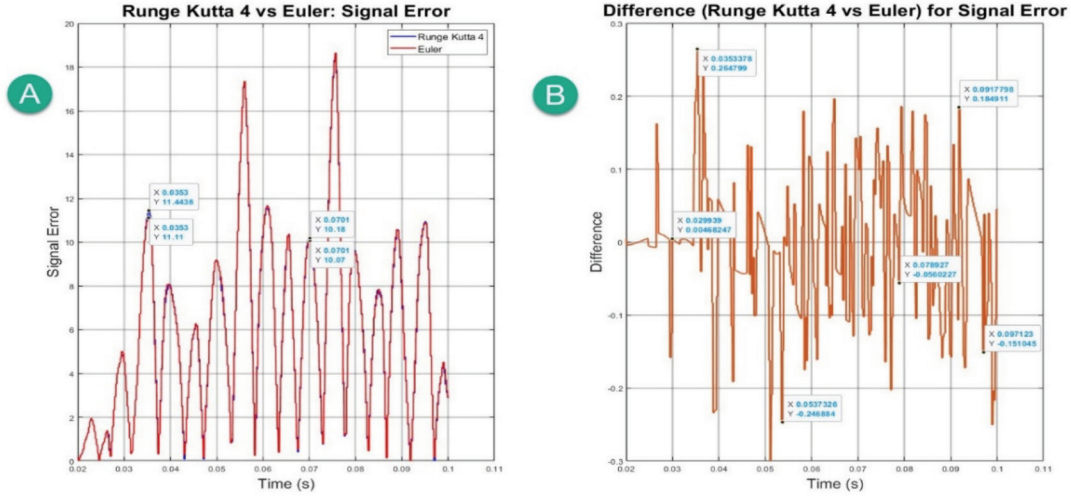

Figure 7. Signal error comparison of stator current (I_a). (A) Setpoint and actual stator current error (RK4 and Euler), (B) Setpoint and actual stator current error difference.

The final compilation stage for the provided complex model, using Xilinx Vivado, translates the design into an FPGA implementation through synthesis, placement, and routing. Table 3 details resource utilisation, including slices, registers, Look-Up Tables (LUTs), RAM, and DSP blocks. The resource utilisation remains within acceptable limits, although DSP usage is relatively high, indicating efficient utilisation of available computational resources. The compilation tool also analyses timing performance, ensuring real-time operation.

Table 3. NI FPGA used resources during compilation for the proposed custom-made HIL.

Device utilization	Used	Total	Percent (%)
Total slices	10,149	25,350	40
Slice registers	21,163	202,800	10.4
Slice LUTs	25,556	101,400	25.2
Block RAMs	4	325	1.2
DSP48s slices	490	600	81.7

4. Real-time Control Platform

4.1. Hardware specification

The NI sbRIO9629, featuring an Intel Atom processor and Xilinx Artix-7 FPGA, functions as the 215 HP induction machine controller. It receives real-time signals via 16-bit analogue inputs, interfaces with relays and encoders through digital I/Os, and communicates with a host PC via Ethernet. The controller executes control algorithms at a 200 ns cycle, generating a selectable range of 5.7–200 kHz Pulse Width Modulation (PWM) signals for the HIL converter's switches. The asynchronous operation of the controller and the HIL emulator, unlike synchronised real-time simulators, presents a risk of aliasing. Specifically, a large time step in the HIL emulator can generate aliased low-frequency components, potentially causing critical steady-state oscillations. To avoid this, the HIL system time step can be adjusted from 100 ns to 10 µs to avoid a lack of simulation regarding mathematical conversions and steady-state oscillations.

4.2. Control philosophy and timings

In a DC machine, the armature and field windings are designed to be orthogonal, creating perpendicular magnetic fields. Assuming negligible iron saturation, these fields interact minimally, allowing the developed torque to be expressed as:

$$T_{em} = k_a \phi\left(I_f\right) I_a \tag{28}$$

Where k_a is a constant coefficient, $\phi\left(I_f\right)$, the measured field flux by especial instrumentation, and I_a the armature current. Controlling torque in a three-phase induction motor is more complex than in DC machines due to the dynamic interaction of stator and rotor fields, which lack a fixed 90° orientation. Flux sensing issues at low speeds further complicate matters. Indirect field orientation control (IFOC) (Ong, 1998) provides a robust alternative. This control strategy eliminates the need for direct air-gap flux measurement. Instead, IFOC leverages a key principle, as long as the rotor flux linkage, $\lambda_{dr}^{'e}$, remains constant, and the developed torque can be independently controlled by adjusting the *q*-axis component of the stator current ($i_{qs}^{'e}$). This relationship is mathematically described in Eq. (29) where, $p = \frac{d}{dt}$.

$$T_{em}^{*} = \frac{3}{2}\frac{p}{2}\frac{L_m}{L_r^{'}}\lambda_{dr}^{'e} i_{qs}^{e} \tag{29}$$

In practical IFOC, the rotor flux magnitude is precisely controlled by adjusting the *d*-axis stator current (i_{ds}^{e}), as shown in Eq. (30). Maintaining proper field orientation involves regulating either the slip speed or the *q*-axis stator current (i_{qs}^{e}) according to Eq. (31). With successful field orientation, the rotor flux linkage ($\lambda_{dr}^{'e}$) aligns with the *d*-axis, and its rate of change is dictated by the rotor circuit time constant $\left(T_r = \frac{r_r^{'}}{L_r^{'}}\right)$.

$$\lambda_{dr}^{*e} = \frac{r_r^{'} L_m}{r_r^{'} + L_r^{'} p} i_{ds}^{e} \tag{30}$$

Eq. (31) defines the slip speed relationship between *d*-*q* stator current components, ensuring precise alignment of the synchronously rotating reference frame with the rotor field. This alignment is critical for successful field orientation control in induction motors.

$$\omega_{sl}^{e} = \left(\omega_{e} - \omega_{r}\right) = \frac{r_{r}^{'}}{L_{r}^{'}} \frac{i_{qs}^{e}}{i_{ds}^{e}} \tag{31}$$

Decoupling algorithms are critical for improving induction motor control performance (Hazzab et al., 2006), as they compensate for the inherent cross-coupling between the *d*- and *q*-axis components of the machine model. This transformation effectively linearises the system, allowing independent control of flux and torque and enabling the use of classical control strategies such as Proportional–Integral (PI) controllers.

In this work, the PI controller gains were initially estimated using the Ziegler–Nichols open-loop tuning method and subsequently refined through simulation and experimental validation within the HIL environment to achieve stable operation, fast dynamic response, and minimal steady-state error.

Without the decoupling algorithm, the interaction between flux and torque components introduces non-linear effects that can result in slower transient response, increased oscillations, and reduced control accuracy, particularly under dynamic operating conditions. Although basic operation can still be achieved, the overall performance is significantly degraded.

This linearisation and tuning process contributes to improved system stability and smoother motor dynamics (Fateh Mehazzem et al., 2008). Key elements of the decoupling algorithm include:

$$V_{ds}^{Decouple} = -\left[\omega_{sl} K_{L} i_{qs} + \frac{L_{m}}{L_{r} T_{r}} \lambda_{dr}^{'e}\right] \tag{32}$$

$$V_{qs}^{Decouple} = \left[\omega_{sl} K_{L} i_{ds} + \frac{L_{m}}{L_{r}} \lambda_{dr}^{'e}\right] \tag{33}$$

Where $K_{L} = L_{s} - \frac{L_{m}^{2}}{\left(L_{r} + L_{m}\right)}$ and $T_{r} = \frac{L_{r}}{R_{r}^{'}}$. The general control structure of the converter is shown in Figure 8.

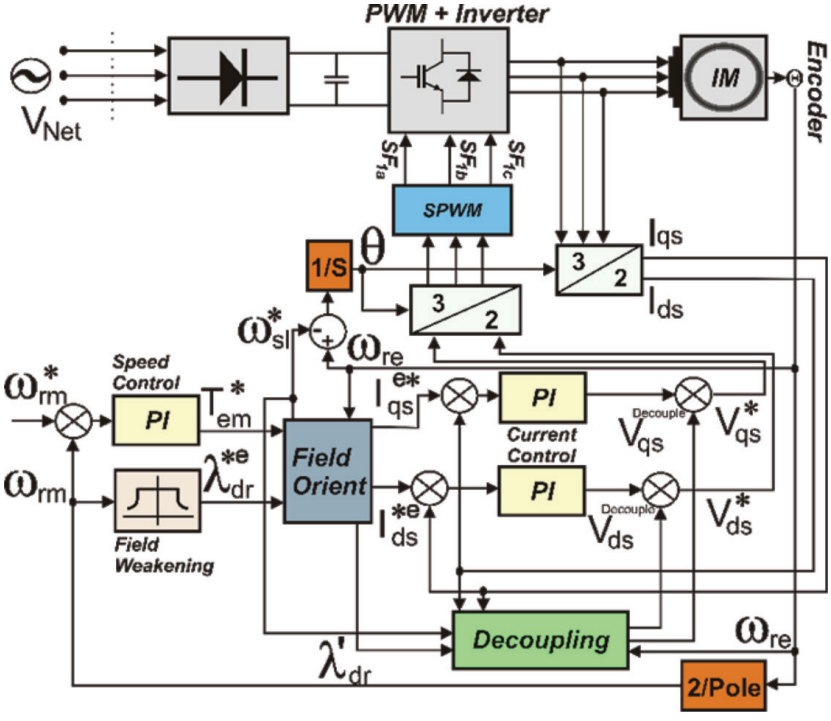

Figure 8. General control structure of converter.

5. Experimental Test Results

The experimental setup consists of a real-time HIL emulator implemented on a National Instruments PCIe-7857R platform featuring a Kintex-7 FPGA, and a controller based on the NI sbRIO9629 system. The controller executes the control algorithm with a 200 ns cycle time and generates PWM signals in the range of 5.7–200 kHz. The HIL system emulates the complete power stage, including the diode rectifier, DC-link, and two-level VSI, as well as the electrical and mechanical dynamics of the induction machine. The system is developed using a combination of MATLAB/Simulink and LabVIEW FPGA, enabling high-fidelity real-time emulation. Real-time interaction between the controller and the HIL emulator is achieved through analogue and digital I/O interfaces, forming a closed-loop configuration as illustrated in Figure 9. This setup allows realistic validation of the control system under various operating conditions. Measurement signals are acquired using a Tektronix oscilloscope with a 2.4 GHz sampling rate, ensuring accurate capture of high-frequency switching phenomena and transient responses.

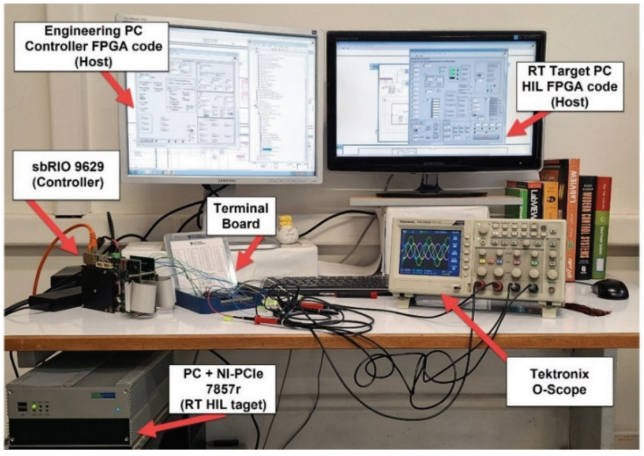

Figure 9. Overview of 215 HP (160 kW) induction machine and its two-level IGBT base inverter.

5.1. Inverter's startup

After the closure of the three-phase AC switch (either symmetric or asymmetric) and DC-link capacitor pre-charge (simulated with an initial value), the diode rectifier produces a 300 Hz DC voltage (Figure 10). With the DC link charged, the sbRIO9629 initiates the startup, driving the four-pole induction machine to 1500 RPM with a 157 rad/s setpoint (Figure 11). Upon reaching the setpoint, the system enters steady-state, ready for speed or torque variations. Figure 12 shows stator currents and rotor speed under a −500 N·m (73 kW) load torque.

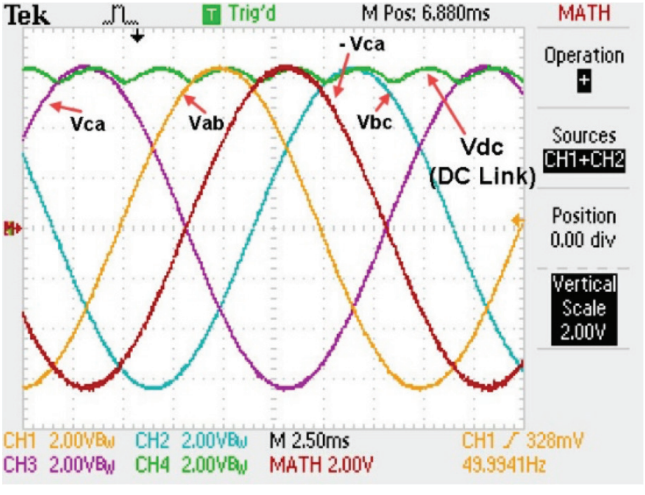

Figure 10. Full-wave bridge diode rectification of three-phase voltage. CH1 (orange) V_{ab}, CH2 (Cyan) V_{bc}, CH3 (Purple) V_{ca}, CH4 (Green) V_{dc} and MATH ($[\![-V]\!]_{ca}$). (Scale voltage: 100 V or Ampere per 1 V DAC). DAC, digital to analogue converter.

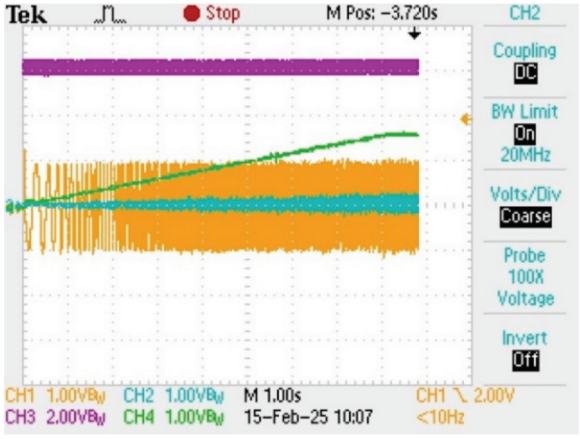

Figure 11. Induction machine's start-up. CH1 (orange) I_a, CH2 (Cyan) Electromagnetic Torque, CH3 (Purple) V_{dc}, CH4 (Green) Speed. (Scale voltage: 100 V or Ampere per 1 V DAC). DAC, digital to analogue converter.

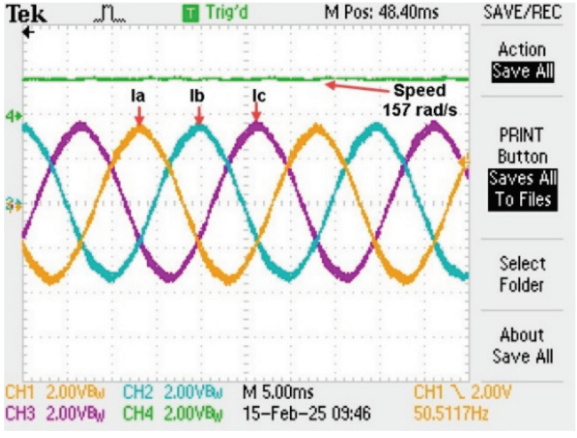

Figure 12. Stator current and speed in steady state operation. CH1(orange) I_a, CH2 (Cyan) I_b, CH3 (Purple) I_c, CH4 (Green) Speed (rad/s). (Scale voltage: 100 V or Ampere per 1 V DAC). DAC, digital to analogue converter.

5.2. Torque variation in nominal speed

The primary goal of IFOC is to maintain motor controllability and DC link voltage stability under varying load conditions (TL). Figure 13 demonstrates this in a 215 HP induction machine HIL setup, showing the system's response to a 900 N·m load application and removal. The results demonstrate the robustness and stability of

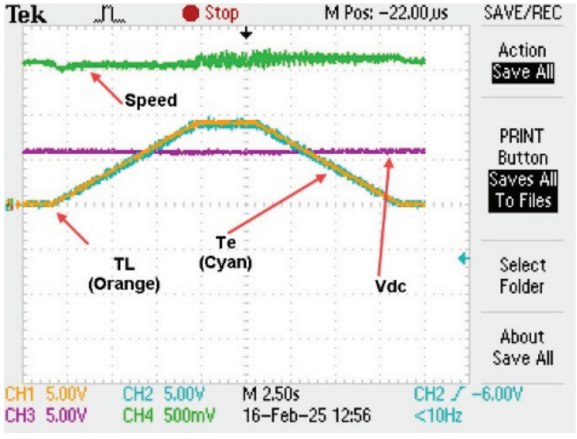

Figure 13. Load increase from 0 to 900 N·m. CH1 (orange) T_L, CH2 (Cyan) T_e, CH3 (Purple) V_{dc}, CH4 (Green) Speed (rad/s). (Scale voltage: 100 V or Ampere per 1 V DAC). DAC, digital to analogue converter.

the implemented IFOC system under varying load conditions. However, the observed speed ripple suggests that further improvement in speed regulation could be achieved through refined controller tuning or the implementation of additional filtering strategies.

For a reference speed of 157 rad/s (1500 RPM), the measured mean speed is approximately 160 rad/s (1527 RPM), indicating a steady-state deviation. The instantaneous speed varies between 150 rad/s (1432 RPM) and 174 rad/s (1661 RPM), resulting in a speed ripple of approximately ±12 rad/s (±79 RPM). This relatively high ripple suggests that further refinement of the control loop parameters or the application of additional filtering techniques could improve speed regulation performance.

5.3. Torque variation in low speed

Another IFOC objective is effective torque control at low rotor speeds. Figure 14 shows that at 10 rad/s (95 RPM), a 900 N·m torque application, applied within approximately 8 s, causes a significant increase in stator current (I_a), while rotor speed and DC link voltage (V_{dc}) remain stable. This demonstrates the system's ability to maintain stable operation and precise torque control at low speeds, crucial for demanding applications.

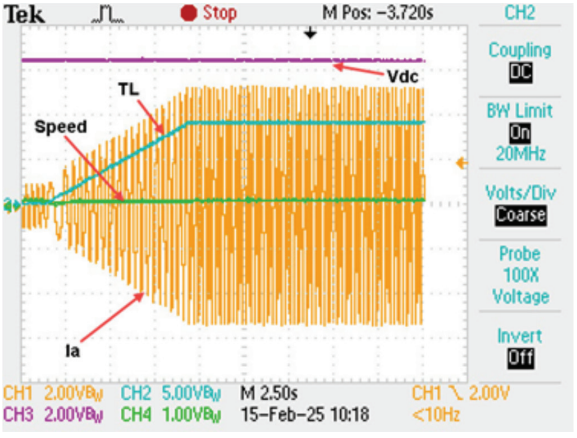

Figure 14. Load increase from 0 to 900 N·m. CH1 (orange) T_L, CH2 (Cyan) T_e, CH3 (Purple) V_{dc}, CH4 (Green) Speed. (Scale voltage: 100 V or Ampere per 1 V DAC). DAC, digital to analogue converter.

To evaluate the dynamic responsiveness of the motor controller, a load torque step response test was implemented. While typical operational scenarios involve gradual load torque variations, a step response provides a more rigorous assessment of the controller's dynamic performance to react to sudden changes. The test involved an abrupt transition in load torque (T_L), changing from −100 N·m (equivalent to a power draw of 12 kW) to −500 N·m (equivalent to a power draw of 73 kW). This deliberate application of a significant load torque disturbance was designed to reveal the system's dynamic behaviour under stress. Figure 15 illustrates the transient response of the

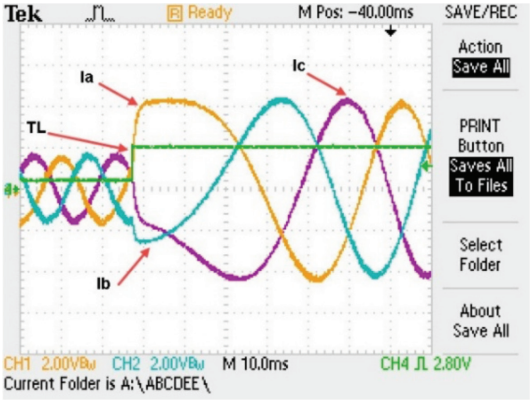

Figure 15. Load torque step from 100 to 500 N·m. CH1 (orange) I_a, CH2 (Cyan) I_b, CH3 (Purple) I_c, CH4 (Green) T_L. (Scale voltage: 100 V or Ampere per 1 V DAC). DAC, digital to analogue converter.

load torque (T_L) and stator currents (I_{abc}) during this event. Furthermore, Figure 16 presents a broader view of the system's response, displaying the DC link voltage (V_{dc}), phase voltage (V_{an}), load torque (T_L), and electromagnetic torque (T_e) as a function of time. Analysis of Figure 16 reveals a step response time of 3.6 ms, defined as the time required for the electromagnetic torque (T_e) to reach its final value (−500 N·m) following the load torque step change. This metric provides a quantitative measure of the controller's ability to track the torque setpoint in response to a sudden disturbance. The zoomed-in view shown in Figure 16 corresponds to a magnified section of the same experimental data, included to highlight the transient behaviour immediately after the load torque step.

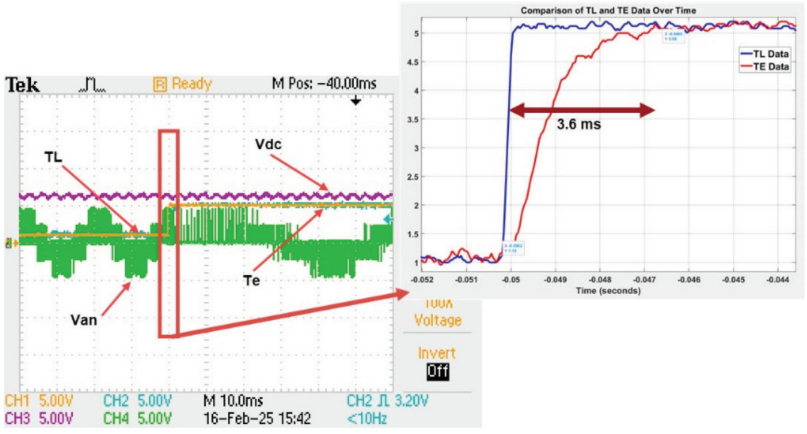

Figure 16. Load increase from 100 to 500 N·m. CH1 (orange) T_L, CH2 (Cyan) T_e, CH3 (Purple) V_{dc}, CH4 (Green) Speed. (Scale voltage: 100 V or Ampere per 1 V DAC). DAC, digital to analogue converter.

5.4. On-load speed variation

Variable frequency drives must adjust rotor speed under all conditions. As seen in Figure 17, with a −500 N·m (73 kW) load torque, a large speed set-point change from 10 rad/s to 157 rad/s is applied, followed by a reverse step change back to 10 rad/s. The results show no variation in DC link voltage or electromagnetic torque during these transitions. This demonstrates the system's robustness in maintaining functionality and stability during significant speed variations under high load.

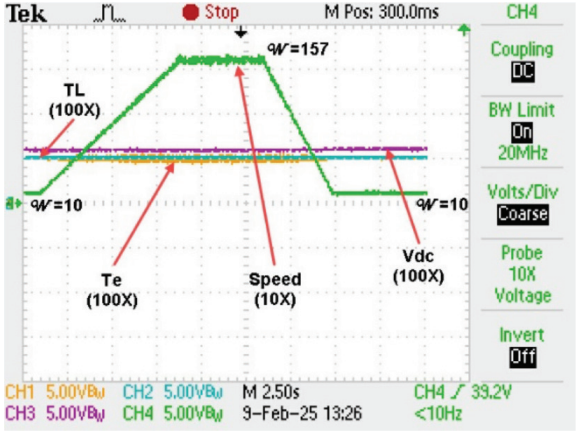

Figure 17. Speed profile from 10 rad/s to 157 rad/s before decreasing back to 10 rad/s, all under 500 N·m load CH1 (orange) T_L, CH2 (Cyan) T_e, CH3 (Purple) V_{dc}, CH4 (Green-Probe 10X) Speed (rad/s). (Scale voltage: 100 V or Ampere per 1 V DAC on O-scope Probe 100X). DAC, digital to analogue converter.

5.5. Ideal and non-ideal switches and dead time in inverter

As described in Section III, the inverter model offers the flexibility to choose between non-ideal switches (IGBTs) and ideal switches for the three-phase two-level inverter. Figure 18 illustrates the differences in phase voltages

when non-ideal switches are employed (in absence of snubber), revealing voltage spikes caused by the inductance inherent in the non-ideal switch model. In real-world applications, such spikes, resulting from switching transients, are typically addressed using snubber circuits. The appearance of these spikes in the simulation emphasises the necessity of incorporating real-world non-idealities into the design and analysis of power electronic systems to ensure accurate modelling and reliable performance.

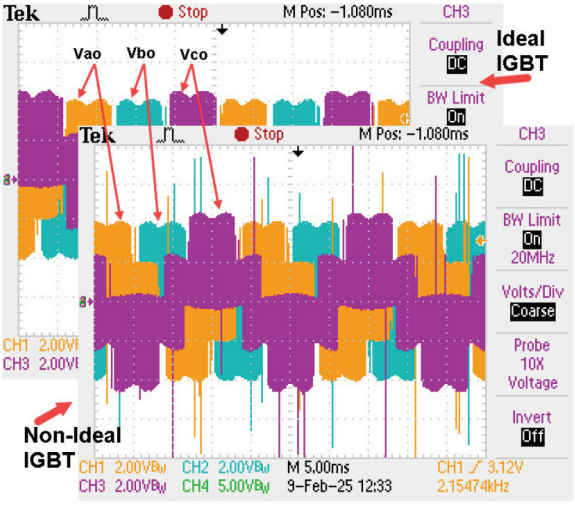

Figure 18. Ideal and non-ideal switches in inverter. CH1 (orange) V_{ao}, CH2 (Cyan) V_{bo}, CH3 (Purple) V_{co}. (Scale voltage: 100 V or Ampere per 1 V DAC). DAC, digital to analogue converter.

As illustrated in Figure 19 and detailed in section III, the control platform implements a programmable dead-time adjustment mechanism. The dead-time interval for the power switches is digitally tunable via firmware, operating within a 20 MHz control-loop clock. Adjustments are made in discrete steps of 50 ns, enabling precise synchronisation of the complementary gate signals. Capable of sub-microsecond simulation steps akin to established commercial HIL solutions (Typhoon HIL 602+), the custom-developed HIL system successfully detects and distinguishes these fine-grained timing variations. This allows the precise dead-time behaviour to be accounted for within the converter model, facilitating control optimisation and ensuring robust shoot-through protection.

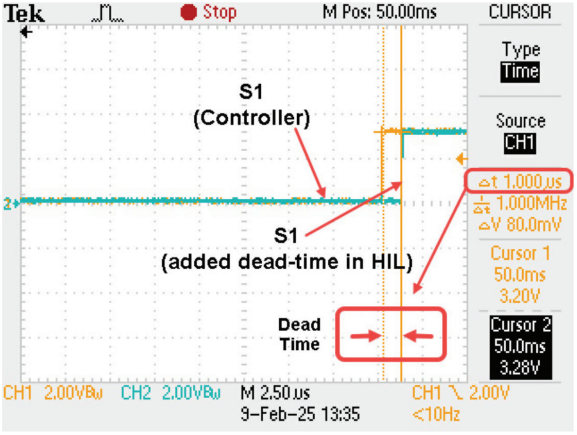

Figure 19. Dead-time parameter in inverter's switches. CH1 (orange) *S*_(1_Controller), CH2 (Cyan) *S*_(1_Controller + deadtime),. (Scale voltage: 2 V digital input 3.3 V_{dc}).

5.6. Rotary encoder performance

Figure 20 shows the simulated rotary encoder's *A* and *B* signals at four speeds, captured via oscilloscope and processed in MATLAB. The square wave frequencies range from 3.25 kHz (95 RPM) to 51.2 kHz (1500 RPM).

These 40 MHz FPGA-generated signals, as described in Section III, provide real-time rotor speed feedback to the control board, ensuring accurate speed control.

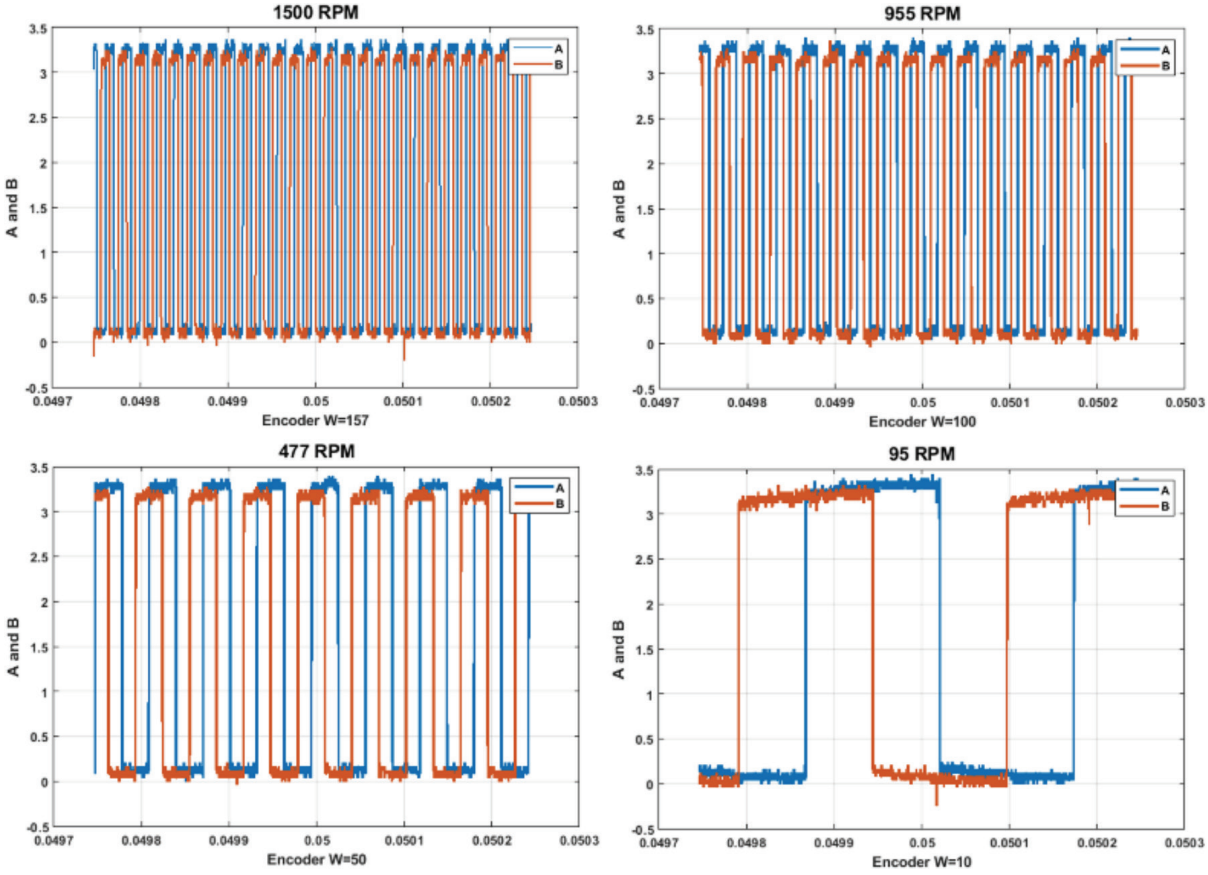

Figure 20. *A* and *B* signal of simulated rotary encoder. CH1 (orange) *A*, CH2 (Cyan) *B*. (Scale voltage: 100 V or Ampere per 1 V DAC). DAC, digital to analogue converter.

5.7. Controller switching frequency *vs* HIL time step

Table 4 provides a quantitative evaluation of the PI current controller's tuning fidelity and the HIL system's operational robustness across a range of time steps and switching frequency provided by the controller. This includes the unprecedented minimum of 100 ns time step achieved in this study for machine and converter modelling. This analysis is based on the mean absolute error (MAE) and root mean square error (RMSE) between the commanded references ($i_{qs}^{*e} = 200$ A, $i_{ds}^{*e} = 70$ A) and measured currents references (i_{qs}^{i} and, i_{ds}^{i}) defined by Eqs (34) and (35) for inner PI controller of the stator current.

To assess the impact of adopting a uniform time step across all subsystems, the effect of increasing the simulation time step is evaluated in Table 4. The results show that increasing the time step leads to significant degradation in current tracking accuracy and, in some cases, numerical instability. This indicates that a constant time-step approach either requires an extremely small time step for all subsystems—resulting in excessive computational burden—or leads to unacceptable accuracy loss. In contrast, the proposed multi-rate architecture enables higher accuracy while maintaining computational efficiency.

$$MAE = \frac{1}{n}\sum_{i=t}^{n}\left|I_{dqs}^{i} - I_{dqs}^{*e}\right| n = 200{,}000 \ (n * T_s = 20 \text{ ms}) \tag{34}$$

$$RMSE = \sqrt{\frac{1}{n}\sum_{i=t}^{n}\left(I_{dqs}^{i} - I_{dqs}^{*e}\right)^2} \tag{35}$$

Table 4. Impact of time step and switching frequency on stator current error calculation.

HIL system time step (T_s)	Switching frequency (sbRIO9629 Controller)				
	Error type	5.7 kHz	50 kHz	100 kHz	200 kHz
100 ns	MAE, I_d	8.1	2.3	2.1	1.5
	MAE, I_q	3.2	2.8	2.2	2.0
	RMSE, I_d	0.27	0.09	0.08	0.04
	RMSE, I_q	0.15	0.09	0.07	0.05
2 μs	MAE, I_d	10.1	7.4	5.2	3.8
	MAE, I_q	5.3	4.3	3.8	3.1
	RMSE, I_d	0.35	0.15	0.09	0.08
	RMSE, I_q	0.29	0.16	0.12	0.1
5 μs	MAE, I_d	14.3	16.4	14.6	14.6
	MAE, I_q	8.2	15.9	15.6	15.3
	RMSE, I_d	0.35	0.46	0.4	0.35
	RMSE, I_q	0.29	0.54	0.52	0.46
10 μs	MAE, I_d	25.4	70.3	N.M.C	N.M.C
	MAE, I_q	18.4	90.6	N.M.C	N.M.C
	RMSE, I_d	0.98	1.21	N.M.C	N.M.C
	RMSE, I_q	0.95	1.25	N.M.C	N.M.C

$I_q^* = 200$ A, $I_d^* = 70$ A, Speed = 500 RPM.

MAE, mean absolute error; N.M.C, no mathematical conversions; RMSE, root mean square error.

6. Performance Comparison with Typhoon Hil

This section presents a comparative evaluation between the proposed custom HIL system and the commercial Typhoon HIL 602+ platform. The objective is not to demonstrate superior performance, but to validate the proposed methodology against a well-established and widely used commercial solution, serving as a reference benchmark. To ensure a fair comparison, both systems were tested under identical operating conditions, including the same control parameters, system model, and control hardware. The results show a close agreement between both platforms in terms of dynamic response, current waveforms, and THD, confirming that the proposed implementation accurately reproduces the behaviour of a validated commercial HIL system.

This agreement demonstrates the validity of the proposed approach. In addition, the proposed custom HIL system achieves a smaller simulation time step (100 ns) compared to the 500 ns used in the Typhoon HIL platform, while maintaining comparable accuracy. Furthermore, this is achieved with a significantly lower system cost, supporting the practical viability of the proposed solution.

As shown in Table 5, the total harmonic distortion (THD) of the stator current at a load torque of 500 N·m exhibits close agreement between the two systems, with only a marginal difference (≈0.1%), indicating high model fidelity. The hardware interface configuration used for this comparison is illustrated in Figure 21.

Table 5. Stator Current (I_{abc}) THD for NI custom and Typhoon HIL systems

THD Calculation (Tektronix O-Scope)	THD	THD (dB)	THD (%)
Custom HIL (PCIe7857r)	0.0351	−29.0909	3.5112
Typhoon HIL (602+)	0.0343	−29.2910	3.4312

HIL, hardware-in-the-loop; THD, total harmonic distortion.

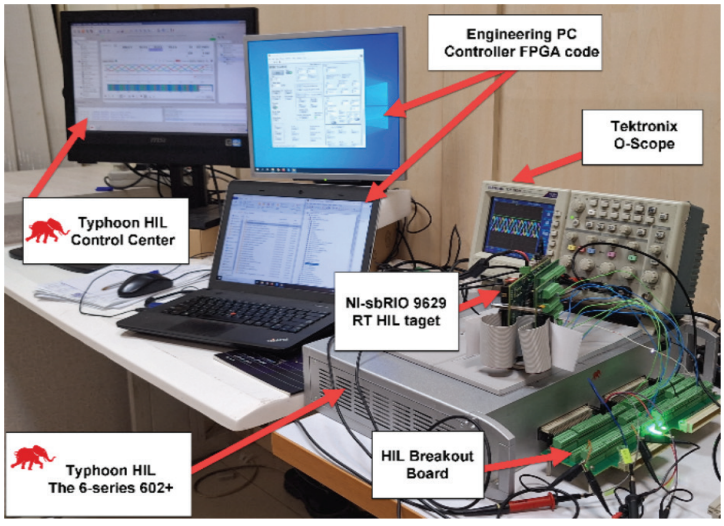

Figure 21. The Typhoon 6-series HIL 602+ setup. HIL, hardware-in-the-loop.

To ensure consistency, identical test conditions were maintained across both platforms. Minor modelling differences, such as the inclusion of snubber circuits, were identified and taken into account in the analysis.

6.1. Load torque step response

To compare performance, a step-change in load torque from −100 N•m to −500 N•m was applied to the Typhoon HIL 602+ machine load settings. Figure 22 displays the resulting stator current, speed, and electromagnetic torque responses. When compared to the proposed HIL system's response (Figure 23), the behaviour of both systems is remarkably similar, showing minimal differences. While both systems utilised the same control board and parameters, minor deviations are expected. These arise from inherent differences in model implementation details (due to confidentiality restrictions on the Typhoon system), solver algorithms used by the Typhoon HIL 602+, and variations in analogue input properties and calibrations. Consequently, two distinct interfaces and calibrations were necessary, introducing potential calibration errors in voltage and current feedback. Despite these factors, the results demonstrate a high degree of correlation between the two HIL systems.

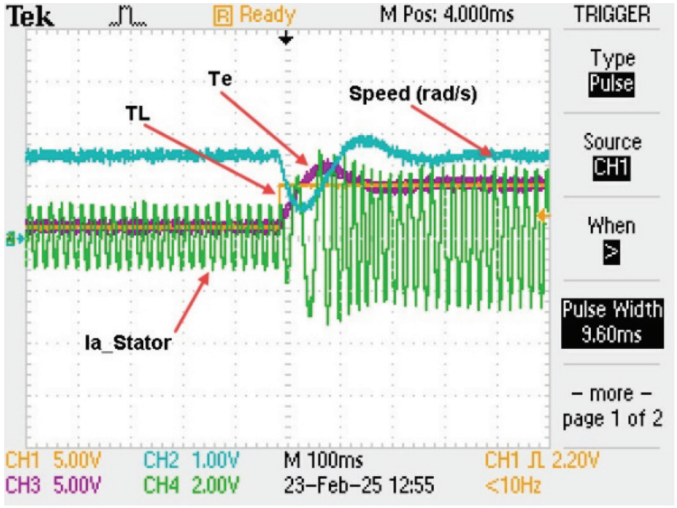

Figure 22. Torque load jump from −100 N•m to −500 N•m. CH1 (orange) T_L, CH2 (Cyan) Speed, CH3 (Purple) T_e and CH4 (Green) I_a. (Scale voltage: 100 V or Ampere per 1 V DAC). DAC, digital to analogue converter.

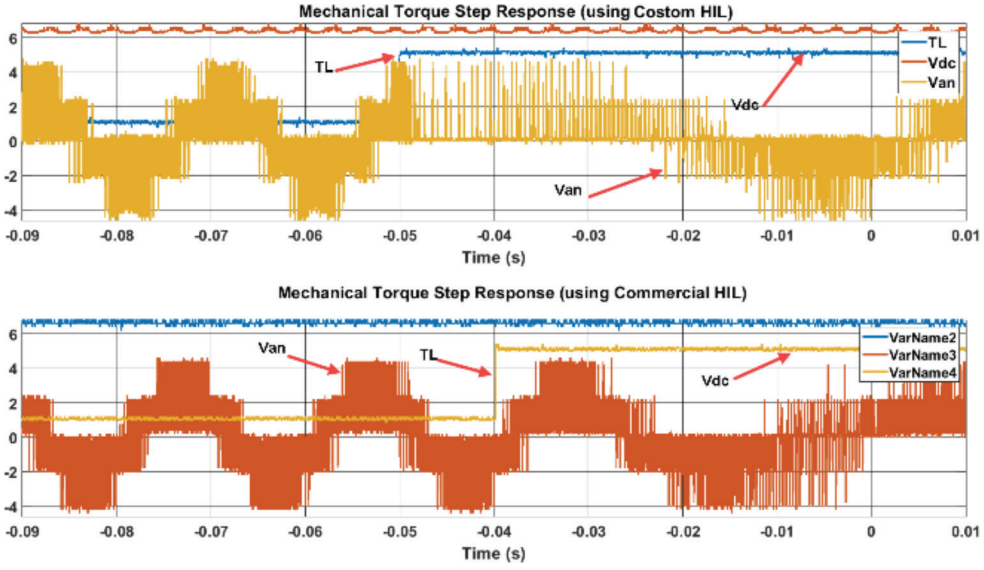

Figure 23. Torque step response comparison test between NI custom made and Typhoon HIL. HIL, hardware-in-the-loop.

6.2. Speed variation in constant load torque

A rigorous comparative analysis was undertaken to validate the performance of the developed custom NI HIL system against the established industry-standard Typhoon HIL platform. This analysis focused on assessing the systems' ability to handle dynamic speed variations with dissimilar user-defined setpoint changes under a consistent load. To this end, both systems were subjected to a speed ramp test, simulating a smooth acceleration from 10 rad/s (95 RPM) to 157 rad/s (1500 RPM) and a subsequent deceleration back to 10 rad/s, while maintaining a constant load torque of −500 N·m. This test was designed to evaluate the effectiveness of the IFOC drives in managing speed changes under a significant load. As evidenced in Figure 24, the NI HIL system exhibited a performance profile that

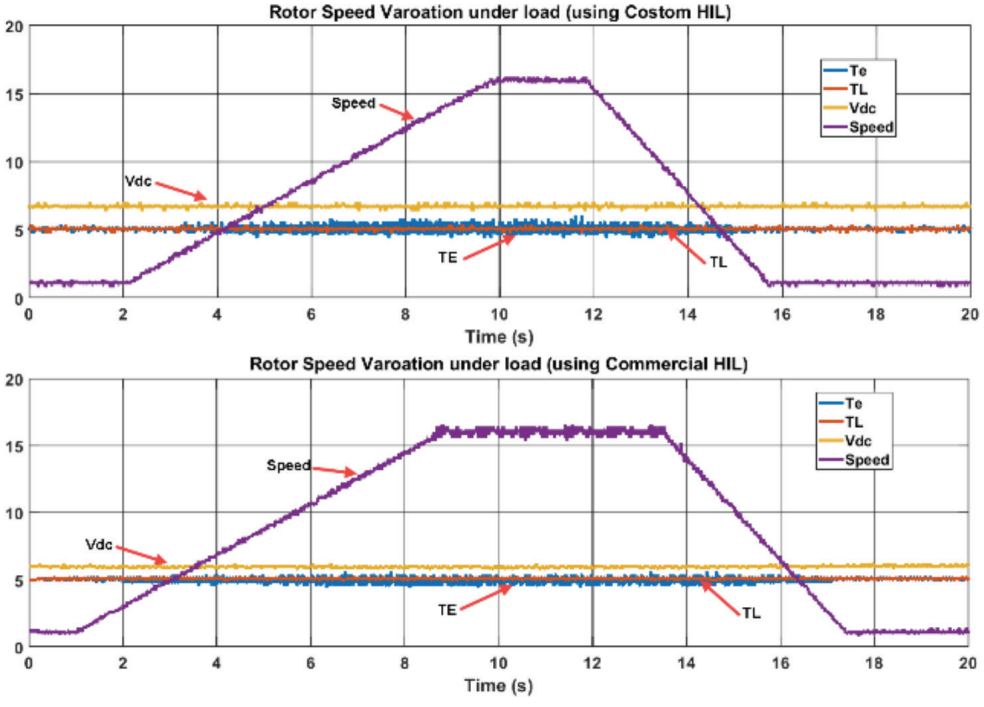

Figure 24. Speed variation 95 RPM to 1500 RPM then 95 RPM under −500 N·m mechanical Torque. CH1 (Blue) T_e, CH2 (Red) T_L, CH3 (Yellow) V_{dc} and CH4 (Purple) Speed. (Scale voltage: 100 V or Ampere per 1 V for Chanel one to three and DAC and 50 V per 1 V for CH4). DAC, digital to analogue converter.

closely mirrored that of the Typhoon HIL. Both systems demonstrated consistent and stable operation throughout the entire speed variation cycle, despite dissimilar user-defined setpoint changes, confirming the robust design and implementation of the custom NI HIL system.

7. Conclusions

This study successfully presented and validated a custom-designed, FPGA-based real-time HIL emulator and its variable time step sub-microsecond controller tailored for power electronics applications, specifically the dynamic analysis of a complex industrial variable frequency drive and potential application areas such as GaN/SiC converter development and EV motor drives. A key innovation of this work is the minimisation of the simulation time step to an unprecedented 100 ns for the core power electronic components. This achievement effectively mitigated aliasing issues and eliminated the need for complex oversampling algorithms to address steady-state oscillations, a significant advantage over conventional approaches. The emulator's flexibility and integration within standard engineering software further offer a cost-effective and highly customisable alternative to commercial HIL systems, empowering scientists with enhanced control over model fidelity and hardware selection.

Furthermore, the significantly reduced time step enabled accurate and stable emulation of the high-frequency switching dynamics inherent in modern power semiconductor devices, facilitating detailed investigation of crucial phenomena such as voltage spikes across switches and transient current ripple that contribute to pulsating currents. This capability positions the developed custom HIL emulator as a valuable and efficient tool for the design, testing, and optimisation of advanced power electronic systems and their control strategies, ultimately contributing to enhanced system performance, reliability, and faster design cycles in engineering practice by directly addressing critical simulation challenges. Future work will focus on extending the model fidelity by incorporating additional non-ideal effects, such as switching delays and more detailed device characteristics, as well as exploring the impact of measurement-related disturbances within the HIL framework.

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