

Optimisation of the Synchronous Rectifier in Phase Shift Full Bridge Converters for High-Frequency Applications

Research paper

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Abstract: Efforts to minimise the size and material usage of power converters are reflected in efforts to increase the switching frequency. The problem is that semiconductor switching losses are proportional to the switching frequency, so it is necessary to find ways to keep efficiency high at higher switching frequencies. Gallium nitride (GaN) transistors have made it possible to improve the parameters of many topologies due to a better figure of merit (FOM). Thanks to GaN technology, it is possible to increase the soft switching range in the inverter of phase-shift full-bridge (PSFB) converter and thus reduce switching losses. This paper addresses the selection of semiconductor transistors for a synchronous rectifier (SR) operating at 500 kHz. Based on mathematical calculations and simulation results in the programme PLECS, the converter was designed and measured under laboratory conditions. The paper highlights the advantages and challenges of using GaN transistors in SRs, which, when properly applied, enable lower losses and thus higher efficiency at a switching frequency of 500 kHz.

Keywords: PSFB converter • high-frequency synchronous rectifier • low voltage GaN transistor • active clamp

1. Introduction

The phase-shift full-bridge (PSFB) converter is widely used because it allows a large conversion ratio, galvanic isolation, achieves high efficiency while containing few components, and regulation is simple by changing the phase shift in the inverter legs at a constant frequency (Chothe et al., 2021; Texas Instruments, 2014). In addition to the advantages, there are also disadvantages. First, there is the circulating current that flows through the transformer and semiconductors when the voltage on the secondary side of the transformer is zero, that is, no power is transmitted but losses are caused; furthermore, the zero voltage switching (ZVS) of the primary transistors is dependent on the load and, last but not least, overvoltage occurs on the secondary semiconductors due to resonance between the stray inductance of the transformer and the output capacitance of the transistors of the synchronous rectifier (SR) (Dudrik et al., 2018; Pastor et al., 2023; Yu et al., 2023). Another challenge is the placement of the sensor and the evaluation of current measurement when using the peak current mode control (PCMC) technique at high switching frequencies (Yu et al., 2024).

With gallium nitride (GaN) or SiC transistors, it is possible to effectively address the inverter's circulating-current problem and achieve ZVS at lower loads. These transistors have a better ratio of series resistance to output capacitance, which affects the ZVS, so that ZVS can be achieved at a lower current. Typically, the converter is designed to achieve ZVS from a load of 50%; however, even if ZVS cannot be achieved at loads of up to 50% for the leading leg, the losses are reduced compared with IGBT or Si transistors, thanks to better switching characteristics, which is also the reason why high efficiency can be achieved even with circulating current. Due to this, it is possible to remove the additional snubbers that solved these problems, especially when using IGBT transistors, which is

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beneficial in increasing the frequency and power density thanks to the reduction of parasitic elements (Beheshti, 2020; Cui et al., 2014; Qi et al., 2019).

The third main disadvantage affecting the efficiency of the PSFB converter is the occurrence of overvoltage oscillation on the secondary side, due to the resonance between the leakage inductance of the transformer and the output capacitance of the switching component. Overvoltage is especially problematic when using an SR because it requires transistors to operate at higher voltages, which increases total losses. The magnitude of the overvoltage depends on the type of rectifier used, but it is still several times higher than the output voltage of the converter. The situation becomes significantly more complicated in the event of transient phenomena, when negative inductance current can cause an increase in the overvoltage, exceeding the maximum voltage of the SR transistors. One way in which to prevent the overvoltage in transients, as suggested by Escudero et al. (2020), is to ensure correct timing of transistor switching. In addition, there are other methods, in particular the lossy RCD snubbers (Renesas, 2018) and the lossless active clamp (AC) (Qi et al., 2019), formed by a transistor and a capacitor that allows for better efficiency than RCD, but requires the MCU to control an additional transistor, which puts further demands on the control system and reduces the power density. The question is how advantageous it is to use AC at very high frequencies, where it may not appear to be lossless.

In addition to these conventional approaches, alternative methods exist. In the work by Chen et al. (2012), an LC network is connected between the node of the lagging leg and the minus pole of the input source, which suppresses the overvoltage and, in addition, helps achieve ZVS of the primary transistors. Park et al. (2007) suppress overvoltage by series connection of a capacitor to the transformer's secondary winding. This solution is especially advantageous for higher output voltages and lower currents because the capacitor must be able to handle the current of the secondary winding. Yet, it is a simple solution that is practically lossless and requires no additional control. Several additional snubbers for a current doubler type rectifier are presented and compared by Mao et al. (2003).

Another problem is the effort to measure current and apply PCMC, which has certain advantages over voltage control, especially in automatic short-circuit protection and the prevention of DC current in the transformer. In the past, it was typical to measure current using a current transformer (Yu et al., 2024) in a DC power supply of an inverter, but resetting the transformer at high frequencies is a challenge.

This paper describes the possibilities and challenges of applying low-voltage GaN transistors in SR with the aim of improving the overall characteristics of a PSFB converter operating at a frequency of 500 kHz.

2. PSFB Converter with SR

Nowadays, even with large output currents, there is a tendency to use an SR, even if several transistors need to be connected in parallel. Typically, three types of rectifiers are used: current-doubler (CD) rectifier, centre-tapped (CT) rectifier and full-bridge (FB) rectifier (Yu et al., 2024). The FB and CD rectifiers require a simpler transformer compared with the CT, which needs a centre winding. The CD and CT require only two transistors, which is advantageous, especially when operating with large output currents. FB and CT rectifiers work with only one output inductance. The FB rectifier has the advantage of being stressed at half the voltage compared with CD and CT, so it is more often used at higher output voltages and lower currents. The CD offers ripple current cancellation, because the frequency of the output current is doubled due to two inductances, which makes it possible to significantly reduce the capacitance of the output filter (Mappus, 2004). For larger currents, a CT or CD rectifier is typically used. Alou et al. (2006) suggest that for output currents of up to 15 A, a CT is preferable, while for currents above 25 A, a CD is recommended, depending on the specific application. The great advantage of CD for high currents is the balanced thermal distribution between the transformer's secondary winding and the two filter inductances (Yu et al., 2024). All the above-mentioned types of rectifiers are stressed by overvoltage oscillations.

For the converter studied in this paper, whose parameters are listed in Table 1, a CD rectifier was selected. The schematic diagram of the PSFB converter with CD SR is shown in Figure 1.

2.1. Overvoltage oscillation on the secondary side

The overvoltage oscillation in the PSFB converter with a CD rectifier (Figure 1) is explained; however, it is similar across all three types. The waveform in Figure 2 is generated by a simulation in the programme PLECS for a given converter, at a load current of 50%. In Figure 2, the first two waveforms show the logic level of transistors T_1 – T_4 , each switching a half-period excluding the dead time (t_d), which is set to 100 ns. The third trace shows the primary current I_p , the fourth the inductance current I_{L_2} and the last the voltage on the transistor V_{DS_TSR1} .

Table 1. Parameters of the PSFB with CD rectifier.

Parameter	Value
Input voltage (V_{IN})	390 V
Output voltage (V_{OUT})	24 V
Output current (I_{OUT})	25 A
Frequency (f)	500 kHz
Transformer ratio (p)	6
Leakage inductance (L_k)	3.5 μ H
Filter inductance (L_1 and L_2)	22 μ H
Output capacitance (C_{OUT})	15 μ F

CD, current-doubler; PSFB, phase-shift full-bridge.

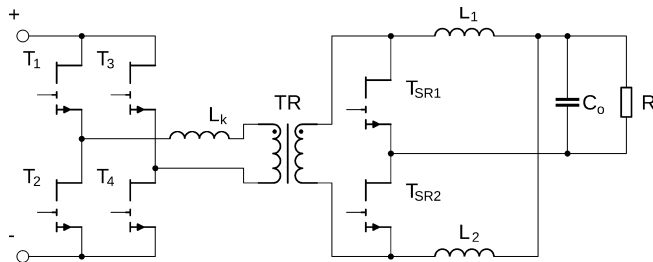


Figure 1. Schematic of PSFB converter with CD SR. CD, current-doubler; PSFB, phase-shift full-bridge; SR, synchronous rectifier.

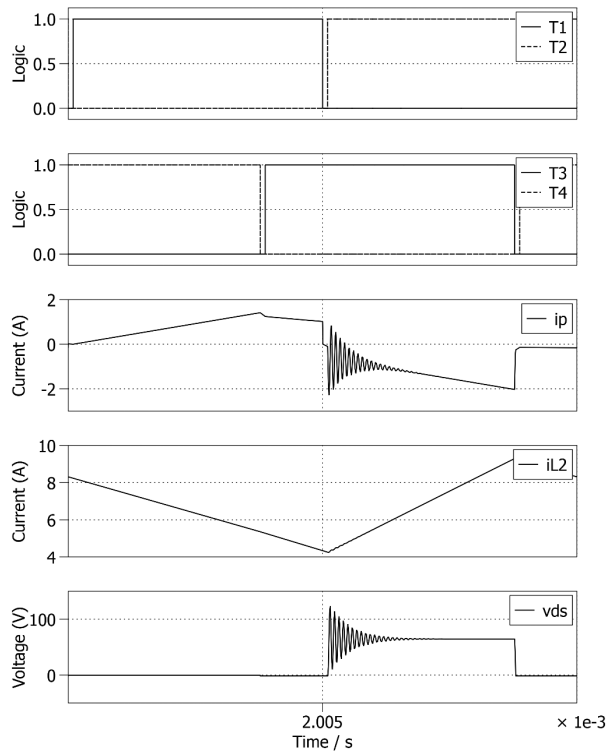


Figure 2. Simulation waveform of overvoltage occurrence on T_{SR1} .

When transistor T_2 is turned on while transistor T_3 is turned on, the direction of the primary current I_p changes. After I_p reaches the value of the current in the filtering inductance (through the transformer ratio), the built-in diode of transistor T_{SR1} is turned off, and the current commutates to the T_{SR2} . In a moment, the resonance of the leakage inductance L_k with the output capacitance of the C_{oss} transistor T_{SR1} occurs, causing an overvoltage oscillation. The overvoltage magnitude in the simulation reached approximately 121 V, while the converter operated at a nominal output voltage of 24 V. An equation describing the magnitude of the overvoltage of the secondary side transistor is given by Park et al. (2007) and Ruan and Zhang (2015):

$$V_{DSTR1(\text{peak})} = \frac{2V_{IN}}{p}, \quad (1)$$

where p is the transformer ratio. Substituting into Eq. (1), we get that the peak overvoltage is 130 V. This value is lower in the simulation because the simulation uses real transistor models, which include resistive elements that influence the resulting overvoltage. The equation assumes ideal capacitive and inductive components, which is why the value is 130 V in the equation and 121 V in the simulation.

However, the peak value of overvoltage is independent of the values of capacitance and inductance, which affect the resonant frequency:

$$\omega_r = \frac{1}{\sqrt{L_k C_{(oss)TSR}}}, \quad (2)$$

where $C_{(oss)TSR}$ is the output capacitance calculated to the primary side. SR transistors in the converter are generally rated for this overvoltage value; however, this is not an optimal condition because this value is many times higher than the 24 V output voltage. Furthermore, if reverse current flows in the filter inductors, the overvoltage value will increase even further. The application of an additional circuit will limit the resulting overvoltage to a certain defined value, which will not be exceeded even during transient events. In addition, another way to limit overvoltage is through the proper timing of transistor switching, as described by Escudero et al. (2020). This approach does not require an additional circuit, which can cause further losses, especially at higher frequencies.

2.2. Semiconductor selection for SR

The aim of selecting SR transistors is to minimise drain to source resistance R_{Dson} of the transistors, that is, to minimise conduction losses, while the transistors must be able to withstand the voltage stress defined in the previous subchapter. Two Si and two GaN transistors with low R_{Dson} were selected for comparison, 100 V for use with AC and 150 V for use without an additional circuit. Parameters of the transistors are shown in Table 2.

The total losses (P_{total}) incurred by SR transistors primarily comprise three parts: conduction losses (P_{con}), switching losses (P_{oss}) and driving losses (P_{gate}) Sam (2013):

Table 2. Parameters of selected transistors.

	IPTG014-N10NM5	IPTG025-N15NM6	EPC2302	EPC2305
Technology	Si	Si	GaN HEMT	GaN HEMT
Manuf.	Infineon	Infineon	EPC	EPC
V_{DS} (V)	100	150	100	150
I_D (A)	366	264	133	133
R_{Dson} (m Ω)	1.4	2.5	1.8	2.2
Q_{oss} (nC)	214	310	85	103
Q_g (nC)	169	105	23	22
$R_{Dson}Q_{oss}$	299.6	775	153	226.6
$R_{Dson}Q_g$	236.6	262.5	41.4	48.4
Footprint area (mm ²)	120	120	15	15

GaN, gallium nitride.

$$P_{\text{total}} = P_{\text{con}} + P_{\text{oss}} + P_{\text{gate}}, \quad (3)$$

$$P_{\text{con}} = R_{\text{DSon}} I_{\text{DS(RMS)}}^2, \quad (4)$$

$$P_{\text{oss}} = 0.5 Q_{\text{oss}} \frac{V_o}{ph_{\text{eff}}} f, \quad (5)$$

$$P_{\text{gate}} = V_g Q_g f, \quad (6)$$

where Q_{oss} is the output charge, Q_g is the gate charge, V_o is the output voltage, V_g is the gate driver voltage, f is the switching frequency, ph_{eff} is the effective duty cycle and I_{ds} is the effective value of the transistor current:

$$I_{\text{DS(RMS)}} = I_o \sqrt{\frac{ph_{\text{eff}}}{2} + \frac{1}{4}}, \quad (7)$$

where I_o is the load current. The equations show that P_{con} is most affected by R_{DSon} , P_{oss} by output charge Q_{oss} , and P_{gate} by gate charge Q_g . Thanks to the fact that GaN technology (Table 2) has a significantly better ratio between parasitic capacitance and R_{DSon} ($R_{\text{DSon}} Q_{\text{oss}}$ or $R_{\text{DSon}} Q_g$), parameters such as Q_{oss} and Q_g are also significantly lower, which results in minimised switching and driving losses; the calculated losses for 100% load are shown in Table 3, while Figure 3 shows the losses when changing the load from 0% to 100%.

As we can see from the results, the low parasitic capacitance of GaN technology makes it possible to achieve low switching losses at high frequencies compared with Si, however, in addition to these, further losses are caused from the reverse conduction because the transistor turns on shortly after current begins to flow through the reverse conduction and turns off just before the current drops to zero, in order to achieve ZVS. These losses are tried to be minimised by shortening the reverse conduction time, especially for GaN transistor, where voltage drop in the

Table 3. Transistors losses at 100% load.

	IPTG014-N10NM5	IPTG025-N15NM6	EPC2302	EPC2305
P_{con} (W)	0.22	0.39	0.28	0.34
P_{oss} (W)	3.38	4.89	1.34	1.63
P_{gate} (W)	1.27	0.79	0.17	0.17
P_{total} (W)	4.86	6.07	1.79	2.13

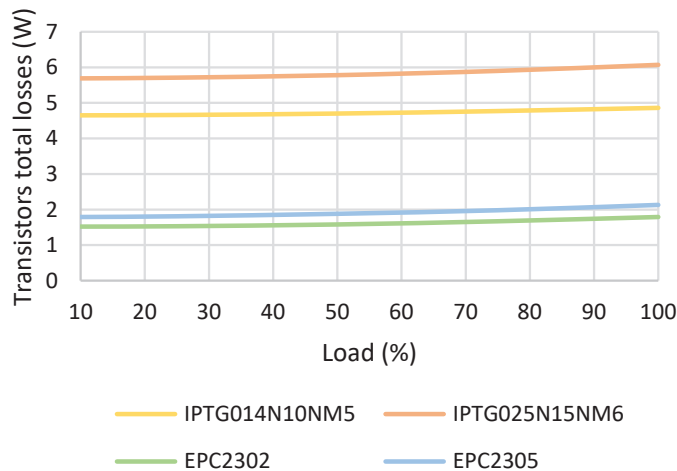


Figure 3. Calculated losses of SR transistors. SR, synchronous rectifier.

reverse direction V_R is two to three times higher compared with Si MOSFETs body diode. The reason is that the reverse conduction of GaN transistors operates on a different principle GaN Systems (2016):

$$V_R = V_{TH(GD)} + V_{GS(off)} + I_{SD}R_{DS(on)}, \quad (8)$$

where $V_{TH(GD)}$ is the threshold voltage value, $V_{GS(OFF)}$ is the value of the voltage at the gate of the transistor in the off state and I_{SD} is the value of the current in the reverse direction. Hence, the challenge of control is to control the timing so that the transistor reaches ZVS by reverse conduction, but to minimise the time to the minimum necessary.

The mathematical calculation of losses was verified by simulation in the PLECS (Figure 4), using models downloaded from the official EPC website. Compared with the calculated losses (Figure 4), it can be seen that the losses are a little higher; nevertheless, simulation showed that the difference between the GaN transistor at 100 V and 150 V is not very significant, for this reason, the EPC2305 transistor was selected for laboratory measurements.

2.3. SR switching modes

Switching of SR transistors can be realised in three modes. The first mode (mode 0) is used in a zero or light load operation, in which switching the transistors would cause greater losses than just operating the reverse conduction of the transistors. In a low-load state, when the current in the inductors drops to zero in discontinuous conduction mode (DCM), the transistors must only be turned on during the rise of the current in the filter inductance (mode 1); otherwise, a reverse current could occur in the filter inductances. In the case of medium and high loads, where the current in the filter inductance is still greater than zero and the filter inductance is in continuous conduction mode (CCM), it is important to maximise the time that the transistor is turned on in order to reduce losses from reverse conduction. The duration of transistor turn-on in DCM and CCM is shown in Figure 5. In the waveform, v_p indicates the primary voltage of the transformer, i_p the current of the primary winding of the transformer, i_{L1} and i_{L2} the current of the filter inductors, v_{ds} the voltage between the drain and source of transistor T_{SR1} , i_{ds} is the current of this transistor and v_{gs} indicates the logic value of transistor switching.

In CCM and switching mode 2, the ideal turn-on time of the transistor is affected by the magnitude of the output current, because the transistor must be turned off only after voltage appears on the secondary side, which is related to the change in current polarity in the leakage inductance. However, the slope of this change depends on the load current. The possible delay time is shown in Figure 6.

As can be seen from the waveform, in CCM, mode 2 is extended by sections in which it is not possible to define whether the current is positive or negative in the DCM region. The time at which the current drops to zero and changes polarity depends on the size of the load and the value of the filter inductance, that is, the current ripple in the filter inductance. Therefore, it is safer in DCM to keep the transistor turned off in this area. However, this is not an ideal situation, especially for GaN transistors, as their reverse conduction losses are greater than those of Si technology. A possible solution is to add a current sensor to the rectifier, which would ideally turn off the transistor so that the polarity of the current does not change, but this solution complicates the control and requires an additional component, which is worth evaluating. The second advantage of the current sensor is that it automatically solves the problem of transistor switching delay in the CCM region.

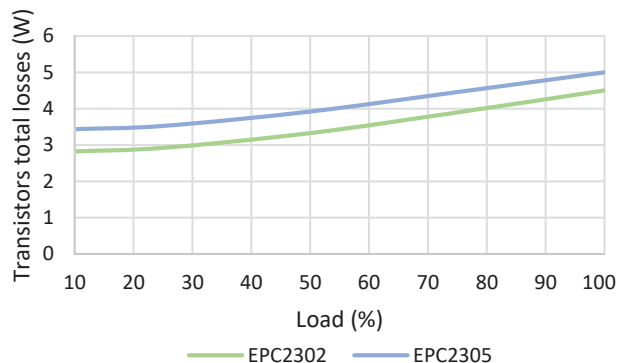


Figure 4. Simulated losses of EPC GaN transistors in PLECS. GaN, gallium nitride.

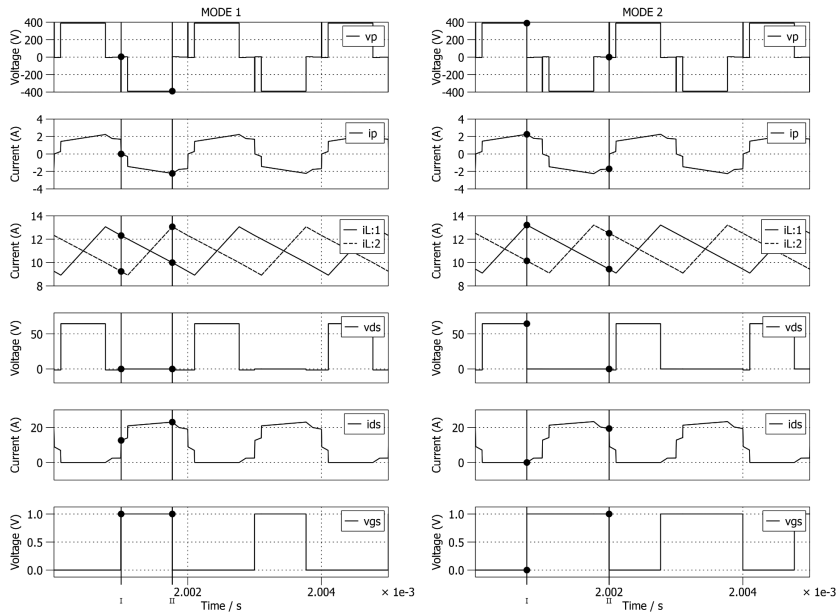


Figure 5. Difference between SR switching in DCM and CCM obtained from PLECS simulation for transistor T_{SR1} . CCM, continuous conduction mode; DCM, discontinuous conduction mode; SR, synchronous rectifier.

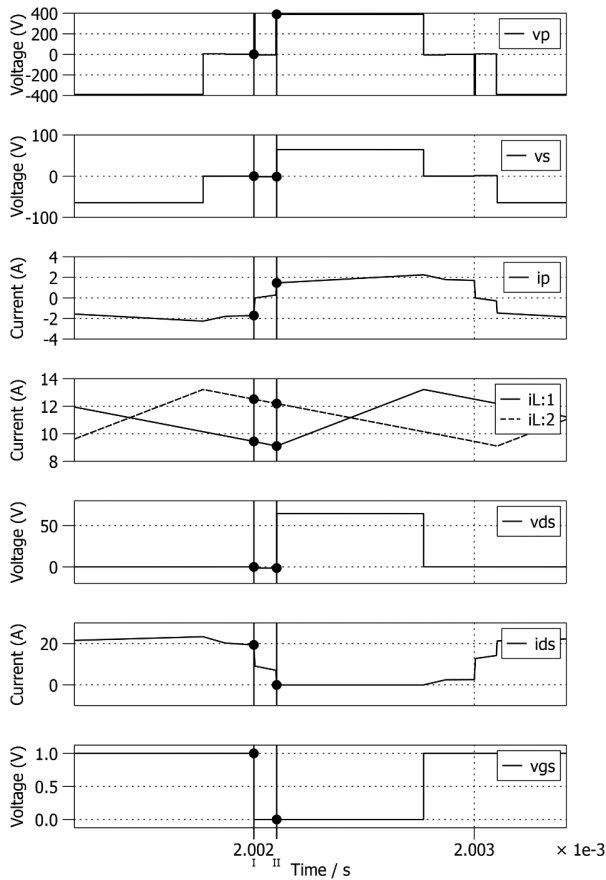


Figure 6. Possible range of delay for mode 2 in CCM. CCM, continuous conduction mode.

2.4. AC design

For a CD rectifier, it is necessary to use two additional networks between the transistor drains and the common negative pole of the secondary side. In this case, a network called an AC is used, that is, a capacitor switched by a transistor (Figure 7). In the design, it is necessary to properly select the capacitor's capacitance, which depends on the transformer ratio, transformer leakage inductance and switching frequency. Eq. (9) is given in the literature (Yu et al., 2023), from which Eq. (10) was derived, which can be used to calculate the capacitor's capacitance. After substitution, we get that the capacitance should be higher than 1.82 μF :

$$T_s \ll 2\pi \sqrt{\left(\frac{N_s}{N_p}\right)^2 L_s C_{AC}} \quad (9)$$

$$C_{AC} \gg \frac{T_s P^2}{4\pi^2 L_s} \quad (10)$$

The principle of the clamp is that, when resonance occurs between the leakage inductance and the output capacitance of the SR transistor, the T_{AC} capacitor charges the C_{AC} capacitor via reverse conduction of the transistor. Subsequently, once the transistor has been turned on, energy is transferred through the filter inductance to the output capacitor C_o . (Yu and Lough 2023).

3. Laboratory Measurements

Based on the previous chapters, a laboratory model of a rectifier for the given converter was designed, operating at a switching frequency of 500 kHz. A photo of the model is shown in Figure 8, and a photo of the set-up, together with the transformer, inverter and control digital signal processor (DSP), is shown in Figure 9. On the left side is the inverter using GS-065-011 GaN transistors, in the middle is the planar transformer designed for 500 kHz, and on the right is the rectifier with GaN transistors and an additional circuit. The PCB of the rectifier is designed to eliminate parasitic elements in the power and driver loop, which can have a negative effect at high switching frequencies. The transistors used have a heat sink on the top side, so they can be easily attached to the passive heatsink. The high switching frequency significantly reduced the size of the LC output filter, and even in the case of filter capacitance, only MLCCs are used, which increases the power density of the converter. The parameters of the laboratory model are shown in Table 4.

Figure 10 shows the primary voltage of the transformer created by the inverter v_p , the primary current i_p , the voltage between the drain and source of transistor v_{DS_TSR1} , and the output voltage v_o , at half output current 12.5 A, half supply voltage 200 V and dead time t_d set to 80 ns. As we can see from the waveform, the output voltage is stable even when the transistor is conducting in reverse. The overvoltage occurring on the transistor is limited by an

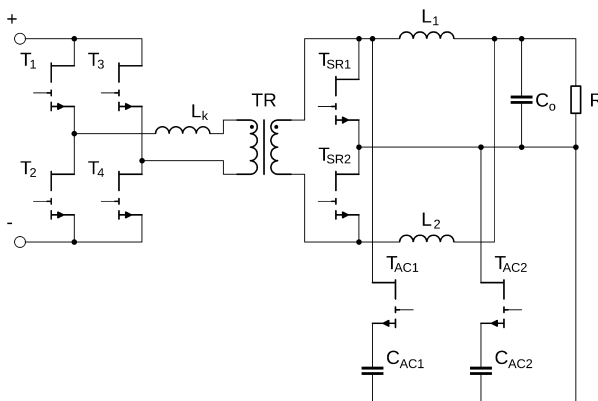


Figure 7. Schematic of PSFB converter with SR and AC. AC, active clamp; PSFB, peak current mode control; SR, synchronous rectifier.

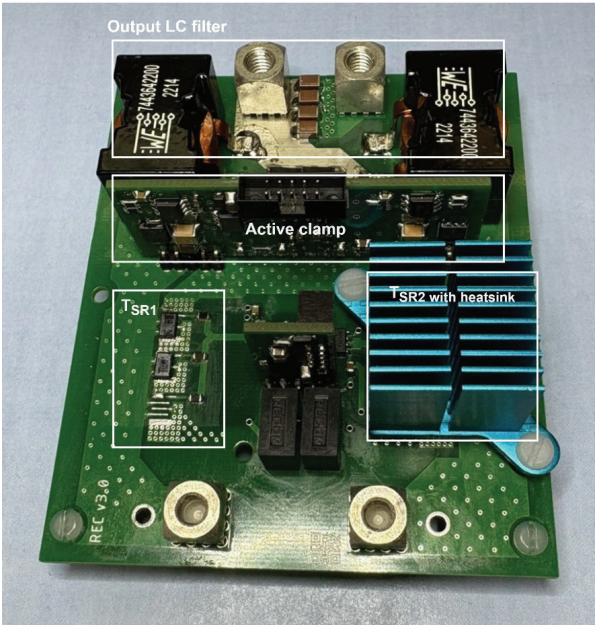


Figure 8. Schematic of PSFB converter with SR and AC. AC, active clamp; PSFB, peak current mode control; SR, synchronous rectifier.

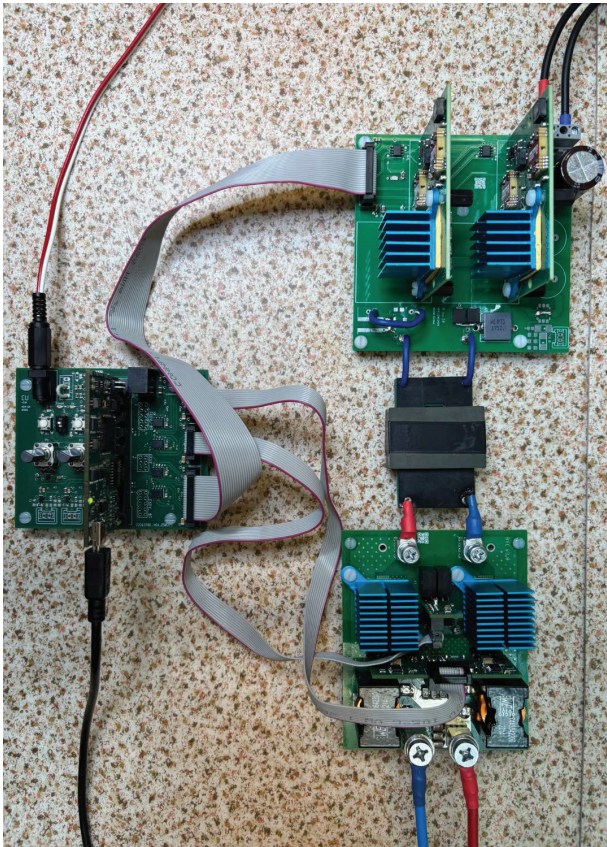


Figure 9. Laboratory set-up. AC, active clamp; DSP, digital signal processor.

Table 4. Parameters of the laboratory model of the PSFB Converter.

Parameter	Value
Input voltage (V_{IN})	390 V (reduced to 195 V during measurements)
Output voltage (V_{OUT})	24 V
Output current (I_{OUT})	25 A
Frequency (f)	500 kHz
Transformer ratio (p)	6
Leakage inductance (L_k)	3.5 μ H
Magnetising inductance	726.9 μ H
Filter inductance (L_1 and L_2)	22 μ H
Output capacitance (C_{OUT})	15 μ F
Inverter transistors (T_1-T_4)	GS-065-011
SR transistors (T_{SR1}, T_{SR2})	EPC 2305
AC transistors (T_{AC1}, T_{AC2})	ISC046N13NM6ATMA1
AC capacitance (C_{AC1}, C_{AC2})	2 μ F

AC, active clamp; PSFB, phase-shift full-bridge; SR, synchronous rectifier.

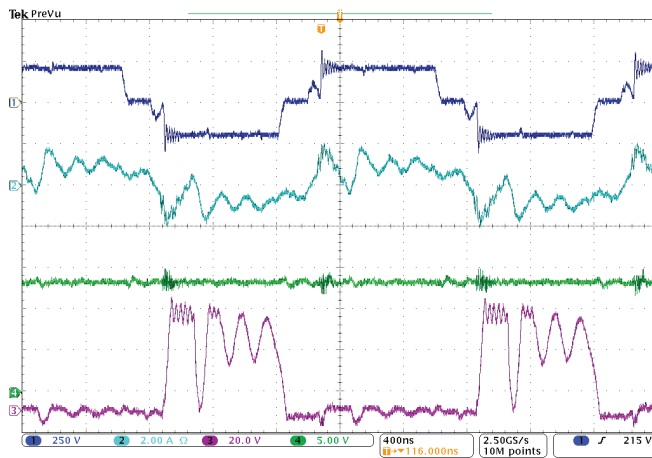


Figure 10. Waveform of v_p , i_p , v_{ds} , T_{SR1} and v_o , at half load 12.5 A and half input voltage (400 ns/div, CH1: 250 V/div, CH2: 2 A/div, CH3: 20 V/div, CH4: 5 V/div).

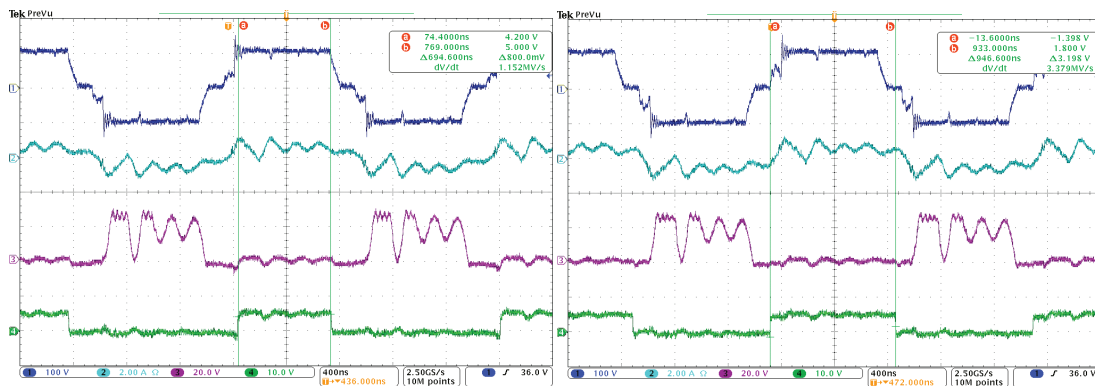


Figure 11. Waveform of v_p , i_p , v_{ds} , T_{SR1} and v_o , T_{SR1} difference in SR transistor switching between DCM and CCM, at quarter input voltage (400 ns/div, CH1: 100 V/div, CH2: 2 A/div, CH3: 20 V/div, CH4: 10 V/div). CCM, continuous conduction mode; DCM, discontinuous conduction mode; SR, synchronous rectifier.

additional circuit and reaches 50 V, which at full supply voltage could be approximately double, that is, 100 V, so still well below the maximum operating voltage of the transistor. The primary current is relatively distorted and does not reach the same shape as at lower switching frequencies, but this is understandable at higher switching frequencies. The primary voltage is relatively smooth, with oscillations arising mainly from the incomplete achievement of ZVS, which would be desirable at half load. For this reason, the inverter should be further optimised in future work, but this is not the subject of this article, as it is focused on the rectifier.

Figure 11 shows the difference in switching of the SR transistor in CCM and DCM, as was also shown in simulations in the programme PLECS. The boundary between switching in DCM and CCM is fixed based on the output current and filter inductance, in order to prevent the filter inductance current from dropping to zero and subsequently to negative values, as this would cause additional overvoltage on the rectifier. The more precisely this limit is set, and the more precisely the delay in the CCM is set, the lower the losses on the transistors will be.

Due to the complexity of measuring rectifier losses, the converter's total losses were measured at the DC input and DC output. The disadvantage is that it is not possible to directly determine the losses of the rectifier,

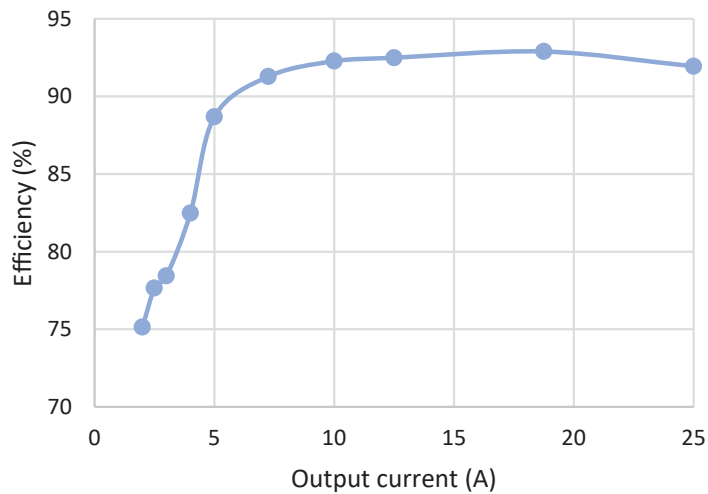


Figure 12. Efficiency of the laboratory model at half of input voltage.

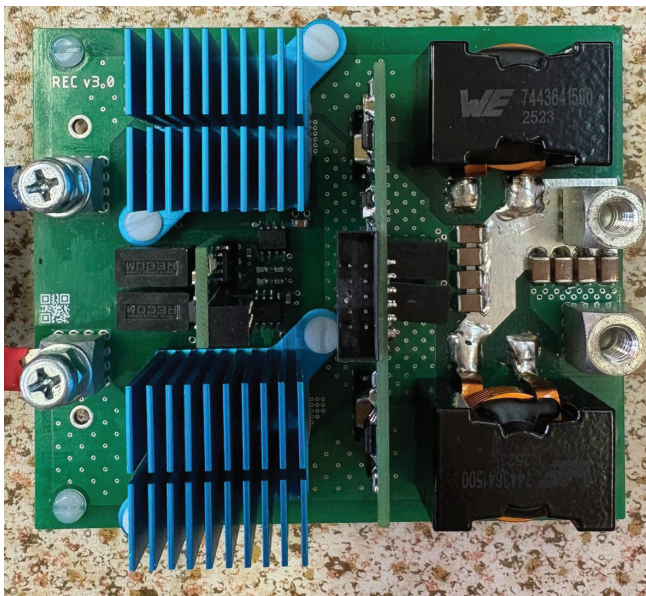


Figure 13. Thermal image of the driver of GaN transistors in a rectifier. GaN, gallium nitride.

but on the other hand, by measuring DC values at the input and output, we achieve relatively accurate results of efficiency, which was measured by the LMG500 device and is shown in Figure 12. The maximum efficiency of 92.89% was measured at an output current of 18.75 A. The shape of the efficiency curve shows that the inverter was not optimised, because with increasing current, losses from $R I^2$ grow exponentially, especially in the rectifier, but despite this, efficiency increases by up to 75% load. The reason for this is that with increasing current, the transistors of the converter achieved softer switching, but they only reached full ZVS at approximately 75% load. As shown in Figure 13, another advantage of GaN transistors is low gate charge Q_g ; in this case, the driver in the SO8 package driving three transistors reached a relatively low temperature in steady state at 500 kHz.

4. Conclusion

This paper presented a comprehensive investigation into the optimisation of an SR for a PSFB converter operating at a high switching frequency of 500 kHz. The primary objective was to evaluate the integration of GaN power transistors as a replacement for conventional Silicon (Si) devices in the secondary stage. Through a combination of analytical modelling and PLECS simulations, it was demonstrated that GaN transistors significantly reduce switching and overall losses due to their superior figures of merit, particularly their low output charge. However, the study also identified a critical trade-off: the inherent increase in reverse conduction losses during the dead-time interval preceding ZVS, a phenomenon more pronounced in high-frequency GaN applications.

To address this challenge, the research characterised the converter's performance across CCM and DCM regions. A key contribution of this work is the proposal of an adaptive delay strategy in the CCM region, specifically designed to minimise the duration of GaN reverse conduction. By precisely timing the gate signals, the duration of the body diode-like conduction was curtailed, thereby reclaiming efficiency that would otherwise be lost to the device's relatively high reverse voltage drop.

The proposed concepts were validated using a laboratory prototype. Experimental measurements were conducted under a high-stress scenario with an input supply voltage of 195 V and a full output load current of 25 A. The resulting oscilloscope waveforms confirmed stable operation and a well-regulated output voltage at the target frequency. Although the system achieved a maximum efficiency of approximately 93%, the analysis revealed that this performance was primarily limited by incomplete ZVS on the primary-side inverter stage rather than the optimised rectifier. This finding underscores the necessity of a holistic system design when migrating to wide bandgap (WBG) technologies.

Future research will build upon these results by focusing on the primary-side inverter's optimisation to achieve full ZVS across the entire load range. Furthermore, an innovative software-defined approach is planned, utilising high-bandwidth (up to 5 MHz) PCB-integrated Hall-effect current sensors on the secondary side. This enhancement will provide the DSP with high-fidelity, low-latency information regarding the current's zero-crossing. Such precise feedback will enable the rectifier to operate as an 'ideal diode,' further maximising power density and efficiency in high-frequency power conversion systems.

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References

- Alou, P., Oliver, J. A., Garcia, O., Prieto, R. and Cobos, J. A. (2006). Comparison of current doubler rectifier and center tapped rectifier for low voltage applications. In: *Proceedings of the Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition APEC '06*. Dallas, TX, USA, 2006. doi: 10.1109/APEC.2006.1620622.
- Beheshti, M. (2020). Wide-bandgap semiconductors: Performance and benefits of GaN versus SiC. *Analog Design Journal*. Texas Instruments,

- Chen, Z., Shi, L. and Ji, F. (2012). Mechanism and suppression countermeasure of voltage oscillation for full bridge converter. In: *Proceedings of the 7th International Power Electronics and Motion Control Conference PEMC*. Harbin, China, 2012, pp.1632–1638. doi:10.1109/IPEMC.2012.6259079.
- Chothe, S., Ugale, R. T. and Gambhir, A. (2021). Design and modeling of phase-shifted full bridge DC-DC converter with ZVS. In: *Proceedings of the 2021 National Power Electronics Conference NPEC*. 2021, pp. 1–6. doi: 10.1109/NPEC52100.2021.9672529
- Cui, Y., Zhang, W., Tolbert, L. M., Wang, F. and Blalock, B. J. (2014). Direct 400 V to 1 V converter for data center power supplies using GaN FETs. In: *Proceedings of the IEEE Applied Power Electronics Conference and Exposition APEC 2014*. 2014, pp. 3460–3464. doi: 10.1109/APEC.2014.6803806
- Dudrik, J., Pástor, M., Lacko, M. and Žatkovič, R. (2018). Zero-Voltage and Zero-Current Switching PWM DC–DC Converter Using Controlled Secondary Rectifier With One Active Switch and Nondissipative Turn-Off Snubber. *IEEE Transactions on Power Electronics*, 33(7), pp. 6012–6023. doi: 10.1109/TPEL.2017.2748569
- Escudero, M., Kutschak, M.-A., Meneses, D., Morales, D. P. and Rodriguez, N. (2020). Synchronous Rectifiers Drain Voltage Overshoot Reduction in PSFB Converters. *IEEE Transactions on Power Electronics*, 35(7), pp. 7419–7433. doi: 10.1109/TPEL.2019.2953797
- GaN Systems. (2016). *Design with GaN Enhancement mode HEMT*. Application Guide. GaN Systems.
- Mao, H., Abu-Qahouq, J. A., Qiu, W., Wen, Y. and Batarseh, I. (2003). Lossless snubber circuits for current doubler rectifiers to reduce reverse-recovery losses. In: *Proceedings of IECON'03. 29th Annual Conference of the IEEE Industrial Electronics Society*. Roanoke, VA, USA, 2003, 2639–2644 Vol.3. doi: 10.1109/IECON.2003.1280664.
- Mappus, S. (2004). *Current Doubler Rectifier Offers Ripple Current Cancellation*. Application Note. Texas Instruments.
- Park, K.-B., Kim, C.-E., Moon, G.-W. and Youn, M.-J. (2007). Voltage Oscillation Reduction Technique for Phase-Shift Full-Bridge Converter. *IEEE Transactions on Industrial Electronics*, 54(5), pp. 2779–2790. doi: 10.1109/TIE.2007.899872
- Pastor, M., Lacko, M., Dudrik, J. and Marcinek, A. (2023). Soft-switching full-bridge DC-DC converter with energy recovery capacitor snubber. *Energies*, 16(4). [Online]. Available: <https://www.mdpi.com/1996-1073/16/4/1591>
- Qi, X., Wang, Z., Wu, Y. and Zuk, P. (2019). Advantage of GaN in phase shift full bridges. In: *Proceedings of the IEEE 7th Workshop on Wide Bandgap Power Devices and Applications WiPDA*. 2019, pp. 384–387. doi: 10.1109/WiPDA46397.2019.8998838
- Renesas. (2018). *ZVS DC/DC Power Supply with Synchronous Rectifiers Evaluation Board. User's Manual*.
- Ruan, X. and Zhang, L. (2015). Voltage oscillation elimination in output rectifier diodes in zero-voltage-switching PWM full-bridge converter: An overview. In: *Proceedings of the IEEE Energy Conversion Congress and Exposition ECCE*. Montreal, QC, Canada, 2015, pp. 6328–6335. doi: 10.1109/ECCE.2015.7310547.
- Sam, A.-R. (2013). *Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier*. Design Note. Infineon.
- Texas instruments. (2014). *Phase-Shifted Full Bridge DC/DC Power Converter Design guide*. Application Note. Texas Instruments.
- Yu, S. and Lough, B. (2023). Achieving High Converter Efficiency with an Active Clamp in a PSFB Converter. *Analog Design Journal*. Texas Instruments,
- Yu, S.-Y., Lough, B. and Yin, L. (2023). Achieving High Converter Efficiency with an Active Clamp in a PSFB Converter. *Analog Design Journal*, 1Q 2023. Texas Instruments. Available at: <https://www.ti.com/lit/pdf/SLYT835>.
- Yu, S., Lough, B., Yin, R. and Ye, Q. (2024). Phase-Shifted Full-Bridge Converter Fundamentals. In: *Texas Instruments Power Supply Design Seminar, Topic 4, Literature No. SLUP414*. Available at: <https://www.ti.com/lit/pdf/SLUP414>.