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A Reduced Switch Single-Source Multilevel Inverter with GA-Based Selective Harmonic Elimination

Research paper

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Abstract: Multilevel inverters (MLIs) are widely employed in medium- and high-power applications due to their ability to generate high-quality output voltage with reduced switching losses and electromagnetic interference. However, conventional MLIs topologies often suffer from increased circuit complexity, higher switch count and large total standing voltage (TSV), leading to increased cost and reduced reliability. To address these challenges, this paper proposes a novel reduced switch single source (RSSS) MLI topology capable of generating multiple voltage levels with a significantly lower number of power switches. For a nine-level RSSS MLI, a genetic algorithm selective harmonic elimination (GA-SHE) technique is employed to determine optimal switching angles, enabling effective elimination of dominant lower-order harmonics, particularly the fifth and seventh harmonics, while maintaining a high fundamental voltage component at low switching frequency. A detailed comparative analysis is carried out to demonstrate the advantages of the proposed topology in terms of switch count and TSV. The performance of the proposed RSSS MLI is validated through MATLAB/Simulink (MathWorks, Inc.) and real-time experimental implementation using a dSPACE CP1104 controller under no-load, resistive and resistive–inductive load (RL-load) conditions. Both simulation and experimental results confirm that the proposed inverter produces high-quality output voltage and current waveforms with harmonic distortion levels compliant with IEEE-519 standards.

Keywords: *genetic algorithm • multilevel inverter • reduce switch count • selective harmonic elimination • total harmonic distortion*

1. Introduction

Power conversion equipment, such as multilevel inverters (MLIs), is increasingly being used in manufacturing and other commercial settings. Most of these uses controlling motors of varying voltages and high power. Additionally, MLIs are finding use in grid-connected systems, uninterrupted power supply (UPS), electric vehicles (EVs), & FACTS devices (Singh et al., 2024). MLI's maximises output voltage as a more sinusoidal oriented waveform, higher efficiency from lower switching operating frequency of switches, reduced blocking voltage required with dv/dt and enhanced electromagnetic compatibility make these uses conceivable (Li and Quan, 2017; Samsami et al., 2017). MLIs have gained significant attention in medium- and high-power applications such as motor drives, renewable energy systems and grid-connected converters due to their ability to generate high-quality output voltage with reduced switching losses and lower electromagnetic interference. However, conventional MLI topologies often require a large number of power switches, gate driver circuits and isolated DC sources, which increase system cost, complexity and total standing voltage (TSV).

One obvious disadvantage of MLI power conversion is the requirement for additional switching devices. This specific limitation may lead to a decrease in the overall performance of an inverter (Franquelo et al., 2008;

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Martins et al., 2006). Numerous MLI topologies, each with its own set of traits and capabilities, have been proposed by different researchers. The main objectives of these topologies in comparison to their previous versions are higher output voltage and lower power usage. Its simplicity is frequently attributed to Cascaded H-bridge Multilevel Inverters (CHB MLIs) capacity to generate five levels per phase with 8 switches, 7 with 12 switches, 9 with 16 switches and so on (Jimenez et al., 2011; Koshti et al., 2017; Lakshmi et al., 2013; Malathy, 2012). Many academics have been working to lower the MLI's overall size and cost in recent years. Therefore, the development of reduced-switch-count MLI topologies with improved power quality and lower TSV remains an active area of research. The paper presented in Babaei et al. (2014b) provides a topology with lower blocking voltage using switches and various techniques to determine the amplitude of the DC voltage source. With a switched capacitor and DC source, respectively, the MLI topologies described in Babaei and Gowgani (2014) and Gupta and Jain (2014) employ a precise number of switches to achieve high voltage steps. The topology presented in Babaei and Gowgani (2014) may be useful for a high-frequency application.

In recent years, MLI topologies have received significant attention due to their capability to produce high-quality voltage waveforms with reduced harmonic distortion and lower switching stress. A comprehensive overview of MLI structures for EV applications has been presented by Poorfakhraei et al. (2021), highlighting the advantages of MLIs in improving efficiency, reliability and power quality in modern power electronic systems.

Advanced control strategies have also been developed for MLIs. Valdez-Fernandez et al. (2023) proposed a model-based control strategy for three-phase CHB multilevel converters that achieves very low total harmonic distortion (THD) in output waveforms. Similarly, Chatterjee and Kastha (2024) introduced a new multilevel converter configuration for medium-voltage open-winding permanent magnet synchronous generator (PMSG) systems used in wind energy applications. Their proposed configuration demonstrates improved current waveform quality and reduced harmonic distortion.

In addition, Catzin-Contreras et al. (2024) proposed an energy model-based control approach for grid-connected modular multilevel converters, where phase-shifted carrier-based pulse width modulation was used to maintain capacitor voltage balancing. Recently, Hosseinzadeh et al. (2024) introduced a generalised multisource inverter topology for EV applications employing model predictive control to achieve improved dynamic performance.

Furthermore, new multisource MLI structures have been proposed to increase flexibility in power sources and improve system efficiency (Espinosa et al., 2025). However, many of these topologies require increased component count, multiple power sources, or complex control strategies (Lee et al., 2016). Therefore, the development of MLI structures with reduced switch count and simplified control strategies remains an active research area. Improving power quality and efficiency are the most important challenges to be solved with these MLIs. The main difficulty with these MLIs is increasing efficiency through the use of suitable modulation and control strategies.

Although sinusoidal PWM and space-vector PWM methods are advised for MLI in order to regulate output voltage & limit unwanted harmonics, it has been shown that these strategies are unable to entirely eradicate low-order harmonics (Holmes and Lipo, 2003; Kouro et al., 2007). Selecting switching angles to suppress certain dominant harmonics of a lower order is another method. The term 'selective harmonic elimination' (SHE) describes this method (Fei et al., 2010). SHE is a widely adopted low-switching-frequency modulation technique for MLIs, as it effectively suppresses dominant lower-order harmonics while maintaining a high fundamental voltage component. The SHE technique has been adopted by a number of researchers because it successfully fixes the primary output voltage component while simultaneously lowering voltage's harmonics. The magnitude of THD is reduced with the use of real-time computations of switching angles supported by analytical proof, which has been presented by Liu et al. (2009). All triplen harmonics can be removed using this procedure, but other harmonic orders cannot. Obtaining an analytic solution for non-linear equations is most challenging for the SHE approaches (Massrur et al., 2016). Iterative approaches, like Newton–Raphson method (Ahmad et al., 2018), may be used to find solutions to such non-linear equations. A good initial estimate is necessary for repeat-based approaches. However, this technique can only determine a single class that is heavily dependent upon starting assumption. Popular examples of evolutionary algorithms in use today include the genetic algorithms (GA), the imperialist competitive algorithm and particle swarm optimization (PSO) (Etesami et al., 2015; Panda and Panda, 2018). They'll look for the simplest solution possible (Eddine et al., 2018). In the paper Kamarposhti (2018) and Latif et al. (2022), a switching method known as modified PSO is explained. It is employed to determine the best way to estimate switching angles. However, the PSO algorithm's primary drawbacks are its low iterative convergence rate and ease of local optimum fall in high-dimensional space. In the paper Hamad et al. (2024), a different technique known as the artificial bee colony (ABC) technique was employed for optimisation to minimise transmission loss and have a powerful ability

to search equations. However, its inadequate development potential and lack of demographic diversity are its drawbacks. Another technique that minimises frequency and power transmission variation with great accuracy is the cuckoo search algorithm (CSA). This algorithm's primary flaw is that it lacks dampening under various power system operating conditions (Ahmadi Kamarposhti et al., 2022). Among these bio-inspired algorithms, GA, Ozpineci et al. (2005) offers several advantages, including their ability to handle complex, non-linear problems, their inherent parallelism and their capacity for global optimisation, making them suitable for a wide range of optimisation tasks. Therefore, in this paper GA method is used for the calculations of switching angles of proposed MLI.

Motivated by these challenges, this paper proposes a novel reduced switch single source (RSSS) MLI topology that significantly reduces the number of power switches while maintaining high-quality output voltage. The proposed topology employs a modular structure consisting of a level generation unit (LGU) and a polarity generation unit (PGU), enabling easy extension to higher voltage levels. Furthermore, a GA-based SHE strategy is implemented to optimally determine switching angles for eliminating lower-order harmonics. The effectiveness of the proposed RSSS MLI is validated through detailed MATLAB/Simulink simulations and real-time experimental results using a dSPACE CP1104 platform under various load conditions, demonstrating its suitability for practical power electronics and drive applications.

1.1. Main contributions of the paper

The main contributions of this paper are summarised as follows:

- A novel RSSS MLI topology is proposed, which significantly reduces the number of power switches and gate driver circuits compared to conventional MLI structures.
- The proposed RSSS MLI achieves reduced TSV, thereby lowering switch voltage stress and overall system cost, making it suitable for medium- and high-power drive applications.
- A genetic algorithm-based selective harmonic elimination (GA-SHE) technique is employed to determine optimal switching angles for a nine-level inverter, effectively eliminating the fifth, seventh order harmonics.
- A detailed comparative analysis with recently reported MLI topologies is presented in terms of switch count, DC source requirement and TSV.
- The proposed topology and control strategy are validated through MATLAB/Simulink simulations and real-time experimental implementation using a dSPACE CP1104 controller under no-load, resistive and resistive–inductive load (RL-load) conditions, demonstrating compliance with IEEE-519 harmonic standards.

2. Proposed Topology

The new suggested RSSS MLI topology is shown in Figure 1. Both the LGU & PGU make up this system. The LGU is made up of a number of switches (N_{sw}), one unidirectional switch (N_u) and one bidirectional switch (N_B), as well as a number of DC voltage sources (N_{DC}), which is determined by the number of inverter levels (N_{level}). When the load is inductive, negative and positive voltages must be opposed, hence bidirectional switches are used. Coils of wire in inductive loads, such as motors, solenoids and fluorescent ballasts, store energy in the form of magnetic field. The term 'flyback voltage' or 'back EMF' refers to the abrupt spike in current and voltage that occurs when an inductive load is turned off due to the collapsing magnetic field. A typical single-pole switch's contacts may sustain damage from this abrupt surge, leading to arcing, pitting and early failure. To manage these surges and safeguard the switch contacts, two-way switches and other speciality switches (such as those with an integrated flyback diode or IGBT) are made. In order to survive the inductive load switching conditions, they frequently include features like arc suppression or a greater current rating. Therefore, this proposed MLI uses IGBTs as switch for the operation of inverter. Other components, like voltage source and one load are also required. Table 1 depicts RSSS MLI switching sequence. By using this circuit, the required amount of output voltage may be achieved by Eq. (1)

$$N_{level} = 2n + 1 \tag{1}$$

Here n signifies number of LGU unit. The PGU unit consists of four unidirectional switch, which is fixed for every level of MLI. The operation of these PGU unit is to generate polarity between the output voltage levels. Relationship amongst N_u, N_B, N_{sw} and N_{DC} based on number of levels being obtained into Eqs. (2)–(5)

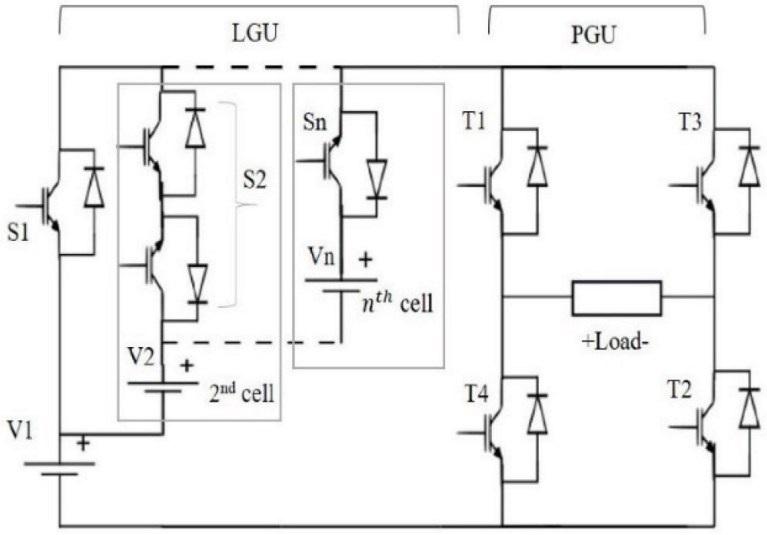


Figure 1. Proposed topology. LGU, level generation unit; PGU, polarity generation unit.

Table 1. Switching sequence of proposed RSSS MLI.

State	S_1	S_2	…	S_n	T_1	T_2	T_3	T_4	V_{dc}
1	0	0	…	0	0/1	1/0	0/1	1/0	0
2	1	0	…	0	1	0	1	0	+1
3	1	0	…	0	0	1	0	1	−1
4	0	1	…	0	1	0	1	0	+2
5	0	1	…	0	0	1	0	1	−2
6	0	0	…	0	1	0	1	0	+3
7	0	0	…	0	0	1	0	1	−3
⋮	⋮	⋮	…	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	…	⋮	⋮	⋮	⋮	⋮	⋮
$N_{level}-1$	0	0	…	1	1	1	0	0	+n
N_{level}	0	0	…	1	0	0	1	1	−n

RSSS, reduced switch single source; MLI, multilevel inverter.

$$N_u = 2 \tag{2}$$

$$N_B = \left(\frac{N_{\text{level}}-1}{2}\right) - 2 \tag{3}$$

$$N_{\text{DC}} = \frac{N_{\text{level}}-1}{2} \tag{4}$$

$$N_{\text{sw}} = \left(\frac{N_{\text{level}}-1}{2}\right) + 4 \tag{5}$$

2.1. Comparison among other MLI topologies

Over the last decade, several MLI topologies were suggested by researchers. The goal of constructing these MLI topologies was to achieve the lowest possible cost by minimising number of switches, the standing voltage, the switching loss and conduction loss. The primary motivation for the development of proposed RSSS MLI is to generate a large number of levels with a small number of switches. Thus, the suggested RSSS MLI is compared to traditional CHB MLI and a number of previously constructed MLI topologies (MLI1, MLI2, MLI3, MLI4, MLI5 & MLI6) reported in

Babaei et al. (2014a,b), Hsieh et al. (2016), Jayabalan et al. (2017), Lee et al. (2018), Najjar et al. (2016) and Oskuee et al. (2015). The TSV and number of required circuit components for each MLI topology are listed in Table 2.

The complexity of circuit may be decreased by minimising number of power switches. The several MLI topologies and number of switches used in each are shown in Figure 2. Although fewer switches are needed to implement MLI1, MLI2 & MLI3, this is still more than the proposed RSSS MLI and significantly less than CHB MLI. MLI6 also has the lowest switch count need of all possible network circuits. The quantity of DC voltage source is another component that impacts voltage at output. Different topologies, as shown in Figure 3, use different numbers of DC voltage sources for the same level. This means that the number of DC sources needed for MLI2, MLI5, & MLI6 is the same that needed for CHB MLI, MLI1, MLI3, MLI4 and the proposed RSSS MLI. The proposed RSSS MLI requires more DC voltage sources than MLI2, MLI5 and MLI6, yet only a single DC voltage source is in use for a particular level.

As such, TSV must be taken into account during the construction of an inverter module. Figure 4 shows the various TSV MLI topologies and suggested RSSS MLI. The power rating of a switch is affected by the amount of blocking voltage along its path; hence, this value is crucial when designing an inverter. When TSV value drops, the inverter's total cost drops with it. The voltage needed to block off LGU power switch is about same as Eq. (6),

$$V_{s1} = V_{s2} = V_{s3} = \ldots\ldots\ldots = V_{sn} = nV_{dc} \tag{6}$$

In a PGU, amplitude of maximum output voltage is equal to blocking voltage of power switches, as shown in Eq. (7),

$$V_{T1} = V_{T2} = V_{T3} = V_{T4} = V_{\max} = nV_{dc} \tag{7}$$

Here, V_{max} represents the maximum allowable voltage at the output terminals. TSV, which may be calculated as in Eqs (8)–(10), is the total blocking voltage of power switches for both LGU and PGU,

$$V_{\mathrm{LGU}} = V_{s1} + V_{s2} + V_{s3} + \ldots\ldots\ldots\ldots + V_{sn} = nV_{dc} \tag{8}$$

$$V_{\mathrm{PGU}} = V_{T1} + V_{T2} + V_{T3} + V_{T4} = 4nV_{dc} \tag{9}$$

$$\therefore \mathrm{TSV} = \left(4n + n\right)V_{dc} = 5nV_{dc} \tag{10}$$

Table 2. Comparison of proposed RSSS MLI with recently developed MLI topologies.

MLI topologies	N_{sw}	N_{DC}	TSV
CHB MLI Najjar et al. (2016)	$2\left(N_{\mathrm{level}} - 1\right)$	$\frac{\left(N_{\mathrm{level}} - 1\right)}{2}$	$2\left(N_{\mathrm{level}} - 1\right)V_{DC}$
MLI1 Oskuee et al. (2015)	$\frac{2\left(N_{\mathrm{level}} + 8\right)}{3}$	$\frac{\left(N_{\mathrm{level}} - 1\right)}{2}$	$\left(3N_{\mathrm{level}} - 7\right)V_{DC}$
MLI2 Babaei et al. (2014a)	$\left(N_{\mathrm{level}} + 3\right)$	$\frac{\left(N_{\mathrm{level}} - 1\right)}{4}$	$2\left(N_{\mathrm{level}} - 1\right)V_{DC}$
MLI3 Lee et al. (2018)	$\frac{5\left(N_{\mathrm{level}} - 1\right)}{3}$	$\frac{\left(N_{\mathrm{level}} - 1\right)}{2}$	$3\left(N_{\mathrm{level}} - 1\right)V_{DC}$
MLI4 Hsieh et al. (2016)	$\frac{2\left(N_{\mathrm{level}} - 1\right)}{3} + 4$	$\frac{N_{\mathrm{level}}}{3}$	$\left(2N_{\mathrm{level}} + 8\right)V_{DC}$
MLI5 Jayabalan et al. (2017)	$\left(N_{\mathrm{level}} + 1\right)$	$\frac{\left(N_{\mathrm{level}} - 3\right)}{2}$	$35\frac{\left(N_{\mathrm{level}} - 1\right)}{4}V_{DC}$
MLI6 Babaei et al. (2014b)	$\frac{3\left(N_{\mathrm{level}} - 1\right)}{4}$	$\frac{\left(N_{\mathrm{level}} - 1\right)}{4}$	$5\frac{\left(N_{\mathrm{level}} - 1\right)}{2}V_{DC}$
Proposed RSSS MLI	$\frac{\left(N_{\mathrm{level}} - 1\right)}{2} + 4$	$\frac{\left(N_{\mathrm{level}} - 1\right)}{2}$	$5\frac{\left(N_{\mathrm{level}} - 1\right)}{2}V_{DC}$

CHB MLI, cascaded H-bridge multilevel inverter; MLI, multilevel inverters; RSSS, reduced switch single source; TSV, total standing voltage.

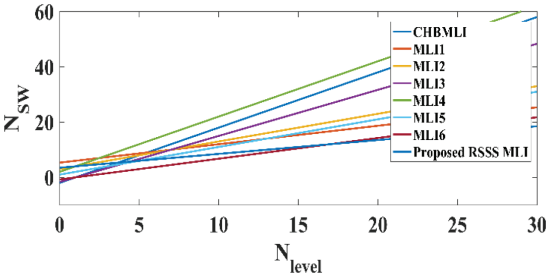


Figure 2. Number of switches against number of levels. CHB MLI, cascaded H-bridge multilevel inverter; MLI, multilevel inverters; RSSS, reduced switch single source.

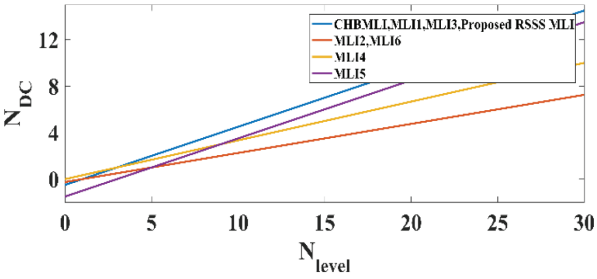


Figure 3. Number of DC voltage source against number of levels. CHB MLI, cascaded H-bridge multilevel inverter; MLI, multilevel inverters; RSSS, reduced switch single source.

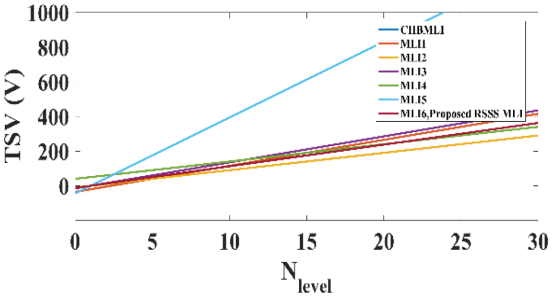


Figure 4. Value of TSV against number of levels. CHB MLI, cascaded H-bridge multilevel inverter; MLI, multilevel inverters; RSSS, reduced switch single source; TSV, total standing voltage.

Where *n* is the total number of LGUs unit. The maximum blocking voltage may be calculated using the DC voltage source's strength and the total number of LGUs. According to Figure 4, the greatest TSV values are seen in MLI5, MLI4, & MLI3. These high values are not desirable for circuit functioning. However, TSV for proposed RSSS MLI & MLI1 are practically the same, and they are much lower than those for MLI3, MLI4 and MLI5. The voltage stress across semiconductor devices is significantly influenced by the TSV of the topology. Compared with conventional CHB and several reduced-switch MLIs, the proposed RSSS inverter exhibits lower voltage stress due to its optimised LGU–PGU architecture. Consequently, devices with lower voltage ratings can be employed, improving overall system reliability and reducing cost.

Given the above analysis, it is clear that proposed RSSS MLI requires just a small number of switches and a DC voltage source with no diode components. An advantage of proposed topology is that it may be extended to as many layers as needed.

Table 3 presents a comparison between the proposed RSSS MLI and several recently reported MLI topologies published between 2022 and 2025. It can be observed that most recent converters either require a higher number of power switches, multiple DC sources or complex capacitor balancing mechanisms. In contrast, the proposed RSSS MLI achieves a lower switch count while maintaining acceptable harmonic performance using the GA-based SHE technique. Consequently, the proposed topology offers a favourable tradeoff between circuit complexity, harmonic performance and implementation cost compared with existing structures.

2.1.1. Performance comparison with recent topologies

To highlight the advantages of the proposed RSSS MLI, a comparative analysis is performed with several recently reported reduced-switch MLI topologies. Key performance metrics including number of switches, DC sources, voltage gain, TSV, THD and control complexity are considered. Table 4 presents a comprehensive comparison between the proposed RSSS MLI and several conventional as well as recently reported MLI topologies. Recently proposed multisource and switched-capacitor MLIs aim to increase voltage gain and flexibility in energy integration. For example, the reduced switched-capacitor inverter presented by Hosseinzadeh et al. (2022) achieves higher voltage gain but requires capacitor voltage balancing. Similarly, the generalised multisource inverter proposed by Hosseinzadeh et al. (2024) improves dynamic performance through model predictive control but increases

Table 3. Comparison of proposed RSSS MLI with recently developed MLI topologies between 2022 and 2025.

Ref.	Topology	No. of levels	Switch count	DC sources	Control/ modulation	THD (%)	Efficiency (%)	Remarks
Goel et al. (2022)	Single DC-source 13-level MLI	13	10	1	Fundamental switching	~8–10	~95	Reduced device count but limited scalability
Kubendran et al. (2022)	Reduced-switch cascaded MLI	9–17	12	Multiple	Nearest level control	~9–12	~94	Suitable for EV applications but requires multiple sources
Jena et al. (2024)	Transformer-less switched-capacitor MLI	9	12	1	PWM-based control	16.48	~94	Self-balancing capacitors but higher THD without filtering
Saravanan et al. (2024)	Reduced-device 31-level inverter	31	12	Multiple	SPWM	<8	~95	Higher number of levels but increased circuit complexity
Mohanty et al. (2025)	Reduced-switch asymmetrical MLI	9–13	10–12	Multiple	PSO-optimised controller	~7–9	~95	Designed for DC microgrid applications
Awadelseed et al. (2026)	Switched-capacitor ANPC inverter	9	10–12	1	Optimised modulation	~5–7	96.9	High efficiency but uses capacitor balancing circuitry
Proposed RSSS MLI	This work	9	8	1	GA-SHE	≈10.86	≈95	Reduced switch count with GA-based harmonic elimination

EVs, electric vehicles; GA, genetic algorithms; GA-SHE, genetic algorithm selective harmonic elimination; MLI, multilevel inverters; PSO, particle swarm optimization; RSSS, reduced switch single source; THD, total harmonic distortion.

Table 4. Comparison of performance of proposed RSSS MLI and recently developed MLI topologies.

Topology	Output levels	Power switches	DC sources	Diodes/ capacitors	Voltage gain	TSV	Control technique	THD (%)	Remarks
CHB MLI Najjar et al. (2016)	9	16	4	0	High	High	PWM/SHE	8–12	Modular but high switch count
MLI1 Oskuee et al. (2015)	9	12	4	2	Medium	Medium	PWM	9–13	Moderate complexity
MLI2 Babaei et al. (2014)	9	10	3	2	Medium	Medium	PWM	10–14	Multiple DC sources
MLI3 Lee et al. (2018)	9	12	4	2	Medium	High	SPWM	9–12	Higher voltage stress
MLI4 Hsieh et al. (2016)	9	10	4	2	Medium	High	PWM	10–13	Increased circuit complexity
MLI5 Jayabalan et al. (2017)	9	10	3	2	Medium	High	SPWM	9–12	Higher TSV
MLI6 Babaei et al. (2014)	9	10	3	0	Medium	Medium	PWM	9–13	Reduced device count
Reduced Switched-Capacitor MLI Hosseinzadeh et al. (2022)	9	10–12	Multiple	Capacitors	High	Medium	PWM	<10	Requires capacitor voltage balancing
Reduced-switch cascaded MLI Kubendran et al. (2022)	9–17	12	Multiple	0	Medium	Medium	Nearest Level Control	9–12	Requires multiple sources
Generalised Multisource Inverter Hosseinzadeh et al. (2024)	9–13	12	Multiple	Capacitors	High	Medium	Model predictive control	<8	High control complexity
Multi-Source MLI Espinosa et al. (2025)	9	10–12	Multiple	Capacitors	High	Medium	PWM	<10	Flexible multi-source operation
Proposed RSSS MLI	9	8	Single source	None	High	Low	GA-SHE	10.86	Reduced switch count and simplified control

CHB MLI, cascaded H-bridge multilevel inverter; GA-SHE, genetic algorithm selective harmonic elimination; MLI, multilevel inverter; SHE, selective harmonic elimination; RSSS, reduced switch single source; MLI, multilevel inverter; THD, total harmonic distortion; TSV, total standing voltage.

control complexity. The multi-source MLI presented by Espinosa et al. (2025) enables integration of multiple energy sources; however, it requires additional components and complex implementation.

It can be observed that the proposed RSSS topology requires fewer switches while maintaining competitive voltage gain and reduced TSV. Furthermore, the use of the GA-SHE technique enables improved harmonic performance without increasing switching frequency. Therefore, the proposed topology provides a favourable tradeoff between hardware complexity and output power quality compared to existing structures.

The theoretical analysis of the proposed inverter is derived based on the following assumptions:

(1) All DC sources are assumed to have equal voltage magnitude.
(2) Semiconductor switches are considered ideal during analytical derivation.
(3) The inverter operates under symmetrical switching conditions.
(4) Load current ripple is assumed negligible compared to the fundamental component.

Based on these assumptions, the output voltage waveform of the nine-level RSSS inverter can be represented using Fourier series expansion. The switching angles are calculated using the SHE technique to eliminate dominant low-order harmonics while maintaining the required fundamental voltage component. Here, we look at the suggested nine-level RSSS structure, which can provide nine different voltage levels using the Eq. (1). Switching angles are θ_1, θ_2, θ_3 *and* θ_4. Each LBU's output voltage is added together to form the output voltage. The nine-level RSSS MLI's waveform output may be represented as a Fourier series, as seen in Eq. (11)

$$V_o(\omega t) = \sum_{n=1,3,5,7\ldots}^{\infty} \frac{4}{n\pi}\left(V_{dc}\cos(n\theta_1) + V_{dc}\cos(n\theta_2 + \ldots\ldots + V_{dc}\cos(n\theta_4)\right)\sin(\omega t) \tag{11}$$

A H-bridge maximum output voltage is represented by the number 4/nπ, and an adjustable modulation index may be employed in Eq. (12)

$$m_a = \frac{V_1}{V_{\max}} = \frac{\pi V_1}{4V_{dc}} \tag{12}$$

Here m_a is modulation index, and V_1 is fundamental component of output voltage of anticipated inverter. The suggested topology should provide four switching angles. Fifth, seventh, eleventh, thirteenth selected harmonics were taken into account while designing the suggested topology. In order to get rid of the previously described harmonic ordering, relation of Eq. (11) has to be solved to get θ_1 to θ_4 under the following condition in Eq. (13)

$$\theta_1 < \theta_2 < \theta_3 < \theta_4 < \frac{\pi}{2} \tag{13}$$

Mathematically SHE problem is given as in Eq. (14)

$$\begin{aligned}
&\cos(\theta_1) + \cos(\theta_2) + \ldots + \cos(\theta_4) = nm_a \\
&\cos(5\theta_1) + \cos(5\theta_2) + \ldots + \cos(5\theta_4) = 0 \\
&\cos(7\theta_1) + \cos(7\theta_2) + \ldots + \cos(7\theta_4) = 0 \\
&\cos(11\theta_1) + \cos(11\theta_2) + \ldots + \cos(11\theta_4) = 0 \\
&\cos(13\theta_1) + \cos(13\theta_2) + \ldots + \cos(13\theta_4) = 0
\end{aligned} \tag{14}$$

Where n is the total amount of H-bridges used per phase. Using the specified value of m_a (between 0 and 1), the GA determines the unknown switching angles θ_1, θ_2, θ_3 and θ_4 for trigger semiconductor switches. The system of transcendental equations represented in Eq. (14) is a kind of equation known as a SHE equation. The main challenge is to solve these non-linear transcendental equations as many local minima may be there which make it difficult to find exact solution using some numerical methods. A non-deterministic method will be adopted here to solve for switching angles that will provide optimal solutions even for cases where no solution exists. Newton–

Raphson method requires the best guess for initial switching angles to obtain the exact solution, which is the main disadvantage of this method.

From a population of points, GA search parallelly. Unlike the traditional methods, which search from a single point, it has the ability to avoid being trapped in local optimal solution. It doesn't use deterministic selection rules. Therefore, it uses probabilistic selection rules. It works on the encoded version of potential solution parameters which is chromosome rather than the parameter itself. The fitness score is obtained from objective functions, which is used in this algorithm without other auxiliary or derivative information.

3. GA

One kind of random search algorithm, GA take their inspiration from natural selection. Although GA has shown to be effective at tackling linear, convex and other conventional optimisation problems, they excel at handling discrete & non-linear problems. In the natural world, better chromosomes are passed down from generation to generation. In the meanwhile, chromosomal alterations may develop and perhaps result in a new generation. This method is also used by the GA to find a solution. In GA, we may produce a number of potential answers to a problem by simulating the evolution of a population of hypothetical solvers. The term 'primitive population' is used to describe this first collection of answers. A chromosome is a unit of reaction. After the best chromosomes have been chosen, GA uses its operators to merge them & introduce a flaw. In the end, it merges the original population with the one that emerged through the chromosomal fusion and mutation. To help GA find best answers in a broad search area, fitness function is crucial. The purpose of this work is to decrease THD & minimise 5th, 7th, 11th, & 13thorder harmonics. Therefore, there must be a connection between fitness function and THD.

Typical GA procedures are given below in step-wise and Figure 5 represents the flowchart of this algorithm.

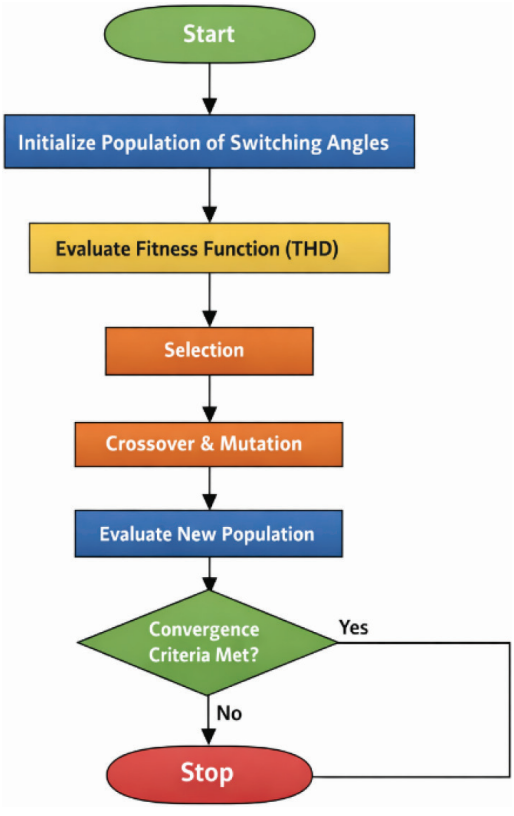


Figure 5. Flowchart of GA for harmonic elimination. GA, genetic algorithm; THD, total harmonic distortion.

Step 1 Set the GA toolbox system settings to their default values, including Crossover, Mutation, etc. Put a 100% value on the generation variable.
Step 2 Evaluate fitness function THD

$$THD = \sqrt[2]{\left(\frac{V_{rms}^2}{V_{1rms}^2}\right) - 1}$$

Step 3 Check constraints of Eq. (13).
Step 4 Choosing parent chromosomes.
Step 5 Generating new offspring by mutation & crossover.
Step 6 Verify whether terminating point has been reached (maximal number of repetitions). If not, go to step 2.
Step 7 End the problem if optimal switching angles are attained.

4. Power Loss Analysis

The efficiency of the proposed RSSS MLI is influenced by semiconductor conduction losses, switching losses and capacitor ripple losses. The total power loss can be expressed as in Eq. (15)

$$P_{\text{loss}} = P_{\text{conduction}} + P_{\text{switching}} + P_{\text{capacitor}} \tag{15}$$

Conduction losses are calculated based on the on-state voltage drop of the semiconductor devices and the load current. Switching losses occur during turn-on and turn-off transitions and depend on switching frequency and device characteristics. Capacitor ripple losses arise due to charging and discharging processes during switching cycles. In general, conduction losses can be given for IGBT ($P_{C,T}$) and diode ($P_{C,D}$) in Eqs (16) and (17) (Boora and Kumar, 2017)

$$P_{C,T} = \frac{1}{2\pi}\int_0^{2\pi}\left[v_{T0}(t) + r_T i_c(t)\right] i_c(t)\, d(\omega t) \tag{16}$$

$$P_{C,D} = \frac{1}{2\pi}\int_0^{2\pi}\left[v_{D0}(t) + r_D i_c(t)\right] i_c(t)\, d(\omega t) \tag{17}$$

where r_D and r_T is the on-state resistance of the diode and IGBT, respectively, v_{D0} and v_{T0} is the on-state reverse voltage of diode and IGBT correspondingly, $i_c(t)$ is current via IGBT or diode at instant *t*.

$$P_C = n_1 P_{C,T} + n_2 P_{C,D} \tag{18}$$

$$P_C = [n_1 V_{T0} + n_2 V_{D0}] I_{rms} \tag{19}$$

For complete fundamental cycle, conduction energy loss (E_C) can be written as follows in Eq. (20)

$$E_C = [n_1 V_{T0} + n_2 V_{D0}] I_{\text{rms}} \tag{20}$$

Values of various parameters of switch has been illustrated into Table 5.

Switching losses is the combination of two losses at time of turn-off and turn-on. Voltage and current are varies linearly considering approximation during switching, energy losses during turn-off and turn-on period of switch are given as in Eqs (21) and (22),

$$E_{\text{on}} = \frac{1}{6} V_{\text{sss}} I t_{\text{on}} \tag{21}$$

$$E_{\text{off}} = \frac{1}{6} V_{\text{sss}} I t_{\text{off}} \tag{22}$$

Table 5. IGBT parameters.

V_{dc}	50 V
I_{rms}	2.16 A
V_{T0}	0.8 V
V_{D0}	1.1 V
T	20 ms
t_{on}	700 ns
t_{off}	450 ns

where t_{off} and t_{on} are turn-off cross interval time and turn-on cross interval time, respectively, V_{sss} is voltage across switch after turning off or before turning on of switch, E_{off} and E_{on} are energy loss during turn-off and turn-on, respectively, I is current via switch after turning off or before turning on. During single turn-off and on, total energy loss of switches can be given as in Eq. (23),

$$E_S = E_{on} + E_{off} = \frac{1}{6} V_{sw} I \left(t_{on} + t_{off} \right) \tag{23}$$

Under-rated load conditions of nine-level MLI, the calculated conduction loss of CHB MLI is 334.70 mJ, whereas RSSS MLI has 131.20 mJ. Also, the switching loss of CHB MLI is 0.38 mJ and that of RSSS MLI is 0.74 mJ. Overall, the total power loss of CHB MLI is 335.08 mJ and that of RSSS MLI is 131.94 mJ, which is very less compared to CHB MLI.

5. Simulation Results

The ability of proposed RSSS MLI to create all negative and positive levels in output voltage is validated in this part using a simulation model in MATLAB/Simulink. For the simulation of a nine-level inverter, four voltage sources with values of 12 V are used that is V_1, V_2, V_3 and V_4. As a result, the peak amplitude of the output phase voltage is 48 V.

Figure 6a, b illustrate the voltage waveforms & output current for a nine-level MLI, respectively. The RL-load is utilised in this topology, with R = 10 Ω and L = 20 mH. The suggested MLI can create all nine levels at output side. The GA-SHE method is used to calculate the firing angles θ_1, θ_2, θ_3 & θ_4. The modulation index ranges between 0 and 1. Higher than 1 and lower than 0 can lead to distortion of signal. Therefore, an optimum modulation index is selected between 0 and 1 (nearly 0.9), which results in better THD of output signal. By keeping the modulation index near to 1, the carrier wave's amplitude is never completely suppressed or reversed. This ensures that the original message signal can be accurately extracted at the receiver. The simulation has been performed for different modulation indexes ranging from 0.6 to 1. We can see from Table 5, the THD of output voltage is minimum at modulation index 1. But it is not possible to attain modulation index 1. Also, the modulation index depends upon the number of levels. At a higher modulation index, switches stay on longer (good for conduction loss), but fast transitions might increase switching losses. The balance between output quality and efficiency is required. So, we consider modulation index of 0.95 for testing the proposed RSSS MLI. Therefore, results are calculated for modulation index 0.95.

For a modulation index of 0.95, the optimum firing angles, in radians, are θ_1 = 0.1717, θ_2 = 0.3557, θ_3 = 0.6703, & θ_4 = 1.054, as calculated by solving a MATLAB script file. The pulses that trigger switches in MLI are generated by using these optimum angles. Figure 7a depicts the relationship between modulation index and range of switching angles. Figure 7b shows the variation of voltage THD and current THD with respect to modulation index. Figure 7a and 7b are also represented in Tables 6 and 7, respectively. Figure 8a and 8b provide a THD analysis of the output phase voltage and phase current, respectively. According to THD study, output voltage and current nearly below 2% for fifth and seventh harmonic components. The circuit's THD shifts when the modulation index is adjusted.

To evaluate the robustness of the proposed RSSS inverter, transient simulations were conducted under sudden load variations. The load resistance was changed from 20 Ω to 10 Ω at t = 0.2 s. The inverter maintained stable output voltage levels and quickly restored steady-state operation within a few cycles. This demonstrates the dynamic stability and robustness of the proposed GA-SHE control strategy.

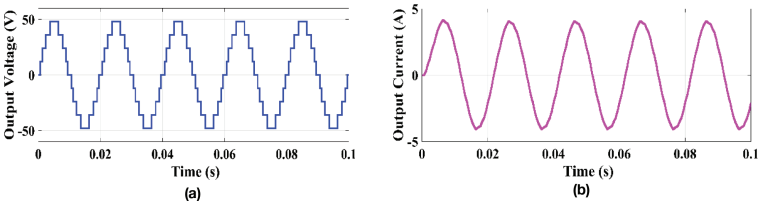


Figure 6. (a) Output voltage of nine-level RSSS MLI using RL-load. (b) Output current of nine-level RSSS MLI using RL-load. MLIs, multilevel inverters; RL, resistive–inductive load; RSSS, reduced switch single source.

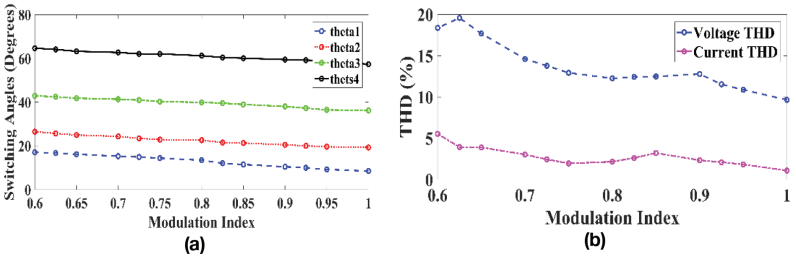


Figure 7. (a) Variations of switching angles with modulation index. (b) Variations of THD with modulation index. THD, total harmonic distortion.

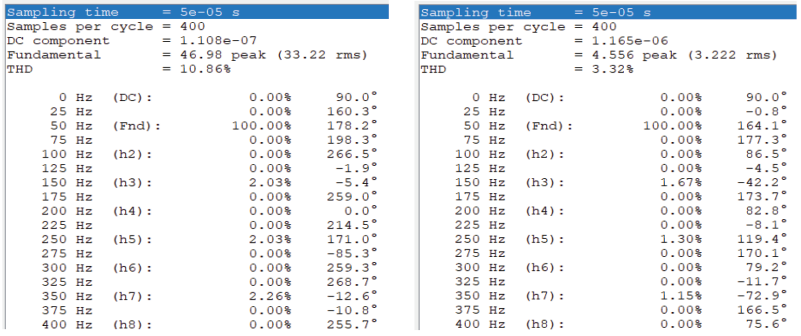
Table 6. Variation of switching angles with modulation index.

Modulation index	θ_1	θ_2	θ_3	θ_4
1.000	8.4389	19.2314	36.1245	57.3176
0.950	9.1926	19.5797	36.4326	58.9095
0.925	9.9500	20.0029	37.2343	59.1851
0.900	10.4054	20.4507	38.0021	59.4559
0.850	11.4501	21.2809	38.9241	60.0872
0.825	12.0383	21.5013	39.5321	60.4146
0.800	13.4202	22.5694	39.8726	61.2269
0.750	14.3501	22.8389	40.2547	62.0705
0.725	14.8955	23.4178	40.9432	62.0796
0.700	15.2552	24.3045	41.3125	62.7213
0.650	16.1434	24.9320	41.7658	63.2394
0.625	16.6702	25.6596	42.4325	64.1026
0.600	17.0195	26.4618	42.8654	64.6620

Table 7. Variations of THD with modulation index.

Modulation index	Output voltage THD (%)	Output current THD (%)
1	9.64	3.08
0.950	10.86	3.32
0.925	11.53	4.09
0.900	12.77	4.33
0.850	12.48	5.20
0.825	12.42	4.61
0.800	12.25	4.15
0.750	12.92	3.94
0.725	13.77	4.44
0.700	14.61	5.02
0.650	17.68	5.88
0.625	19.57	5.92
0.600	18.36	6.53

THD, total harmonic distortion.



```
Sampling time      = 5e-05 s
Samples per cycle = 400
DC component       = 1.108e-07
Fundamental        = 46.98 peak (33.22 rms)
THD                = 10.86%

     0 Hz   (DC):          0.00%     90.0°
    25 Hz                  0.00%    160.3°
    50 Hz   (Fnd):       100.00%    178.2°
    75 Hz                  0.00%    198.3°
   100 Hz   (h2):          0.00%    266.5°
   125 Hz                  0.00%     -1.9°
   150 Hz   (h3):          2.03%     -5.4°
   175 Hz                  0.00%    259.0°
   200 Hz   (h4):          0.00%      0.0°
   225 Hz                  0.00%    214.5°
   250 Hz   (h5):          2.03%    171.0°
   275 Hz                  0.00%    -85.3°
   300 Hz   (h6):          0.00%    259.3°
   325 Hz                  0.00%    268.7°
   350 Hz   (h7):          2.26%    -12.6°
   375 Hz                  0.00%    -10.8°
   400 Hz   (h8):          0.00%    255.7°
```

(a)

```
Sampling time      = 5e-05 s
Samples per cycle = 400
DC component       = 1.165e-06
Fundamental        = 4.556 peak (3.222 rms)
THD                = 3.32%

     0 Hz   (DC):          0.00%     90.0°
    25 Hz                  0.00%     -0.8°
    50 Hz   (Fnd):       100.00%    164.1°
    75 Hz                  0.00%    177.3°
   100 Hz   (h2):          0.00%     86.5°
   125 Hz                  0.00%     -4.5°
   150 Hz   (h3):          1.67%    -42.2°
   175 Hz                  0.00%    173.7°
   200 Hz   (h4):          0.00%     82.8°
   225 Hz                  0.00%     -8.1°
   250 Hz   (h5):          1.30%    119.4°
   275 Hz                  0.00%    170.1°
   300 Hz   (h6):          0.00%     79.2°
   325 Hz                  0.00%    -11.7°
   350 Hz   (h7):          1.15%    -72.9°
   375 Hz                  0.00%    166.5°
   400 Hz   (h8):          0.00%     75.6°
```

(b)

Figure 8. (a) THD analysis of output voltage of nine-level RSSS MLI. (b) THD analysis of output current of nine level RSSS MLI. MLI, multilevel inverter; RSSS, reduced switch single source; THD, total harmonic distortion.

6. Experimental Response

In order to investigate the capabilities of proposed RSSS MLI, an experimental setup based on digital signal processor (DSP) Dspace (CP1104) is created. Figure 9 shows a picture of prototype configuration. Dspace (CP1104) controller board has been used which is cost-effective single-board system for controller development. It upgrades a PC to a development system for rapid control prototyping. The board can be installed in any PC with a free peripheral component interconnect (PCI) or peripheral component interconnect express (PCIe) slot. Therefore, Dspace (CP1104) is used as interconnection between prototype and computer programming so that controlling should be done by PC and signals sent through Dspace to the prototype.

The experimental data is recorded using a Tektronix (TPS2014B) 4-channel digital oscilloscope and a FlukeView (43B) single-phase power quality analyzer. Tektronix digital oscilloscope offers a distinctive range of capabilities in an oscilloscope with controls and menus. It is available in two or four channel version with isolated channel that provides isolation from ground and isolation between channels, allowing us to take measurements with less worry about damaging circuitry. In this prototype, four channel TPS2014B digital oscilloscope is used to visualise the output voltage waveform of different levels from the inverter output. The test has been carried out for different load conditions, such as resistive load (R-load) and RL-load. Also, FlukeView (43B) has been used to record the current and power waveform during different load conditions. The FlukeView power quality analyzer performs the measurements we need to maintain power systems, troubleshoot power problems and diagnose equipment failures. All the power and current signal measurements are done by using this and data are saved.

Four DC battery source (Chloride SafePower Lead Acid) are used in nine level RSSS MLI which are rated as 12.6 V–12.8 V. Eight IGBT/MOSFET modules (1,200 V/40 A) have been used out which four are in PGU unit and four are in LGU unit. In LGU unit, two IGBT/MOSFET modules are bidirectional as per the proposed RSSS MLI. The switching of RSSS MLI has been done at angles of $\theta_1 = 0.1717$, $\theta_2 = 0.3557$, $\theta_3 = 0.6703$ and $\theta_4 = 1.054$ at modulation index 0.95. The operation of this MLI is analysed under different condition such as without load, with R-load only and with RL-load. In industries these are the three different possible conditions of load that's why these are used to validate and test the results of RSSS MLI. When the RSSS MLI tested under this condition, it can produce the desired voltage level at the output i.e. nine level and the current across the load is measured by FlukeView.

6.1. Without load

The output voltage of nine level RSSS MLI is shown in Figure 10a. This MLI is able to achieve its all level at a modulation index of 0.95. The peak value of voltage is 40 V and RMS voltage is 34.10 V. THD content in output voltage is shown in Figure 10b. THD of output voltage is 8.4% and fifth and seventh harmonics contents are 1.1% and 1.5% respectively.

6.2. With R-load

In this case, a R-load of 20 Ω is connected across the RSSS MLI. For this, a rheostat (0–100Ω) is used, which is set at 20 Ω. The output voltage achieves its all nine level by attending a peak value of 40 V and RMS value of 27.97 V.

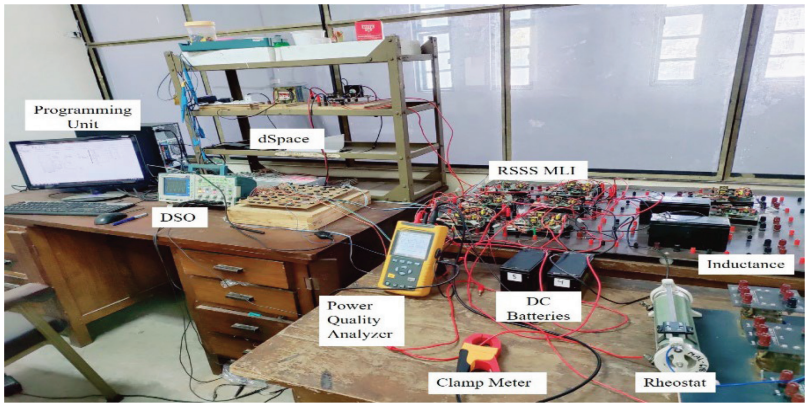


Figure 9. Hardware setup of proposed work. MLI, multilevel inverter; RSSS, reduced switch single source.

The current after applying load is 1.392 A. Both the waveforms of voltage and current is shown in Figure 11a. Also, power is calculated with these parameters, which is equal to 38.8 W and shown into Figure 11b. THD of output voltage is 9.9% and that of current is 9.8%, which are portrayed into Figures 12a and 12b, respectively. The fifth and seventh harmonic contents of output voltage is 1.3% and 1.5%, respectively.

6.3. With RL-load

A load of R = 10 Ω and L = 20 mH is connected across the MLI. Peak value of 40 V and RMS value of 28.48 V are obtained by the nine level MLI. Current value of 1.883 A is measured through the load. Both the waveforms are shown in Figure 13a. In the power calculation, active power of 40.9 W, reactive power of 34.3 VAR, apparent power of 53.4 VA and power factor of 0.77 are obtained which is portrayed in Figure 13b. Figure 14a displays THD of output voltage, which is 12.5%, whereas Figure 14b displays THD of output current, which is 3.4%. From this, the fifth and seventh harmonic contents of output voltage is 1.2% and 1.5%, respectively.

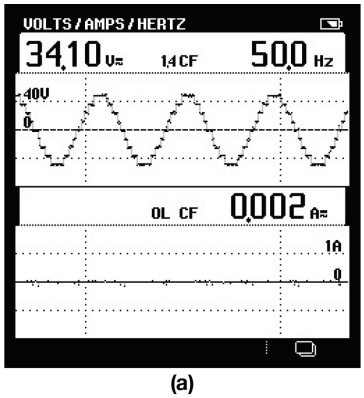
The THD is calculated for both current and voltage at the output to check the fifth and seventh harmonic contents. Under IEEE-519 standards, the allowable limit of fifth and seventh harmonic content is under 2%. Therefore, from the above parameters, we can see that the fifth harmonic content is in the range of 1.1%–1.3% and that of seventh harmonic content is 1.5% of RSSS MLI, which meets the IEEE-519 standards.

From the above presented results for proposed nine-level inverter, its seen as experimental and simulation outcomes are in near agreement and hence validate the simulation results as well as the validity of this topology with SHE-GA. The Voltage THD of nine-level MLI comes 10.86% with simulation, while it comes 12.5% with experimental result for RL-load. Similarly, for Current THD, it comes 3.32% with simulation while it comes 3.4% with experimental results. Talking about fifth and seventh harmonics, they are 1.3% and 1.15% respectively with simulation and 1.2% and 1.5% respectively with experimental results. In both cases, they are below 2%, which comes in IEEE-519 standards.

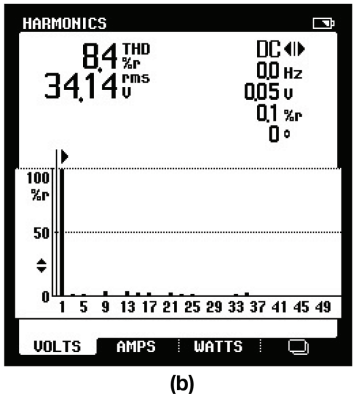
7. Conclusions

This paper presented a novel RSSS MLI topology aimed at reducing circuit complexity, switch count and TSV while maintaining high-quality output voltage. The proposed topology employs a modular structure consisting of LGUs and a PGU, enabling easy scalability to higher voltage levels with a reduced number of power electronic components.

To improve power quality at low switching frequency, a GA-SHE strategy was implemented to compute optimal switching angles for a nine-level RSSS MLI. The proposed modulation technique effectively suppressed dominant lower-order harmonics, particularly the fifth and seventh harmonics, while preserving the fundamental voltage component. Comparative analysis demonstrated that the proposed RSSS MLI requires fewer switches and exhibits lower TSV than several recently reported MLI topologies, making it a cost-effective solution for practical applications.

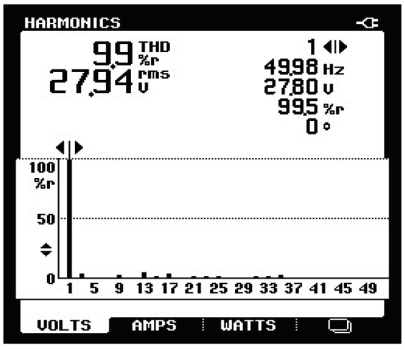


(a)

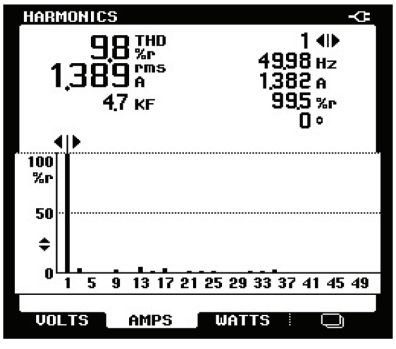


(b)

Figure 10. (a) Output voltage without load. (b) THD analysis without load. THD, total harmonic distortion.

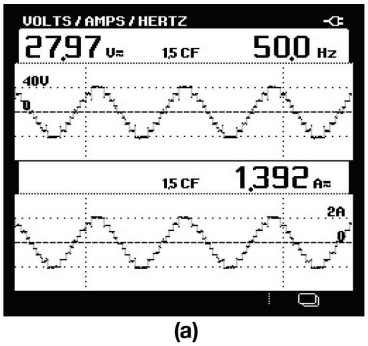


(a)

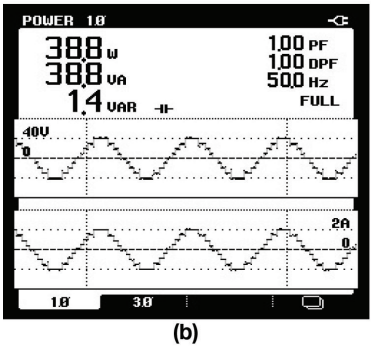


(b)

Figure 12. (a) THD analysis of output voltage with R-load. (b) THD analysis of output current with R-load. R-load, resistive load; THD, total harmonic distortion.

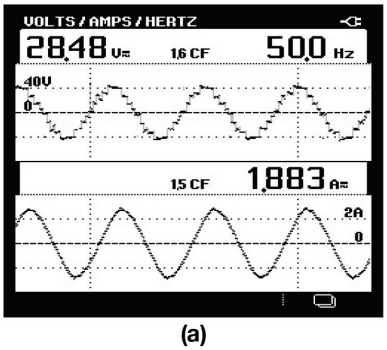


(a)

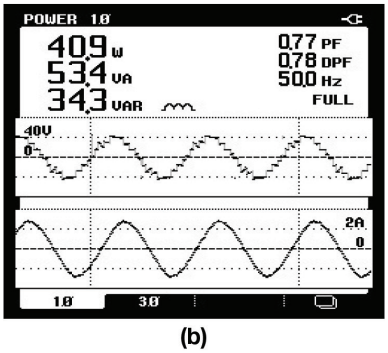


(b)

Figure 11. (a) Output voltage with R-load. (b) Output power with R-load. R-load, resistive load.

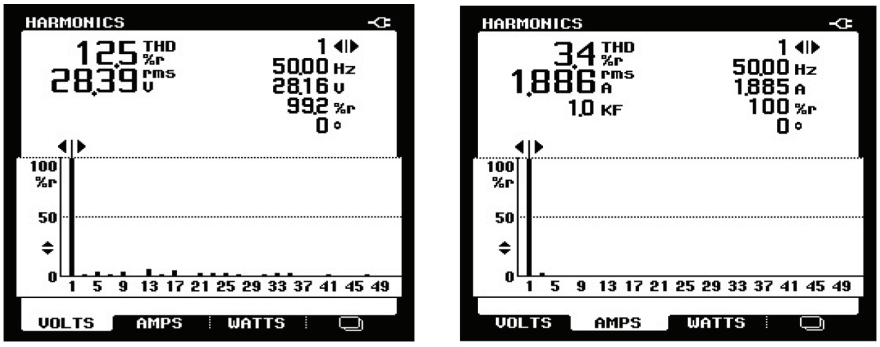


(a)



(b)

Figure 13. (a) Output voltage with RL-load. (b) Output power with RL-load. RL-load, resistive–inductive load.



(a) (b)

Figure 14. (a) THD analysis of output voltage with RL-load. (b) THD analysis of output current with RL-load. RL-load, resistive–inductive load; THD, total harmonic distortion.

The performance of the proposed inverter was validated through MATLAB/Simulink simulations and real-time experimental implementation using a dSPACE CP1104 controller. Experimental results under no-load, R-load and RL-load conditions confirmed that the RSSS MLI is capable of generating all intended voltage levels with acceptable voltage and current waveforms. The measured harmonic distortion levels complied with IEEE-519 standards, with the fifth and seventh harmonic components maintained well below the prescribed limits.

The modular structure of the proposed RSSS inverter allows straightforward extension to three-phase systems by integrating three identical inverter legs. This makes the topology suitable for grid-connected renewable energy systems and motor drive applications. Furthermore, harmonic analysis demonstrates that the dominant harmonic components remain within the limits specified by the IEEE-519 standard, ensuring compatibility with modern grid codes.

Overall, the proposed RSSS MLI topology combined with the GA-SHE control strategy demonstrates strong potential for power electronics and drive applications, particularly in renewable energy systems and medium-power industrial drives where reduced component count, lower switching losses and improved power quality are critical. Future work may focus on extending the proposed topology to higher voltage levels and investigating its performance under grid-connected and dynamic load conditions.

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