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An Improved and Efficient High-Boost Switched Capacitor Multilevel Inverter

Research Paper

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Abstract: This paper presents a fundamental nine-level switched-capacitor multilevel inverter (CSMLI) powered by a single DC source. The configuration employs two capacitors, nine switches, and one diode to generate nine distinct output voltage levels. It achieves an inherent voltage-boosting capability of up to four times the input voltage. The switched-CSMLI represents an enhanced topology that utilises a strategic switching scheme to guarantee adequate capacitor charging and natural voltage balancing. The circuit adopts a novel charging approach that increases the number of charging states, thereby maintaining sufficient stored charge across the capacitors. An extended version of the basic CSMLI structure is also introduced to further increase the number of discrete output voltage levels. The proposed topology is evaluated against other comparable state-of-the-art inverters to demonstrate its advantages and effectiveness. The base configuration delivers improved harmonic performance and requires relatively small passive LC (inductor-capacitor) filters for harmonic mitigation. Simulation studies are conducted using the Power simulation (PSIM) platform, and a hardware prototype is developed to experimentally verify the performance and validate the proposed design.

Keywords: *capacitor switched • high-boost • multilevel inverter • sinusoidal pulse width modulation • total harmonic distortion*

1. Introduction

Renewable sources nowadays are quite lucrative option for harnessing energy. However, these sources require suitable power electronic converters to produce high-quality power (Hosseinpour et al., 2024; Seifi et al., 2024). Distributed generation offers advantages like reduced power conversion losses, reduced transmission losses, and lesser reactive power issues. The conventional inverters (two-level type) require bulk filters to compensate harmonics. So, many conventional inverters have been replaced by multilevel inverters (MLI) (Anand et al., 2023a; Saif et al., 2025) because of its numerous advantages. MLIs are popular due to many reasons such as lesser total standing voltage (TSV) of switches, lower total harmonic distortion (THD), economic feasibility, and lesser electromagnetic interference (Anand et al., 2023a,b; Kar et al., 2024; Kar et al., 2023a,b). Three basic types of MLI topologies are diode-clamped (Anand et al., 2023a), flying capacitor type (Ben Smida and Ben Ammar, 2010), and cascaded H-bridge (Kouro et al., 2010; Rodriguez et al., 2009). Diode-clamped and flying capacitor-based MLIs required many components, especially diodes in case of diode-clamped and capacitors in case of flying capacitor model. Hence,

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employing these types of traditional MLI to furnish higher number of voltage levels becomes impractical. Moreover, the traditional diode clamp design gives voltage imbalance normally due to the use of dividing capacitors (Nabae et al., 1981).

Cascaded H-bridge, on other hand, requires a lot of independent voltage sources (Niu et al., 2020). Hence the task of building a robust MLI with reduced components, higher efficiency, lower-voltage stress across the circuit components is a big challenge. Much of the research work is in progress on 'switched capacitor multilevel inverter' (CSMLI). The compact design and requirement of very fewer voltage sources have made CSMLI quite popular. CSMLI topology can give an inherent boost which other types of MLI cannot give. This is a big advantage of CSMLI. Because of these advantages CSMLI topologies have becomes quite suitable for renewable energy source integration (Hassan et al., 2023), as renewable source gives low-voltage DC output. Use of single voltage source would require single charging circuit; hence for charging the circuit, the CSMLI presents a good option. Recently, several CSMLI have been proposed. Certain problems such as voltage imbalance, voltage ripple across capacitors, and deep discharge are not taken very seriously but need to be considered in the long run (Azimi et al., 2020; Panda et al., 2021). MLIs described in Hosseinzadeh et al. (2022) use Ampere's second rule of charging to avoid inrush capacitor current, but in order to do so, the boost factor should be compromised to just one. Raman et al. (2019) use two DC sources, two capacitors, nine switches, and three power diodes to constitute a nine-level MLI. As can be seen, the component count is high, and, additionally, it uses two independent DC sources. Azimi et al. (2020) also use higher component count to realise a 13-level MLI. The voltage boost in Raman et al. (2019) and Sandeep and Yaragatti (2018) is just equivalent to one. Abdel-Rahim and Wang (2020) produce a five-level MLI with one capacitor and one DC-voltage source. Here too, component count is more with respect to the number of voltage levels it can produce and comparatively poor utilisation of capacitor voltage to produce voltage levels. Sarwer et al. (2020) use two DC sources and a capacitor to form a seven-level MLI with eight switches offering a boost factor of 2. Roy et al. (2021), on other hand, give three times the boost factor; however it needs numerous switches. Siddique et al. (2023) propose a nine-level MLI (neutral-clamped) with two times boost factor. The MLI in Kumari et al. (2021) is a nine-level MLI with a boost factor of two times. However, (Kumari et al., 2021; Roy et al., 2021; Sarwer et al., 2020; Siddique et al., 2023) use comparatively higher number of components with respect to the number of voltage levels it can generate. Iqbal et al. (2021a) offer quadruple boost but still the component count is high.

The proposed work gives a nine-level MLI topology with a single DC source as its basic topology. Suitable extended versions can give much higher levels. Following points highlight the merit of both the proposed CSMLI topology.

1. It consists of optimal number of components.
2. A unique switching strategy ensures optimum charging and balance of capacitor voltage in CSMLI topology by Allowing more charging points to ensure lesser capacitor voltage ripple in CSMLI topology.
3. It offers high boost (four times) at output terminal of CSMLI topology.
4. The topology offers superior efficiency.
5. The basic model can be easily extended for higher levels and also for three-phase networks.

Section 2 describes the overall circuit topologies and their operation. It describes the design aspects, specifying the factors that determine the choice of components. Section 4 shows vivid comparison of the proposed model with other existing similar CSMLI models. Section 5 discusses simulation and experimental results. Section 6 depicts suitable ways of extending the circuit to produce higher number of voltage levels. Finally, the paper ends with the concluding section.

2. Circuit Architecture

2.1. Circuit architecture of the proposed CSMLI

Figure 1 describes the proposed nine-level CSMLI. The basic module (BM) consists of one DC source, two capacitors, nine switches, and a diode. Out of the two capacitors, one is charged up-to 1 pu (per unit). Then, the series combination of this capacitor and input DC is applied across the other capacitor and is charged up to 2 pu. Here, 1 pu is equal to the value of the input DC source. Both the capacitors, along with the input DC source, can produce a total of four distinct voltage levels. All switches can be of any type, either MOSFET, power transistor,

or IGBT (insulated gate bi-polar transistor), except for switch *S*4, which needs to be unidirectional strictly. Hence for switch *S*4, any typical reverse block IGBT (RB-IGBT) is used. The remaining switches are MOSFETs. Switch *S*5, connected in antiparallel configuration, is included in the circuit to facilitate reactive power flow during the first voltage level. Figure 2 describes the conduction and charging paths undertaken during various voltage levels. Referring Figure 2c the H-bridge is for polarity reversal and is not playing any role in producing active voltage levels of the inverter. Figure 3 shows the status of level-generating circuit during freewheeling state, and Table 1 shows the switching states during each voltage level along with the status of capacitors. The terms 'C' and 'D' denote charging and discharging. The switches H1 and H4 are in the on-state to produce positive half-cycle, and during the negative half-cycle, H2 and H3 will be on and H1 and H4 will be in off-state. For the voltage level 0 or freewheeling state, H1 and H2 will be in the on-state, and H3 and H4 will be in the off-state. The level 0 is not generated from level-generating circuit, rather it is generated by the H-bridge. During this period, capacitor *C*2 can be charged with the help of DC source and capacitor *C*1.

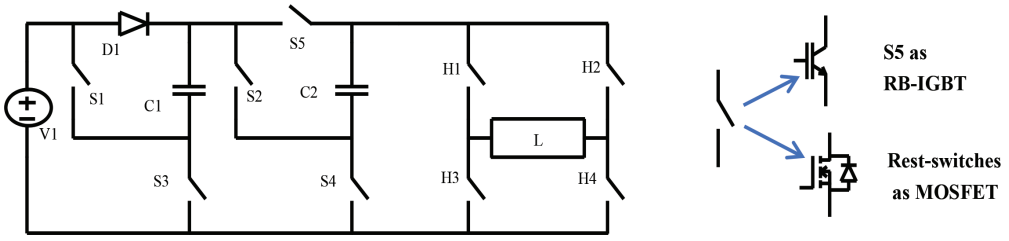

Figure 1. Schematic diagram details of proposed CSMLI. CSMLI, switched capacitor multilevel inverter; RB-IGBT, reverse block IGBT.

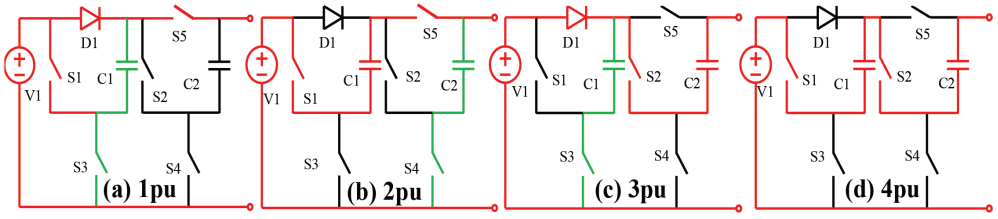

Figure 2. Mode diagram for all active voltage levels (red is conduction path, green is charging path and black is non-conducting). (a) Mode diagram during 1 pu. (b) Mode diagram during 2 pu. (c) Mode diagram during 3 pu (d) Mode diagram during 4 pu.

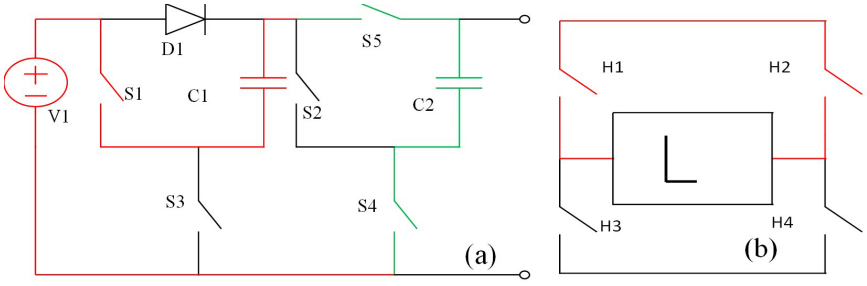

Figure 3. Mode 0th state for (a) level-generating circuit (b) H-bridge.

Table 1. Switching states and capacitor status (positive half).

Switching states of the switches in level-generating circuit					H-bridge				Capacitor status		Output voltage
*S*1	*S*2	*S*3	*S*4	*S*5	H1	H2	H3	H4	*C*1	*C*2	Levels
1	0	0	1	0	1	1	0	0	D	C	0 pu
0	0	1	0	1	1	0	0	1	C	-	1 pu
1	0	0	1	0	1	0	0	1	D	C	2 pu
0	1	1	0	0	1	0	0	1	C	D	3 pu
1	0	1	0	0	1	0	0	1	D	D	4 pu

2.2. Switching strategy and charging problem with *C*2

During conduction, *C*1 gradually losses its charge and hence its voltage level droops. Because *C*2 is charged from both a fixed DC source and a variable DC source in the form of a capacitor, complete charging of *C*2 cannot be achieved in a single step. This scenario is graphically shown in Figures 4a and 4b. Hence, *C*2 will never get charged to 2 pu of voltage in one step. For *C*2 to get charged very close to 2 pu voltage, it needs repeated charging. During 2 pu-voltage level at output, (refer Figure 2b) *C*2 is charged with input DC and capacitor *C*1 in series. However, here, the input DC and capacitor *C*1 equally supply the load, and charging *C*2 during this time will not charge it to 2 pu. Moreover, as observed from the simulation results, the voltage of *C*1 during 2 pu level droops at higher rate, for which *C*1 demands a higher capacitance value. During the voltage 0 level, the H-bridge gets disconnected from the load, and both the capacitors are idle. Now, charging *C*2 can be initiated, but the 0th instance remains for a very short time. So, it can be observed that charging *C*2 would be a challenge.

In summary, the factors that make charging capacitor *C*2 challenging are identified.

(1) Except at the 0 level of the output voltage, there is no instant at which both capacitors are relaxed and can be completely engaged in charging.
(2) The level 0 also prevails for a very short period of time. Hence, within that period, the desired level of charging both the capacitors is a challenge.
(3) The charging paths of the capacitors will have substantial internal resistance and internal inductance. This makes the RC time constant high and the overall charging time of the capacitors.

2.3. Solution of charging capacitor *C*2

A unique way of using modulation technique can help overcome this problem. For the proposed circuit, variable frequency multi-carrier sinusoidal pulse width modulation (VF-MC-SPWM) is used. The VF-MC-SPWM serves two purposes in the proposed topology.

(1) Shaping the multi-stepped raw output into near sinusoidal.
(2) Creating more freewheeling instants for better charging of the capacitors (Figure 4b).

The first point is clear and a popular example of high-frequency modulation used in most of the inverter design. The reason is to raise high-frequency components and filter with small filters. The second point needs explanation. During 1 pu-voltage level, the SPWM modulation makes the output voltage magnitude switch to and from between 1 pu and 0 pu. This produces a greater number of freewheeling or 0 pu instants (Figure 4b), and hence there is a chance of initiating charging of both the capacitors. Figure 4b describes the scene with VF-MC-SPWM. During 1 pu, *C*1 can be charged, and at 0th instant, *C*2 can be charged. The carrier frequency corresponding to the 1 pu-voltage level is set higher to get greater number of charging points. The other carrier frequencies may be specified at comparatively lower frequency, keeping in view the switching losses. Table 2 shows the charging cycle of capacitors during 1 pu level of voltage prevalence. This process greatly enhances the sufficiency of charging for capacitor *C*2, thereby improving the voltage profile and the stability of capacitor *C*2.

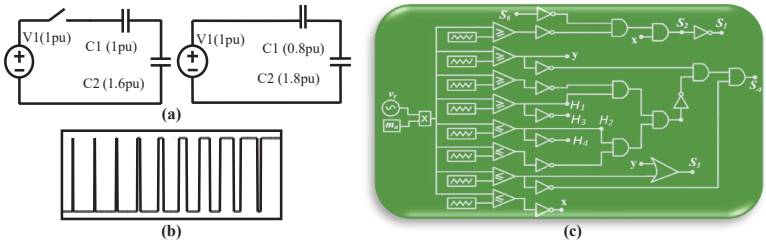

Figure 4. (a) An example of instant voltage status of both capacitors during normal operation. (b) Typical SPWM output during 1 pu-voltage level, where upper band is 1 pu and lower band is 0 pu. (c) Logic circuitry for generating gate pulse for all switches.

Table 2. Modified-switching states and capacitor status (during 1 pu).

Switching states of the switches in level-generating circuit					H-bridge			Capacitor status		Output voltage
*S*1	*S*2	*S*3	*S*4	*S*5	H1	H2	H4	*C*1	*C*2	Levels
0	0	1	0	1	1	0	1	C	-	1 pu
1	0	0	1	0	1	1	0	D	C	0 pu
0	0	1	0	1	1	0	1	C	-	1 pu
1	0	0	1	0	1	1	0	D	C	0 pu

2.4. Gating pulses generation

The level-shifted multi-carrier pulse width modulation method is used to generate the switches' gate pulses. This is a popular high-frequency modulation used to minimize the lower-order harmonics in the output voltage and simultaneously increase the higher end frequency components centred around the switching frequency of the triangular source. It contains a 60 Hz-sinusoidal reference signal in the form of $V_p(\sin(\omega t))$ as a dominant signal along with the high-frequency band of signals centredaround 3 kHz. This sine reference signal has been compared with all the triangular carrier signals whose peak-to-peak amplitude is one and the frequency is 3 kHz. Varying pulse width is generated by comparing the reference sine wave and the triangular signal, which is shown in the figure (Fig.4(b)). To acquire the switching state as per Tables 1 and 2, the logic circuitry is depicted in Fig.4(c). The amplitude of the N-Level inverter's output voltage is directly proportional to the modulation index (Ma), which can be expressed as Ma = 2 V_{pr} (N−1) V_{pp}, where V_{pp} indicates the peak-to-peak value of the carrier signal.

2.5. Solar photo-voltaic (PV) applicability

The proposed topology will be of great use as an isolated solar microgrid for domestic purpose. This MLI gives an inherent boost of four times and does not require any boosting circuit. A PV panel of DC voltage of 36–40 V as input when switched with 60 Hz will produce an output sine with approximately of 110 V (rms), 60 Hz. This is a standard voltage-frequency utility coordinate in most of the countries. Apart from that, it can be a good way of interfacing directly with solar or any other suitable form of renewable energy, utilising renewable sources without any additional power stages in-between. With higher input DC, the boosted output voltage can be fed directly to grid, thus forming an effective grid-free or off-grid mode DC-AC converter.

2.6. Reactive power flow

The proposed topology allows the feedback during four distinct levels, namely 0 pu, 2 pu, 3 pu, and 4 pu. The feedback of current from source to load is a critical factor while considering the smooth conduction of reactive load of low power factor. The description of path undertaken during each level is given below. The H-bridge with four antiparallel diodes act like a diode bridge rectifier in reverse direction. So, a H-bridge can conduct load current in reverse direction without any problem. Keeping this fact in mind, the path undertaken during each level is described below.

0 Level (0 pu) – Taken care by the H-bridge itself. Switching on the two adjacent switches of H-bridge creates a freewheeling instance for the load current that traces one of the switches and the body diode of the other, comfortably in both the direction.

1. **Level (1 pu) –** The load current goes from the H-bridge through switch *S*5, then through capacitor *C*1, switch *S*3, and all the way back to the H-bridge.
2. **Level (2 pu) –** The reactive load current from the load flows via the antiparallel diodes of H-bridge switches towards the level-generating circuit. The load current then flows via *C*2 in the opposite direction and then via switch *S*4 back to the H-bridge.
3. **Level (3 pu) –** The reactive load current from load flows via antiparallel diodes of switches of the H-bridge towards the level-generating circuit. The load current then flows all the way via *C*2 in the opposite direction and then via the body diode of switch *S*3, tracing *C*1 in the reverse direction all the way via charging switch *S*2 and back to the H-bridge.
4. **Level (4 pu) –** The reactive load current from load flows via antiparallel diodes of switches of the H-bridge towards the level-generating circuit. The load current then flows via *C*2 in the opposite direction and then via the body diode of switch *S*3, tracing *C*1 in the reverse direction and then via the body diode of switch *S*1, tracing V_1 and finally back to the H-bridge.

Alternative for 1 Level (1 pu) – The non-availability of feedback path for 1 pu level may create problem for reactive power flow. However, from the simulation results and the experimental results, it is confirmed that a shunt filter capacitor can easily manage the reactive power flow smoothly for even very low factor loads. The use of shunt filter is necessary as the high-frequency modulation needs a filter to filter out the high-frequency harmonics. This shunt filter equally takes care of the low power-factor load. In results section, this will be proved with all necessary results. In order to create a feedback path for 1 pu, extra switch(s) are required, which will increase the cost. As far as just one missing level is concerned, the shunt capacitor is sufficient to manage the reactive power flow.

3. Design Aspect

Choice of proper components and ensuring their ratings are crucial for proper functioning of the proposed topology.

3.1. Diode and switch design (for both switched-diode and switched-capacitor models)

The forward voltage drops, and the dynamic resistance of the diode decides the capacitor voltage profile and is a crucial factor in deciding the optimal performance of the proposed topology. The charging path of both the capacitors will have the diodes in their path. Hence, it is desired to have a low forward-voltage drop and low dynamic on-state resistance. The TSV and average current of diodes D_1 and D_2 are as follows.

$$V_{S3} = V_{S1} = V_{D1} = V_{in} \tag{1}$$

$$V_{S4} = V_{S2} = V_{S5} = 2\ V_{in} \tag{2}$$

$$I_{D1} = 2\left(\int_{t1}^{t2}(I_L)\sin(wt).dt + \int_{t3}^{t4}(I_L)\sin(wt).dt\right) \tag{3}$$

$$I_{D2} = 2\left(\int_{t1}^{t3}(I_L)\sin(wt).dt\right) \tag{4}$$

Where V_{D1}, V_{S1}, V_{S2}, V_{S3}, and V_{S4} are TSV of diode D_1 and switches $S1$, $S2$, $S3$, and $S4$. V_{in} is the input DC voltage. I_{D1} and I_{D2} are the average diode currents of D_1 and D_2. I_L is the peak value of load current. The time snaps like t_0, t_1, t_2, t_3, and t_4 define the time at which the voltage level goes to 0 pu, 1 pu, 2 pu, 3 pu, and 4 pu, respectively. Any suitable Schottky diode such as SR360 (60 V, 3 amps) has low drop and low resistance, so can be a potential choice. The diode TSV is comparatively less; hence, for most of the lower- and medium-voltage application, the peak inverse voltage range of Schottky diode will fit. Schottky diodes can handle 3–5 amps of current (rms) and up to 30 A of surge current for 8 ms (approx.) and 70 amps for 4 ms. The charging inrush current can be well adjusted within these limits. For higher load, more than one such diode can be connected in parallel. For switches also, similar scenario follows. The TSV of switches $S1$ and $S3$ is V_{in} whereas TSV of $S3$, $S4$, and $S5$ is 2 V_{in}. The topology design ensures minimum TSV to all level-generating switches. Hence, a low-voltage or medium-voltage switch with high current capability will give effective performance. Switches such as IRF series MOSFET offer low impedance and very low voltage drop. For both switches and diodes, on-state resistance and low voltage drop are important for the performance of the proposed topology.

3.2. Capacitors selection (switched-capacitor model)

Capacitor selection is based on two points: the charging and the discharging instants. Discharging instant is dependent on load current and its conduction time until next recharge. The charging time depends on the path resistance and the total amount of charging time available. Capacitor $C1$ discharge is maximum during 4 pu-voltage level. At 3 pu, it gets recharged (refer to Table 1). So, the discharge amount will be

$$\Delta Q_{C1} = \int_{t4}^{t4'} I_L \sin(wt).dt \tag{5}$$

$$\Delta Q_{C1} = (C1)(\Delta V_1) \tag{6}$$

During 4th level band of output voltage, the voltage swings between 3 pu and 4 pu. During 3 pu-voltage level, *C*1 gets tikling recharge, where the voltage level in *C*1 improves to an extent. This voltage gain needs to be accounted.

$$A_{r2} = 4\int_{t4}^{t4'} \sin(wt).(dt) \tag{7}$$

$$1.(\Delta t_4) = A_{r2} \tag{8}$$

$$\Delta t_3 = (t4' - t4) - \Delta t_4 \tag{9}$$

The term 'IL' represents the peak value of load current. The amount of charge lost is shown in black region in Figure 5, which is computed in Eq. (7). 'Ar2' represents that area. The scripts *t*4 and *t*4` denote the starting and ending time of 4th voltage-level band. Δt_4 and Δt_3 are average estimated time for which 4 pu and 3 pu level prevails. The amount of time for which 4 pu level prevails can be approximated according to Eq. (8). From this, the effective amount of time for which 3 pu level prevails can be approximated according to Eq. (9). Next, considering a maximum allowable voltage ripple of *C*1 as ΔV_1^*using the transient state equation, the following relation can be established, where R_d and R_s are switch and diode resistance. ΔV_1^* is the maximum allowable voltage droop (for *C*1), which can be chosen as 5% or 10% of the final steady state voltage achievable. ΔV_1 is the voltage ripple of *C*1, produced while conducting load current during 4 pu voltage level, and it can be calculated according to Eq. (6). ΔV_1^* is user-defined. ΔV_2 is the voltage ripple of *C*2. Point to be noted is that if *C*1 functions perfect at 4 pu-voltage level, then it will definitely function well during other voltage levels because 4 pu-voltage level gives the highest current and causes maximum discharge.

$$1 - \Delta V_1^* = 1 + \left\{(1 - \Delta V_1) - 1\right\} e^{-\Delta t_3/(R_d + R_s)C1} \tag{10}$$

Simplifying the equation

$$\frac{\Delta V_1^*}{\Delta V_1} = e^{\frac{\Delta t_3}{(R_d + R_s)C1}} \tag{11}$$

For estimating capacitor *C*2, similar steps can be followed. *C*2 goes on a continuous conduction mode during 3 pu and 4 pu with no intermittent charging in between. So, discharge amount for *C*2 can be calculated as

$$\Delta Q_{C2} = \int_{t3}^{t3'} I_L \sin(wt).dt \tag{12}$$

$$\Delta Q_{C2} = (C2)(\Delta V_2) \tag{13}$$

Charging of *C*2 takes place during 2 pu-voltage level but complete charging cannot take place as during the same time, and a significant proportion of capacitor charge goes to the load as well. Hence, charge gained during 2 pu level is ignored. Full charging of *C*2 can take place during 1 pu-voltage level when the voltage level swings to 0 pu (refer Figure 4). Necessary equations to work out while charging *C*2 are as follows

$$A_{r1} = \int_{t0}^{t1} \sin(wt).(dt) \tag{14}$$

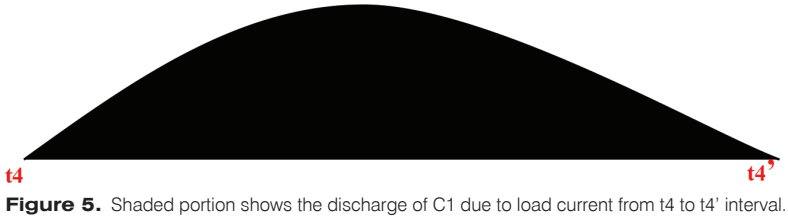

Figure 5. Shaded portion shows the discharge of C1 due to load current from t4 to t4' interval.

$$1.(\Delta t_1) = A_{r1}. \tag{15}$$

$$\Delta T_0 = (t1 - t0) - \Delta t_1. \tag{16}$$

Ar1 represents area of conduction during 1 pu-voltage level Eq. (7). 'Δt_1' and 'Δt_1' represent averaged estimated time for which 1 pu- and 0 pu-voltage levels prevail.

$$2 - \Delta V_2^* = 2 + \left\{(2 - \Delta V_2) - 2\right\} e^{-\Delta T_0/(R_d + 2R_s)C1} \tag{17}$$

Simplifying the equation

$$\frac{\Delta V_2^*}{\Delta V_2} = e^{\frac{\Delta T_0}{(R_d + 2R_s)C1}}. \tag{18}$$

where ΔV_2^* is the maximum allowable voltage droop (for *C*2) which needs to be chosen according to the application or the user's interest.

4. Comparative Analysis

A rigorous comparison with recently published and similar work is carried out and presented in detail to prove the merit of the circuit. Table 3 displays comparison with respect to the number of components and the device count. Table 4 shows comparison based on the performance parameters. The notations used in Table 3 such as N_L and N_v denote number of levels and number of DC-voltage sources. The terms N_s, N_d, and N_c denote the total number of switches, diodes, and capacitors used. The term T means topologies. In Table 4, the term K means boosting factor. The terms TSV and Fc TSV of all switches are in per unit and cost function, respectively. The cost function can be defined as follows.

$$F_c = \frac{\left\{2N_s + N_d + N_c + (TSV)\alpha\right\} N_v}{N_L} \left(\frac{1}{K}\right) \tag{19}$$

The term *α* in cost function denotes weightage factor of TSV with respect to the total number of the components used. At present, *α* value will be taken as 1 for easy and fair comparison. Alpha value >1 or <1 can be taken and a modified cost function can be designed for comparison for specific purposes. Two times *Ns* is taken to indicate switch and their gate driver circuit. Apart from the tabular comparison, a detailed analysis of the compared topology is presented. Sarwer et al. (2020) describe a seven-level MLI. One major problem with this MLI (Sarwer et al., 2020) is poor utilisation of DC source and capacitor voltage (Sarwer et al., 2020) use two DC sources of 1 pu each and a capacitor charged up to 2 pu. This combination could produce four discreet levels of voltage, but it can at the maximum produce three levels of voltage. This indicates poor utilisation of voltage cells and poor boost factor as well. The 3 pu-voltage level is supplied by the capacitor and one DC source in series. The capacitor with 2 pu-voltage supplies two times more power than the DC source. This will cause rapid discharge of the capacitor. The MLI in Roy et al. (2021) uses a high number of component count, especially switches. From Figures 2c and 2d of Roy et al.

Table 3. Comparison of device count.

T	N_L	N_v	N_s	N_d	Nc	Extension to higher levels
Sarwer et al. (2020)	7	2	8	2	1	No mention
Roy et al. (2021)	7	1	9	2	3	No mention
Iqbal et al. (2021b)	9	1	10	1	2	No mention
Panda et al. (2023)	9	1	10	3	2	Yes
Barzegarkhoo et al. (2021)	9	1	14	0	4	Yes
Sathik (2024)	9	1	10	2	5	No mention
[P]	9	1	9	1	2	Yes

Table 4. Comparison of performance.

T	K	TSV	Fc	Ripple loss (W)	Conduction loss (W)	Efficiency (%)	Remarks
Sarwer et al. (2020)	1.5	14	6.28	1.75	0.35	94.1	Poor use of capacitor voltage, multiple DC
Roy et al. (2021)	3	13	1.71	2.85	0.3	93.8	High conduction and switching loss
Iqbal et al. (2021b)	4	20	1.19	1.85	0.36	94.1	Capacitor instability
Panda et al. (2023)	4	18	1.19	1.91	0.42	93.1	Insufficient charge to capacitor
Barzegarkhoo et al. (2021)	4	24	1.5	3.96	0.41	91.2	Complex circuit, poor use of capacitors
Sathik (2024)	2	9	3.25	2.85	0.45	92.5	Low boost, high voltage droop
[P]	4	22	1.16	1.5	0.35	96.1	High TSV

TSV, total standing voltage.

(2021), it is observed that for 2 pu level, four switches and, for 3 pu level, a total of five switches are traced. Hence, at higher-voltage level, a greater number of switches are involved, and this will produce higher conduction loss. The MLI in Roy et al. (2021) also makes higher number of switching transition between consecutive voltage levels. This makes the switching technique complex and difficult to incorporate. Switching loss becomes pronounced for high-frequency modulation.

The next section describes the challenges and shortcoming of the comparative analysis in detail. MLI in Iqbal et al. (2021b) describes a nine-level inverter. High component count and complexity of the overall circuit assembly is a demerit. By analysing Figure 2 of Iqbal et al. (2021b), it can be observed that *C*2 is not getting properly charged. Except during 2 V_{dc}, level there is no other scope. During 2 V_{dc} level, the load also demands the power. The problem is clearly described in Section 2 under the subheading 'Switching Strategy and Charging Problem with *C*2'. Another mistake in the MLI (Iqbal et al., 2021b) is in the topology itself. Figure 2 of Iqbal et al. (2021b) shows the mode diagram, where it indicates if switch *S*9 is on then the current from capacitor *C*2 can get short-circuited via switch S9 and antiparallel diode of switch *S*10. Hence, this is a fundamental issue in Iqbal et al. (2021b), and under such condition, the circuit would fail to operate. MLI in Panda et al. (2023) makes a good try towards designing a nine-level quadruple boost MLI with optimum number of components. Panda et al. (2023) utilises the zeroth voltage level to charge capacitor *C*2 up to 2 pu. However, in one half cycle, there is only one such instant for *C*2 to get charged. Moreover, the duration of zeroth voltage level is very short. Hence, charging of *C*2 cannot be effective. During 2 pu-voltage level, the charging of *C*2 takes place, but it faces the same limitation as encountered by Iqbal et al. (2021b). The topology proposed by Panda et al. (2023) is restricted to a low-frequency-modulation technique; hence, additional charging states for *C*2 are not possible as proposed in the topology. MLI in Panda et al. (2023) also features its expandability, producing just two additional distinct voltage levels for four switches, two diodes, and one capacitor . Hence, such an extension is economically challenging for Panda et al. (2023) MLI. MLI in Barzegarkhoo et al. (2021) requires high device count as evident from Table 1. Barzegarkhoo et al. (2021) propose a five-level BM. Although Barzegarkhoo et al. (2021) claim a common ground formation as a big factor of novelty, many other parameters are compromised in their MLI. Eqs (1)–(9) of Barzegarkhoo et al. (2021) formulate necessary information for higher voltage levels. Analysing the equation, it can be realised that the extension to produce higher level is quite challenging both for circuit point of view and economically. A high switch count results in high conduction and switching losses. MLI in Barzegarkhoo et al. (2021) uses one DC source and two capacitors for five-level but boost factor is just two instead of three. It shows poor capacitor utilisation. Sathik (2024) describes a nine-level MLI. One of the demerits of Sathik (2024) MLI is that it uses a total of five capacitors and a DC source, but still voltage gain is limited to two. A higher number of capacitors leads to increased capacitor losses and reduced volumetric efficiency. From mode diagrams in Figure 3 of Sathik (2024), it can be observed that the DC source is not involved in supplying the load during any voltage level. The capacitors are solely supplying the load. This will create relatively higher voltage droop especially during the highest voltage level. Sathik (2024) is a clamped-type circuit and they have a natural demerit of capacitor voltage instability after prolonged use. On a comparative scale, the proposed topology design utilises minimum number of components to yield maximum boost with effective charging of capacitors, avoiding voltage imbalance or insufficient charge for capacitors to realise nine-level CSMLI. Based on this loss optimisation (especially ripple loss), the proposed topology shows a superior efficiency of 96% (Table 4).

5. Results and Discussion

For simulation, the components with specification are as follows. Capacitors of value 2,200 uF (*C*1) and 3,300 uF (*C*2) are taken. Input DC voltage of value 36 V is considered. The power and switching frequency are set at 60 Hz and 3 kHz, respectively. The following describes the steady-state outputs for the switched-capacitor model. Figure 6 shows output results under steady-state condition. It is worth noting that in Figure 6a, voltage droop during the topmost level is comparatively less with a load of 48 Ω. This is because *C*2 and *C*1 receive more charge with the unique switching technique. Figure 6b shows the respective voltage profile of capacitors *C*1 and *C*2. It can be seen that both capacitors more or less maintain a consistent flat voltage profile. Figure 6c shows output voltage and current for an R–L load of impedance 48 ∠ 45°Ω. Figure 6d shows the voltage profile of both the capacitors *C*1 and *C*2 and, as expected, both the voltage profile base remains nearly flat. Also, it can be seen that with inductive load, the load current becomes nearly sinusoidal with THD less than 3%. Figures 6e and 6f show the filtered waveform in the presence of LC filter (5 mH and 15 uF) for the resistive and inductive loads, respectively. In all the cases of filtered waveforms, the voltage and current THD remain below 5% limit, thus proving its usefulness in any possible grid application. Apart from these set of results, the test is also carried out for other types of loads with varying values of impedances with same value of LC filter. It has been observed the steady-state values of the waveforms not only are consistent but also give the THD content well below 5%. For example, for a set of resistive loads such as 30 Ω, 60 Ω, 100 Ω, 120 Ω, 150 Ω, and 200 Ω in the presence of LC filter, both steady-state current and voltage values show consistent performance giving a net THD in the range 3%–4%. Similarly, a set of inductive loads is also tested at its best to prove the usefulness of the circuit. For example, for a set of diverse inductive loads with varying impedance and power factor, angle like 15 ∠ 20°Ω, 30 ∠ 45°Ω, 60 ∠ 30°Ω, 90 ∠ 45°Ω, 120 ∠ 45°Ω, and 150 ∠ 65°Ω. were put to test the performance. It was observed that the load current steady-state value is nearly sinusoidal due to inherent filtering effect of inductive load in addition to the external LC filter giving THD in the range of 1%–2%. The output voltage for inductive loads showed THD values that were consistent with the limit of less than the 5% mark. The next set of figures shows the circuit performance under transient condition. Figure 7a shows the output wave performance in case of modulation index change (MI) from 0.95 to 0.6, in the presence of a resistive load of 60 Ω with LC filter. The point *D* marked in red colour shows the point of disturbance. It can be seen that both voltage and current comply perfectly to the change. Figure 7b shows the scenario of disturbance like former with another added-frequency change effect at the point of disturbance. Figure 7c shows two disturbances at two different points, D_1 and D_2. D_1 corresponds to MI change and frequency change instant (as in Figure 7b) and D_2 corresponds to load change instant. During D_2 point, the load changes from R–L (30 ∠ 40°Ω.) to 32 Ω R load. It can be seen that all waveforms maintain their consistency and synchronism with the load current. Thus, the performance confirms the robustness of the proposed topology. Hence, with successful confirmation of simulation results, the hardware validation can begin. The next section shows the performance of the proposed. topology in terms of an inbuilt laboratory-based utility scale model. For designing a utility-based hardware model proper choice of component is very important. For switches *S*1, *S*2, *S*3, *S*4, and *S*5 IRF540 (100 V, 25 A) MOSFET will be a fitting choice. For H-bridge switches (H1–H4) IRF200 MOSFET is considered. For diode, SB5100 (100 V, 5 A) is used. The switch *S*4 is required to be unidirectional, hence a SB5100 is used in series with IRF540 to make it function like a typical RB-IGBT switch. The DC voltage in this case is set at 36 V which is typically the

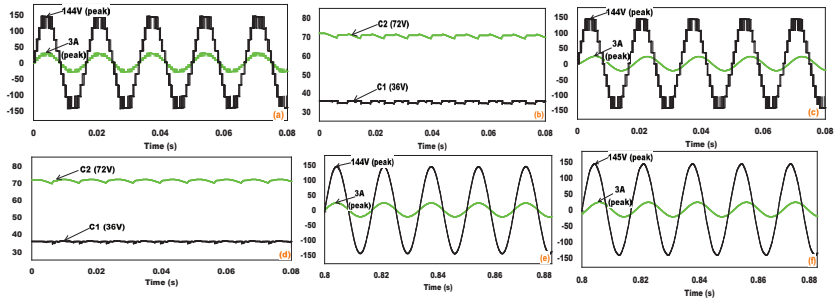

Figure 6. Steady-state output results (a) Output voltage and current waveform for a resistive load of 48 Ω (b) Voltage profile of capacitors *C*1 and *C*2 with load of 50 Ω (c) Steady-state output voltage and current waveform for a resistive load of 48∠45°Ω (d) Steady-state voltage profile of capacitors *C*1 and *C*2 with load of 48∠45°Ω (e) Filtered output voltage and current profile for resistive load of 48∠45° Ω (f) Filtered output voltage and current profile for inductive load of 48∠45°Ω.

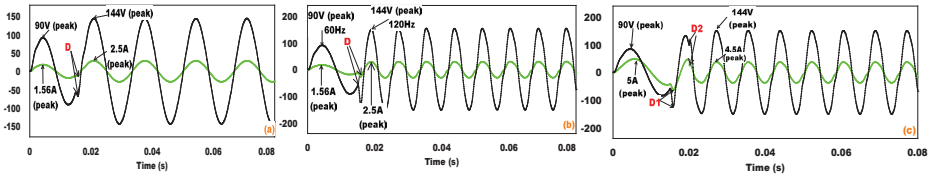

Figure 7. Transient results (a) MI change from 0.95 to 0.6 (b) MI and frequency change simultaneously (c) MI change with frequency change and load change. MI, modulation index change.

output of an average solar panel and standard Li-ion or lead-acid battery pack. The passive filter circuit, which in this case is LC filter, is taken as 8 mH and 15 uF, respectively. Figure 8 shows output waveforms of the laboratory-based prototype model. Figures 8a and 8b show filtered voltage and current wave for a resistive (48 Ω) and inductive (48 ∠ 45°Ω) loads, respectively. Figure 8c shows the voltage profile and their inrush current profile for both the capacitors for a 3 A load current. It can be seen the voltage and current waves are nearly sinusoidal, and the voltage profile of both capacitors is nearly flat. Capacitor *C*1 gives a voltage ripple of 2 V and *C*2 gives a voltage ripple of neatly 4 V for 3 A output load current. The inrush current of *C*1 as indicated in Figure 8(c) shows a peak value of 7 A while for *C*2, the inrush current peak value is 10 A approximately. Figures 8d and 8e show THD figure for load voltage and current. The THD of current is very less, around 0.8% (<1%), while the voltage THD is also very less, settling at around 1.8%. This proves the effectiveness of the proposed circuit in utilising the small edance and power factor angle like 15 ∠ 20°Ω, 30 ∠ 45°Ω, 60 ∠ .30°Ω, 90 ∠ 45°Ω, 120 ∠ 45°Ω, and 150 ∠ 65°Ω, the THD comes in the range of 0.6%–2% for load current and 2%–4% for load voltage. The next set of figures (Fig. 9) shows the voltage stress or TSV pattern of different switches. The TSV pattern is recorded over a period of two full cycles to reveal the intrinsic details of the voltage pattern. It can be seen that all switches lower limit is 0 V except switch *S*4, which is −36 as it has to block a reverse voltage as well. It can be observed that the pattern that H1 switch represents actually is common to H-bridge switches as well. Remaining switches such as *S*1, *S*2, *S*3, *S*4, and *S*5 have their TSV as indicated in Figures 9a and 9b. Figures 9c and 9d indicate the gate pulse pattern of the switches.

Figure 10 investigates the transient analysis of the circuit and shows some figures highlighting the behaviour of the circuit during transient state. As can be seen, Figure 10a indicates output performance of the proposed topology under disturbed condition. Point 'D' indicates point of disturbance. Initially, an R–L load of 17 ∠ 30°Ω. is applied with a 60-Hz supply frequency and 0.6 MI. Then at point D, a sudden change in frequency, load impedance, and MI are introduced. The frequency is changed to 120 Hz, MI changed to 0.95, and load is changed from R–L type to pure resistive load of 29 Ω. It can be observed that the pf factor changes in accordance with the value of load current. The voltage wave immediately regains its full capacity with change in MI to 0.95. Overall, the waveform changes appear to settle with new conditions within one full cycle. Figure 10b shows a condition of absolute load change case where initially an R–L load of 20 ∠ 30°Ω. is applied, and then at point of disturbance D, the load is changed from R–L to pure resistive load of 48 Ω. It is observed after the initiation of change that the load current immediately comes in phase with voltage wave and shows a value of 3 A peak load current. It is also observed that the both voltage and current respond to the change in conditions within one quarter of the full cycle. It is necessary also to investigate the performance of the proposed topology in terms of efficiency and loss analysis. For demonstration purpose, Figure 11a shows the efficiency curve of proposed topology with respect to output power. It can be seen that the efficiency curves show a gradual fall with increase in load power. At 100 W, it registers a efficiency of 96.4%, and at 300 W, it gives an efficiency of 95.6%. When load is at 500 W, the efficiency is around 94%; then at 700 W it is 92.6%, and at 900 W it shows an efficiency of 90.6%. Figure 11b shows the proportion of each of the three prominent loss types taken at an average load power of 500 W.

The work till here describes a novel nine-level quadruple boost topology with all the required results to prove its novelty and specialty. It provides optimum performance efficiency and cost function. A natural way to explore further any basic MLI topology is by analyzing various ways it can be extended (keeping the basic circuit unchanged) to achieve higher level count. The basic quadruple boost nine-level topology can be creatively extended in various ways at the expense of a few additional components which, in exchange, can give much higher magnitude of level count, giving the overall sinusoidal wave very much close to the ideal one. The following are some of the ways the basic topology of nine level can be extended to achieve higher voltage level count.

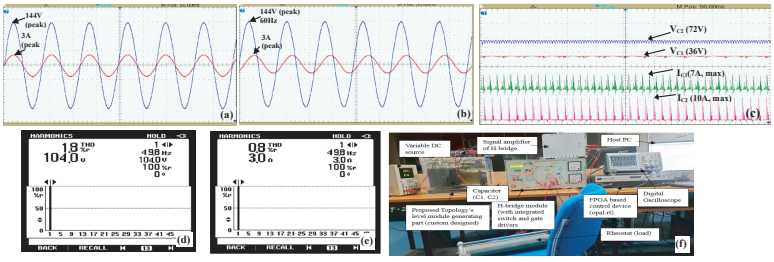

Figure 8. Experimental results (a) Output voltage and current for 48 Ω load. (b) Output voltage and current for 48∠45° Ω load. (c) Voltage and current profile of capacitor *C*1 and *C*2 for supplying load current of 3 A (d) THD of voltage. (e) THD of current (power quality analyser), (f) Hardware setup. THD, total harmonic distortion.

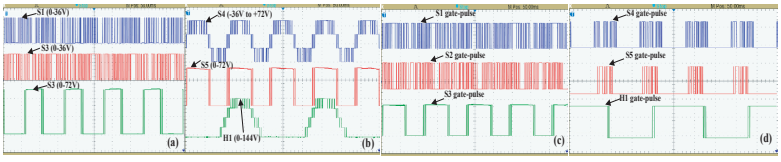

Figure 9. Voltage stress across different switches (a) stress across switches *S*1, *S*2, and *S*3 (b) stress across switches *S*1, *S*2, and *S*5 (c) gate pulse sequence of switches *S*1, *S*2, and *S*3 (d) gate pulse sequence of switches *S*4, *S*5 and H1.

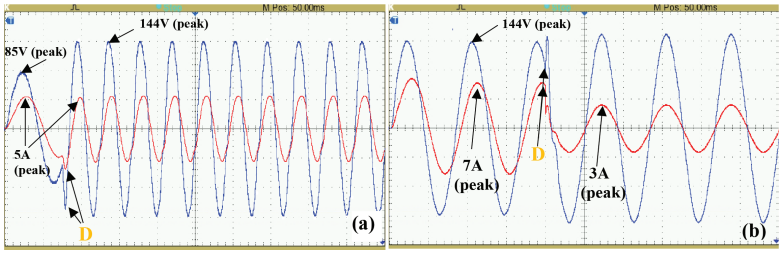

Figure 10. Output during transient state (a) MI change, load change, and frequency change all at one instant (b) load change only. MI, modulation index change.

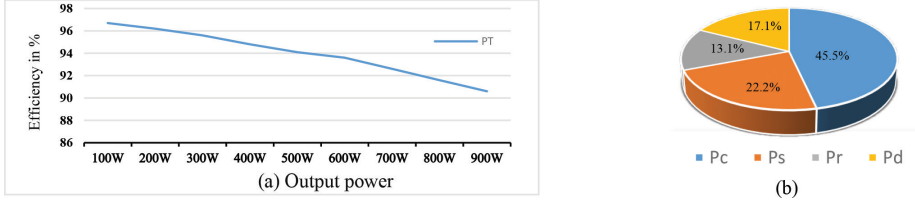

Figure 11. Output during transient state (a) Efficiency curves vs load (b) Loss proportion analysis for 500 W load.

6. Possible Extensions

The proposed topology can be extended in a suitable way for higher levels. The best extension is shown in Figure 12, which consists of two modules and connected back-to-back. The proposed topology is connected with another similar topology with back-to-back connection. If the first module's input DC value is 1 pu, then the second module's value would be set at 9 pu.

Such a configuration is very simple and does not require any additional components for accomplishing the connection. It would be surprising if it can produce a total of 41 distinct levels. So, a perfect 81-level MLI model at the end would be accomplished. Another point about such configuration would be its natural and inherent path for reactive power flow. The reason it can produce such high number of levels is that it can use both additive and subtractive sides. The first module can produce a maximum of four voltage levels. The 5th voltage level would be produced by the difference between the input DC voltage of the second module and the maximum voltage value of

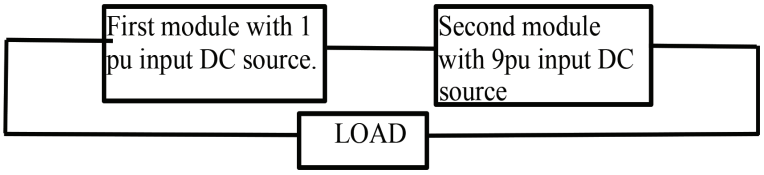

Figure 12. Cascade connection for higher voltage levels.

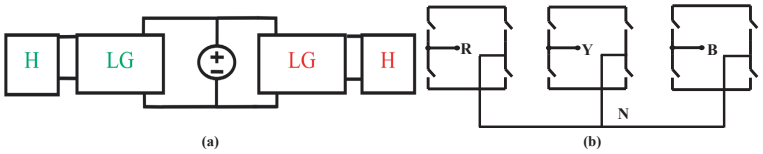

Figure 13. (a) Extension to three phase circuit (red colour represents R phase and green colour represents Y phase). (b) Clubbing H-bridges terminal to form a neutral point (N is neutral).

the first module; hence 9 − 4 = 5 becomes the 5th level. Next, 9 − 3, 9 − 2, and so on with 9 bypassing the entire 1st module to yield the 9th voltage level. The next step is when nine comes subsequently in addition to the voltage level produced by the first level. This additive phase gives 10th level to 13th level of voltage. The 14th voltage level is generated when the 2nd module produces 18 units, a difference of four units compared to the 1st module, thereby producing 18 − 4 = 14th level of voltage. Next, 18 − 3, 18 − 2, and so on with 18 units bypassing the entire 1st module to yield 18th voltage level. Likewise, such permutation and combination would produce a total of 41 distinct voltage levels.

6.1. Possibility of extension to three phase

The proposed circuit extension to a three-phase system is possible as depicted in Figure 13(a). The R phase is in red colour, and the Y phase is in green colour. Considering the figure complexity, the entire circuit is not shown and just R-phase and Y-phase are shown. Similarly, the B-phase can be extended. Keeping the DC voltage source common, the level–generating circuit (LG) circuit and their respective H-bridge circuit can be connected as shown in Figure 13(a). The basic multilevel inverter proposed consists of an input DC followed by a level-generating circuit and then a H-bridge for polarity reversal. The proposed three-phase circuit works well with isolated loads in each phase. But any unified three-phase loading becomes little tricky and identification of a common neutral point is to be considered. Each phase has its own H-bridge as shown in Figure 13(b). A possible way of forming common neutral along with R, Y, B line terminal would be what shown in Figure 13(b). As the basic circuit and its extended variant (with single DC input source) contain only one DC input source and hence a balanced three-phase circuit can be constructed. Thus, the formation of a three-phase MLI is seamless without the use of any extra DC source. Use of only one DC source is also advantageous considering such a configuration will require only one charging circuit and maximum power point tracker (MPPT) control. The problem of array mismatching in case of multiple PV integrated DC source is eliminated. Thus, the single DC source in the middle serving as input source for all the three phase simultaneously is an advantage from many points of view.

7. Conclusion

This article discussed a novel, reduced component nine-level switched-CSMLI topology. It uses only one DC source and two capacitors. A unique switching scheme is discussed to mitigate insufficient capacitor voltage problem which is associated with majority of high-boost CSMLI. This is naturally stable and gives balanced capacitor voltage profile also. A vivid comparative analysis with similar other topologies in quantitative and qualitative terms is presented. Among the existing works, the proposed topology achieves the minimum cost function. Furthermore, a unique suitable and effective extension is proposed to produce higher number of voltage levels. A possible description is also given towards extending it to a three-phase model as well. Both the basic model and the extended model have inherent reactive power flows. Both simulation and experimental results have shown steady-state and transient output response to prove the merit and effectiveness of the circuit.

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