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Analysis of a Novel Soft-Switching DC–DC Converter for Reduction in Switching Loss

Research Paper

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Abstract: The conventional buck converter is the first and foremost member among the family of DC–DC converters. Major drawback of the conventional buck converter is the hard-switching that leads to many shortcomings and finally leads to poor efficiency. So it is the soft-switching (i.e. zero-voltage switching or zero-current switching) mechanism that can alleviate these shortcomings. In past, the researchers have proposed a numerous soft-switching topologies without giving attention to number of active and passive components. Hence it has been focused on optimization of number of active and passive components to be used in proposed topology. This article introduces a novel technique for soft-switching of a DC–DC buck converter, which is independent of snubber resistance and possesses only a snubber capacitor across each switch. The filter parameters of proposed structure are different than those of conventional one. With the inclusion of these filter parameters, the proposed structure is operated under zero-voltage switching or zero-current switching to enable the soft-switching of its devices. The designing technique of this proposed converter is properly narrated. The control strategy is quite simple. The MATLAB/Simulink (MATLAB 6.1 (Version)) model for the proposed topology is developed and its simulation is carried out to analyze its performance.

Keywords: *MATLAB (Simulink) • design and modification of filter parameters • zero-current switching • non-isolated type two-switch buck converter • zero-voltage switching*

1. Introduction

Buck converter is the prominent and first generation member among the family of DC–DC converters (Rashid, 2004; Wu et al., 2015). In this, the necessities of soft-switching associated with various topologies of DC–DC converters have been illustrated. The hard-switching of self-commutating switching devices in power electronic circuits has been a major concern for researchers due to their various shortcomings. Hence, it results in an increase in the size of the heat sink, rating of filters, electromagnetic interference, etc. It finally leads to poor efficiency and so on. So it is the soft-switching mechanism (i.e., zero-voltage switching [ZVS] and zero-current switching [ZCS]) which can overcome these aforesaid problems. The fundamentals and the analysis of different DC–DC converters are covered (Rashid, 2004). Initially, the soft-switching is initiated with the load resonant technique, and later this technique went through its various developmental stages. The latest technique is terminated with a quasi-resonant technique. The researchers have utilised most preferred quasi-resonant principle for boost converter using single resonant network (Barreto et al., 2005). A soft-switching DC/DC converter with high voltage gain is presented (Do, 2010). This topology comprises two switches, four diodes, four capacitors, one source inductor and two pairs of coupled inductors. The researchers (Li et al., 2012) proposed the zero voltage transition (ZVT) principle, in which a very small interval of zero-voltage is created in a switching cycle for soft-switching using a quasi-resonant

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technique. Researchers (Gu et al., 2014; Prabhala et al., 2016; Siwakoti et al., 2014) proposed a high voltage DC–DC converter and a method of cancellation technique of current ripple at the input.

Prabhala et al., 2016 have incorporated two input boost stages for high voltage gain, whereas the researchers (Gu et al., 2014) suggested a technique for cancellation of current ripple at the input of the boost converter using a tapped inductor. To enable soft-switching the devices (Li et al., 2014), the converter possesses more than one switch and additional passive parameters. In some cases, they retain coupled inductors to drain out the primary current to the secondary, which appears to be complex because of a significant increase in components. A novel soft-switching DC–DC converter is proposed (Rathore et al., 2016). Here it is proposed a bi-directional soft-switching current-fed LCL resonant DC/DC converter is proposed to interface with a micro-grid, whereas Dobakhshari et al., 2017 have proposed a novel quasi-resonant current-fed converter with minimum switching losses. The researchers (Hosseinzadeh et al., 2019; Mohseni et al., 2020) proposed a soft-switching bidirectional step-up/step-down DC–DC converter. There has been proposed by researchers (Maulik et al., 2020) for a LCL resonant network and coupled inductor to enable soft-switching, but this phenomenon makes it bulky and complex to analyse the topologies. In literature (Behera et al., 2020), it has been emphasised to utilise the soft-switching technique for regulated power supply. Mohammadi et al., 2021 have presented a review paper listing a family of soft-switching DC–DC converters with two degrees of freedom in which the main topology is oriented in two different ways without the addition of any extra components to achieve desired performances. Hasanpour et al., 2021 proposed a new concept of using three winding coupled inductors along with a few other passive components for soft-switching for a fixed power rating, but in case of different ratings, it needs to redesign those coupled inductors. A separate secondary turn-off snubber is utilised for high-frequency soft-switching DC–DC converters (Pastor et al., 2022), whereas the researchers (Cheng et al., 2021) have highlighted the state-of-the-art on soft-switching technologies of DC–DC converters in their review paper. The inclusion of soft-switching technologies has been implemented in renewable power sources (Danyali et.al., 2022). The researchers (Yen and Chao, 2022) have proposed a topology comprising two switches, a coupled inductor along with multiple passive components and diodes, whereas the soft-switching technique (Forouzesh, 2022) has been extended to a three-phase AC-DC converter for power factor correction. Lalitha et al., 2022 have extended the soft-switching technique using ZVS for vehicle and grid applications with enhanced efficiency. On the contrary, it has been stressed the single-switch resonant principle for soft-switching DC–DC converter (Abbasian et al., 2022).

The researchers (Li et al., 2022; Yen and Chao, 2022) have proposed a two-switch topology with coupled inductors and other passive components for a soft-switched DC–DC converter. Researchers (Guan et.al., 2022, Kalahasthi et al., (2022 and 2023)) have included the high-gain soft-switching technique in DC–DC converter for renewable applications. It has been proposed a fully soft-switched non-isolated high step-down DC–DC converter (Khallili et al., 2023) with reduced voltage stress by using a number of switches and considerable passive components (i.e., three switches along with their anti-parallel diodes, five capacitors and two inductors).

Zhou et al., 2023 proposed a two-switch topology along with a considerable number of active and passive parameters (i.e., four capacitors, six diodes, two inductors) for soft switching of the devices. Researchers (Yan et al., 2023) have implemented the soft-switching technique for a bidirectional converter so as to extend its application for battery charging/discharging systems without sacrificing in minimising the ripple. Kalahasthi et al., 2023 have proposed a two-switch topology with two pairs of coupled inductors and five capacitors, which appears to be a significant increase in passive components. Similarly, the proposed topology (Montazerolghaem et al., 2023) contains two switches, two diodes, four inductors, one coupled inductor and four capacitors for step-down DC–DC converter. Such excessive passive components may not be attractive for researchers and commercially viable. Researchers (Pakdel et al., 2019) utilises a two-switch topology, one coupled inductor, one filter inductor, three diodes and three capacitors. Both switches are turned on ZVS and turned off under ZCS. Though the topology (Jahangiri et al., 2022) comprises a single switch, on the contrary, it possesses two pairs of coupled inductors, six diodes and two capacitors. Significant increase in the number of diodes and use of a coupled inductor make this topology less attractive.

From the above reviews, it is summarised that most of the researchers have used two or more switches, but with a significant number of passive components to facilitate soft-switching. In this paper, a novel two-switch topology with minimum passive components is proposed for a soft-switching buck converter. In a conventional buck converter, the filter inductor carries unidirectional current. But the filter inductor of the proposed topology carries bidirectional current, and the control technique for this converter is very simple. The proposed topology is analysed and validated through experimentation.

2. Proposed Topology and Modes of Operation

The conventional buck converter is shown in Figure 1. It comprises a semiconductor switch along with a snubber mechanism in parallel and a free-wheeling diode across the load. The anti-parallel diode across the switch acts as a feedback element and also as a protection tool for the switch. A low-pass filter is provided between the switching device and the load in order to minimise the ripple content in the output voltage. The prominent shortcomings in the conventional buck converter are the limitation in switching frequency, requirement of comparatively higher rating of filter parameters and heat sink, etc.

2.1. Proposed topology

The conventional topology can be replaced by the proposed novel buck converter, which can perform with soft-switching as shown in Figure 2. The proposed topology comprises a pair of switches (one in series and the other across a shunt/dc link) and each switch is provided with an anti-parallel diode and high frequency snubber capacitor. The mid-point between the switches is connected to high-frequency filter inductor, followed by a filter capacitor connected across the load. The filter inductor and capacitor are designed in such a way that the current in the filter inductor becomes bidirectional with the alternate operation of two switches.

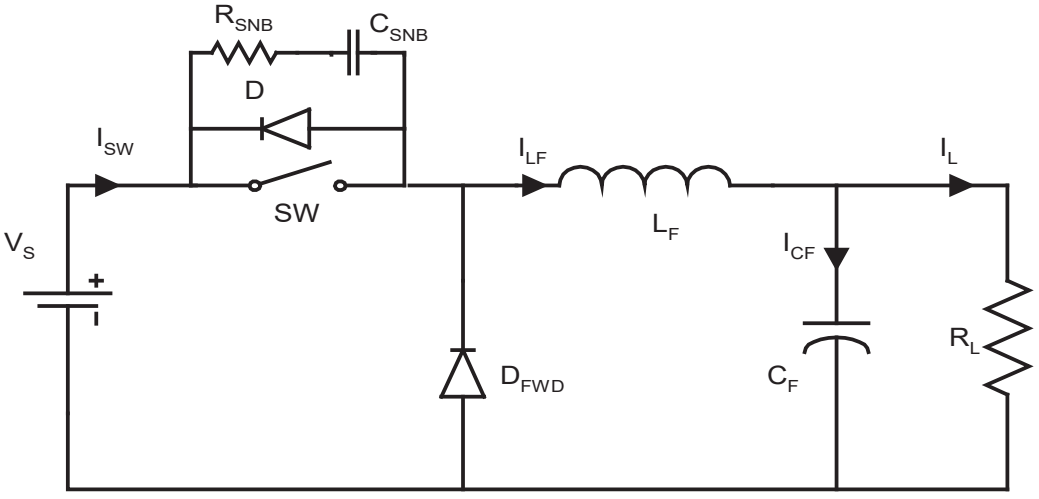


Figure 1. Conventional buck converter.

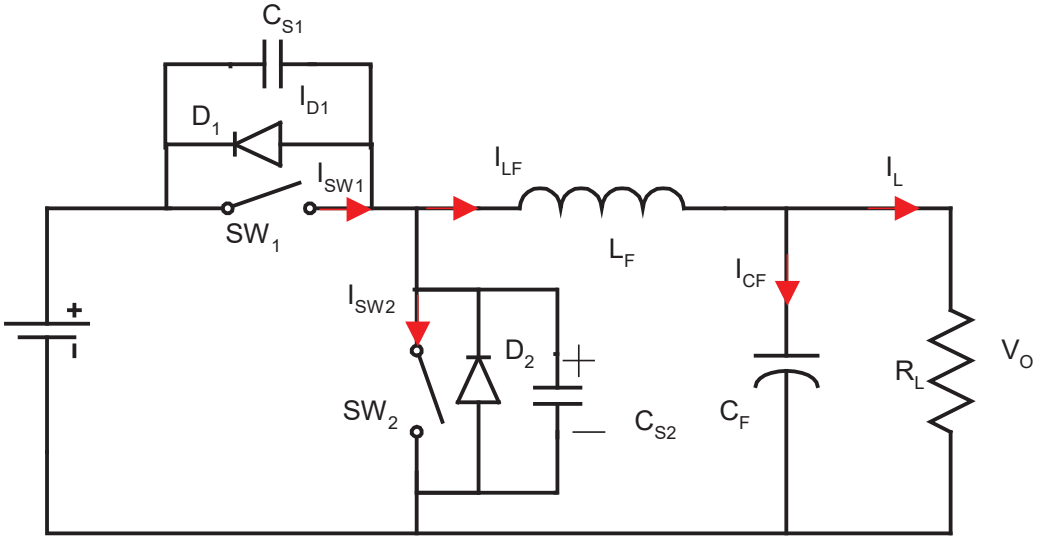


Figure 2. Proposed two-switch buck converter.

2.2. Modes of operation

The principle of operation of the proposed converter is explained through Figures 3 and 4. Figure 3 shows a typical waveform for the explanation of the operation of the proposed topology during a switching cycle under steady state operation. The operation during a switching cycle is divided into eight modes of operation (i.e., Mode I to Mode VIII). These modes are shown in Figure 4. The dead time (i.e., time lag between the two switches when both of them are an off condition) is maintained during the transition of SW_1 to SW_2 and vice versa to enable soft-switching.

Assuming that the snubber capacitor (C_{S2}) across the DC link is charged to the source voltage and both devices across it (i.e., SW_2 and D_2) are in the off-state. The switch SW_1 is turned on, but it is in the off state as its anti-parallel diode D_1 is conducting the reversal current of the filter inductor. So the voltage across the snubber capacitor (i.e., C_{S1}) is at zero due to the conduction of diode D_1.

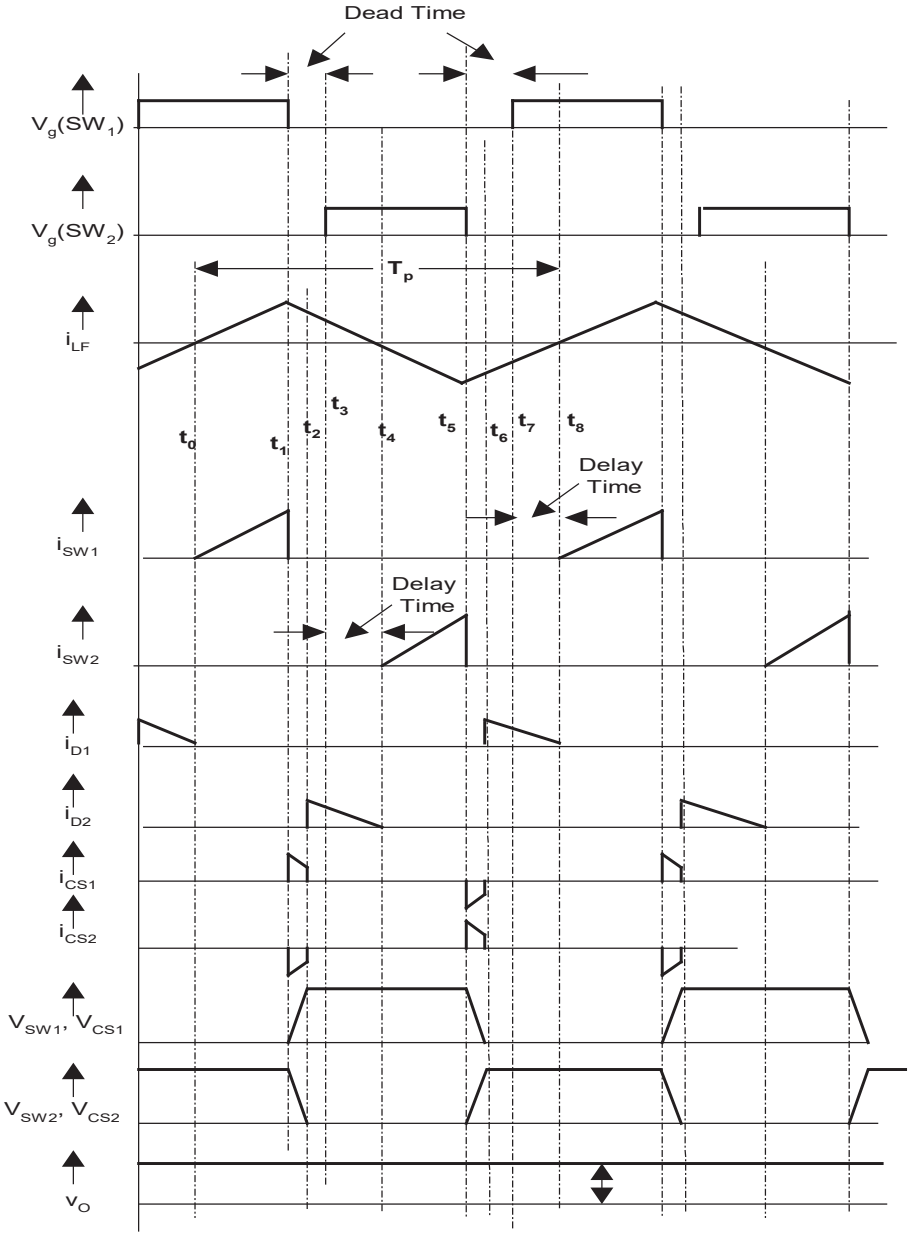
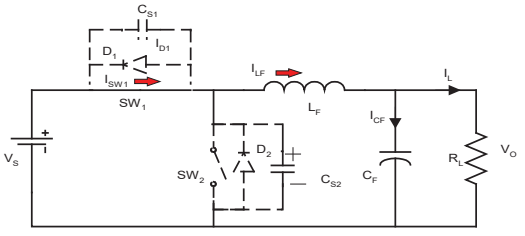
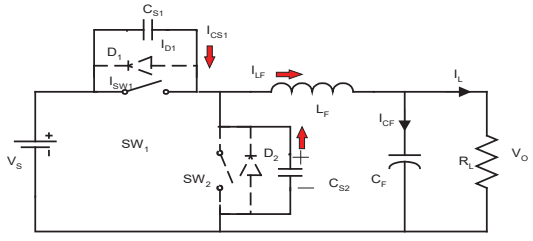


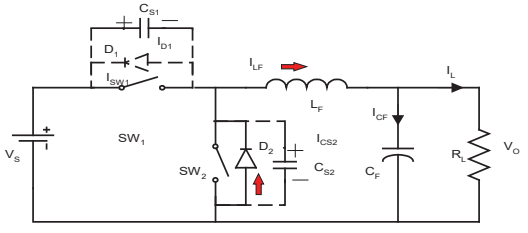
Figure 3. Typical waveforms during one cycle under steady-state operation.



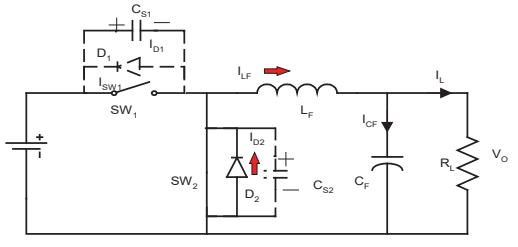
(a) Mode I



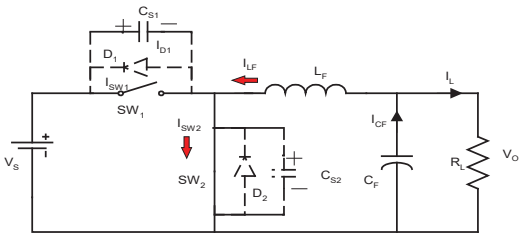
(b) Mode II



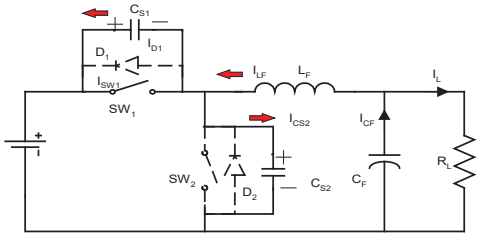
(c) Mode III



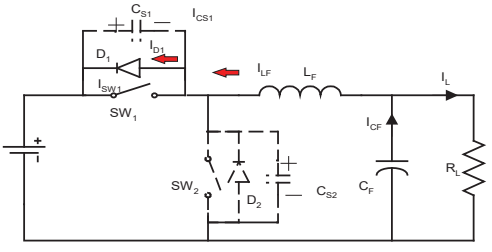
(d) Mode IV



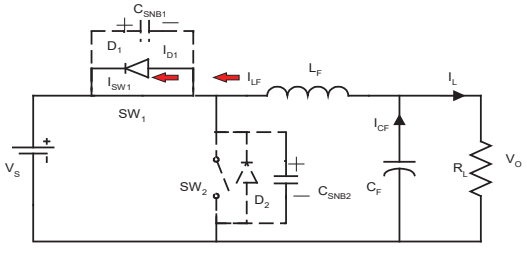
(e) Mode V



(f) Mode VI



(g) Mode VII



(h) Mode VIII

Figure 4. Modes of operation (Modes I to IV). Modes of operation (Modes V to VIII).

Mode I (t_0~t_1): Though the switch (SW_1) is already turned on prior to this mode, as stated in the initial condition, it does not conduct current as the diode D_1 is forward-biased due to reverse current in the filter inductor. This mode (i.e., Figure 4a) starts when the diode D_1 becomes reverse biased (i.e., when the reverse current in the filter inductor drops to zero) and the switch SW_1 starts to carry current linearly from zero through the filter inductor. Thus, it provides power/energy to the parallel combination of load and filter capacitor. Now the direction of current in the filter inductor is from the source to the load. In this mode, the capacitor across switch (SW_2) is clamped to the source voltage. The first mode ceases when the gating signal from SW_1 is withdrawn.

Mode II (t_1~t_2): In the second mode of the operation (Figure 4b), as the gate signal of SW_1 is withdrawn, the current in the filter inductor diverts its path from switch SW_1 to its parallel capacitors, C_{S1} and C_{S2}. This instant is the initiation of Mode II. This capacitor C_{S1} gradually charges to the source voltage, whereas C_{S2} discharges to zero, which is the end of this mode. When the capacitor C_{S2} attains the magnitude of the source voltage, the voltage across SW_2 falls to zero. So the DC link is virtually isolated from the source. During this mode, the current in the filter inductor decays. During the process of charging capacitor C_{S1}, the series switch SW_1 gets enough time for its turn-off under ZVS, as the charging time of C_{S1} is more than the turn-off time of SW_1.

Mode III (t_2~t_3): In the 3rd mode (i.e., Figure 4c), as the voltage across SW_2 falls to zero, the current in the filter inductor diverts its path to the shunt diode (D_2) across the shunt switch (SW_2). This mode continues till the shunt switch SW_2 is turned on.

Mode IV (t_3~t_4): In the 4th mode of operation (i.e., Figure 4d), as the shunt switch SW_2 is already turned on, but it does not carry current due to the forward-biased of its anti-parallel diode D_2. This mode continues till the current in D_2 falls to zero. This situation is the end of this mode, and the turn-on of the switch SW_2 is under ZVS (i.e., at zero voltage due to conduction of diode D_2).

Mode V (t_4~t_5): In the 5th mode (i.e., Figure 4e), the current in the filter inductor reverses as the current in the shunt switch SW_2 gradually increases from zero, which is the initiation of this mode. From the previous mode IV and current mode, it is concluded that the switch is turned on under ZVS, followed by ZCS, when the current in it starts from zero. This will continue till the gating signal of switch SW_2 is withdrawn, which is the end of this mode.

Mode VI (t_5~t_6): In the 6th mode of operation (i.e., Figure 4f), the gating signal from SW_2 is withdrawn and the reversal of current in the filter inductor shifts from SW_2 to the capacitors C_{S2} and C_{S1}. The capacitor C_{S2} charges to the source voltage, and C_{S1} discharges to zero. Both charging and discharging processes occur simultaneously. At the end of this mode, the phenomena of charging and discharging of capacitors stops, but still the filter inductor retains some quantity of reversed current. The switch (SW_2) is turned off under ZVS due to its parallel capacitor C_{S2}, which is already at zero voltage level.

Mode VII (t_6~t_7): In the 7th mode (i.e., Figure 4g), as the voltage across C_{S1} falls to zero due to the previous action, the reverse current of the filter inductor takes its path from the snubber capacitors to diode D_1. This is the initiation of the mode, and this mode ceases when SW1 is turned on.

Mode VIII (t_7~t_8): In 8th mode (i.e., Figure 4h), the series switch SW_1 is provided with a gate pulse, but the diode D_1 is already on in earlier modes due to reversal current in the filter inductor. So the conduction of SW_1 gets delayed even if it is turned on. This mode would continue till the reversal current in the filter inductor (i.e., via diode D_1) decays to zero. So this leads to soft-switching on for the switch SW_1 under ZVS (i.e., due to conduction of diode D_1), followed by ZCS (i.e., current in SW_1 initiates from zero). After this mode, the switching cycle repeats again with Mode I.

This concept is completely innovative, as the snubber capacitors do not discharge their energies across their switches under steady-state operation, and this fact can be confirmed later from the simulation. The filter parameters of the proposed topology are designed in such a way that the filter inductor carries bidirectional current. The switch SW_1 carries the rising portion of positive half current in the filter inductor, whereas its shunt switch SW_2 carries the falling portion of negative half current in the filter inductor. A dead time is allowed between two switches not only to avoid a short-circuit across the DC link, but also to facilitate the charging of the capacitor across a switch, followed by the discharging of the capacitor across the other switch and vice versa. Also, it leads to the conduction of anti-parallel diodes. More clearly, it can be stated that before the conduction of SW_2, the snubber capacitor C_{S1} is allowed to charge, followed by the discharging of C_{S2}. This happens due to positive/forward current in the filter inductor during dead time, and it leads to conduction of the anti-parallel diode D_2. So during the conduction of D_2, SW_2 is activated. The conduction of D_2 creates a situation of zero voltage across switch SW_2, which prevents its conduction, even though this switch is turned on. This would continue till the current in diode D_2 decays to zero. After this situation, the SW_2 would start to conduct with zero current. As a consequence, the conduction of SW_2 gets delayed with respect to its initiation of gating pulse, and it leads to turn-on of this switch under ZVS, followed by ZCS.

A similar procedure repeats for SW_1. Before SW_1 is turned on, it is allowed to charge C_{S2} and discharge C_{S1} by the negative/reverse current in the filter inductor, followed by conduction of anti-parallel diode D_1. During the conduction of diode D_1, the SW_1 is gated on, but it is delayed due to the conduction of diode D_1. So this leads to its turn on under ZVS (i.e., due to conduction of diode D_1), followed by ZCS (i.e., due to initiation of SW_1 from zero current). When the gate signals are withdrawn from the switches, their currents are diverted through respective parallel snubber capacitors, which leads to turn off for the switches under ZVS.

3. Design of Parameters for Proposed Buck Converter

The design of filter parameters for the discontinuous current in the filter inductor of conventional topology (Rashid, 2004) is required in this case, as these parameters need to be extended to the proposed topology to enable the bidirectional current in the filter inductor. This bidirectional current is achieved with the help of the alternate operation of its two switches.

3.1. Design of a filter for a two-switch buck converter

In order to achieve discontinuous current through the filter inductor of a buck converter for soft-switching on, a proper design method is required. The filter inductor at the source (L_F) and the filter capacitor across the load (C_F) are designed as follows:

The design of filter parameters for discontinuous operation in the case of a conventional one is as follows.

The voltage across the series inductor L_F of the buck converter is, in general

$$e_{LF} = L_F \frac{di_{LF}}{dt} \tag{1}$$

The ripple current in L_F is assumed to rise linearly from I_{min} to I_{max} in time t_{on}. Eq. (1) is rewritten as

$$V_s - V_o = L_F \frac{I_{max} - I_{min}}{t_{on}} = L_F \frac{\Delta I}{t_{on}} \tag{2}$$

$$\Rightarrow t_{on} = L_F \frac{\Delta I}{V_s - V_o} \tag{3}$$

$$\Rightarrow \Delta I = \frac{(V_s - V_o)\, t_{on}}{L_F} \tag{4}$$

The current in the filter inductor falls linearly from I_{max} to I_{min} in time t_{off}. 'ΔI' is the difference between the peak and minimum value of ripple current. Eq. (2) is written under the off-period as follows.

$$-V_o = L_F \frac{-\Delta I}{t_{\text{off}}} \tag{5}$$

$$\Rightarrow t_{\text{off}} = L_F \frac{\Delta I}{V_o} \tag{6}$$

$$\Rightarrow \Delta \text{I} = \frac{V_o\, t_{\text{off}}}{L_F} \tag{7}$$

where ΔI = $I_{max} - I_{min}$ and equating 'ΔI' in Eqs (4) and (7) gives:

$$\frac{(V_s - V_o)\, t_{\text{on}}}{L_F} = \frac{V_o\, t_{\text{off}}}{L_F} \tag{8}$$

On substituting t_{on} = kT and t_{off} = (1 − k) T (i.e., where k: duty ratio and T: switching period) in Eq. (8), it yields the average output voltage

$$V_o = V_s \frac{t_{\text{on}}}{T} = kV_s \tag{9}$$

If it is assumed a lossless circuit, then input power = output power

$V_s I_s = V_o I_o = kV_s I_o$ and the average input current $I_s = k I_o$

The switching period (T) can be expressed using (3) and (6) as

$$T = \frac{1}{f_{\text{sw}}} = t_{\text{on}} + t_{\text{off}} = L_F \left(\frac{\Delta I}{(V_s - V_o)} + \frac{\Delta I}{V_o} \right) \tag{10}$$

$$= \frac{\Delta I\ L_F\ V_s}{(V_s - V_o)V_o}$$

$$\Rightarrow \Delta I = \frac{(V_s - V_o)V_o}{f_{sw} L_F V_s} = \frac{kV_s(1-k)}{f_{sw}\ L_F} \tag{11}$$

The inductor current i_{LF} can be expressed as

$$i_{LF} = i_{CF} + i_L \tag{12}$$

If the ripple current upon load is assumed to be small, then $i_{LF} = i_{CF}$.The average capacitor current that flows into the filter capacitor for the duration of $t_{on} + t_{off} = T/2$ is

$$I_{Cf} = \Delta I / 4 \tag{13}$$

The load capacitor voltage is expressed as

$$v_{CF} = \int i_{CF}\ dt + v_{CO}(t=0) \tag{14}$$

and the peak-to-peak ripple voltage of the capacitor is

$$\Delta VC_F = v_{CF} - v_{CFO} = \frac{1}{C_F}\int_0^{\frac{T}{2}} \frac{\Delta I}{4}\ \text{dt} \tag{15}$$

$$= \frac{\Delta I\ T}{8C_F} = \frac{\Delta I}{8 f_{sw} C_F}$$

Using 'ΔI' of Eq. (11) in (15), it yields

$$\Delta V_{CF} = \frac{kV_s(1-k)}{8\ L_F C_F f_{sw}^2} \tag{16}$$

Eqs (11) and (16) are required to design the value of L_F and C_F, provided the ripple current and voltage are given.
Condition for verge of continuous current in the filter inductor and voltage across the filter capacitor:
If I_L is the average inductor current, the maximum ripple current is $\Delta I = 2I_L$ and substituting it in Eq. (11)

$$2I_L = \frac{kV_s(1-k)}{f_{sw}\ L_F} \tag{17}$$

The average output/load current (I_L) is expressed as

$$I_L = \frac{V_o}{R_L} = \frac{kV_s}{R_L} \tag{18}$$

where R_L is load resistance, V_o and V_s are average output and input voltage, respectively
On substituting Eq. (18) into (17)

$$\frac{2kV_s}{R} = \frac{kV_s(1-k)}{f_{sw}\ L_F} \tag{19}$$

This Eq. (19) gives the critical value of inductor L_{CF} by replacing L_F by L_{CF} in Eq. (19) (i.e., verge of continuous conduction of inductor current)

$$L_{CF} = \frac{(1-k)R}{2 f_{sw}} \tag{20}$$

Similarly, if the V_{CF} is the average capacitor voltage, the capacitor ripple voltage will be maximum when

$$\Delta V_{CF} = 2\ V_o \tag{21}$$

On substituting Eq. (16) into (21), we can get

$$\frac{kV_s(1-k)}{8\ L_F C_F f_{sw}^2} = 2V_o \tag{22}$$

Since V_o = kV_s, so Eq. (22) is replaced as

$$\frac{kV_s(1-k)}{8\ L_F C_F f_{sw}^2} = 2kV_s \tag{23}$$

Eq. (23) results in getting the critical value of the capacitive filter. By replacing C_F by C_{CF}

$$C_{CF} = \frac{(1-k)}{16\ L_f\ f_{sw}^2} \tag{24}$$

Eqs (20) and (24) result in determining the critical values of the filter inductor and capacitor that give the information on the verge of continuous conduction for current in the filter inductor (L_F) and voltage of filter capacitor (C_F). So it indicates that the values of L_F and C_F below their critical values L_{CF} and C_{CF} lead to discontinuity in inductor current in the case of a conventional one, but bidirectional continuous current in the filter inductor of the proposed topology. But as per the requirement of the topology, it is needed a continuous bidirectional current in the filter inductor and a negligible ripple in voltage across the filter capacitor at the maximum permissible value of duty ratio. So the practical value of the filter inductor and capacitor would satisfy the following conditions.

$$L_F < L_{CF} \text{ and } C_F >> C_{CF} \tag{25}$$

The L_{CF} and C_{CF} (i.e., for the load resistance R_L = 15 ohm, source voltage V_s = 30 V, switching frequency f_{sw} = 40 kHz at a maximum permissible duty ratio of 0.85) to be considered for simulation are computed from Eqs (20) and (24) as follows.

The critical value of the filter inductor (L_{CF}) is 28 μH, and the critical value of the filter capacitor C_{CF} is 0.58 μF. But the actual value of the filter inductor and filter capacitor is based upon Eq. (25) are considered as 10 μH and 100 μF, respectively.

3.2. Design of snubber capacitor

To design the value of snubber capacitors (C_{S1} and C_{S2}) across switches, the following three parameters are required.

Peak current through filter inductor/switch

Device turn-off time (t_q)

Source voltage (V_s)

The charging time (t_c) for the snubber capacitor to be connected across the switch must be greater than the device turn-off time so as to facilitate soft-switching of the device. So this charging time (t_c) is assumed to be twice the device turn-off time (t_q), which can be obtained from the data sheet of the device.

The equation of charging of the snubber capacitor ($C_S = C_{S1} = C_{S2}$) is given by

$$V_s = I_{peak}\frac{t_c}{C_S} = I_{peak}\frac{2t_q}{C_S} \tag{26}$$

$$\Rightarrow\ C_S = 2I_{peak}\frac{t_q}{V_s} \tag{27}$$

where I_{peak} is the peak current through the switch, and it is assumed to the twice the average load current

$$I_{\text{peak}} \approx 2I_L \tag{28}$$

On substituting Eq. (28) in (27), the expression of the snubber capacitor is given by

$$C_S = 4I_L \frac{t_q}{V_s} = 4\left(\frac{V_o}{R_L}\right)\frac{t_q}{V_s} = \frac{4V_o\ t_q}{R_L V_s} \tag{29}$$

The rating of the snubber capacitor is obtained from Eq. (29) and is considered to be common for both series and shunt snubber capacitors. The value of the snubber capacitor is considered as 0.15 μF for both C_{S1} and C_{S2}.

3.3. Dead time (T_{dead}) between switches

The dead time (T_{dead}) is provided (i.e., between turn-on of SW_2 and turn-off of SW_1 and vice versa) not only to avoid the short-circuiting across the DC link, but also to facilitate the soft-switching. The minimum dead time is the summation of the charging or discharging of snubber capacitors. Both charging and discharging of snubber capacitors take place simultaneously. The actual dead time is more than the charging or discharging time of snubber capacitors. So the minimum dead time is decided in such a way that before conducting any switch, its anti-parallel diode must be conducting. The switch would start to conduct when the anti-parallel diode across it stops conducting. The dead time is computed with the following equation.

$$T_{\text{dead}} \geq 2\ T_{\text{charge/discharge}} \tag{30}$$

where $T_{charge/discharge}$: Charging or discharging time of snubber capacitor (μs).

3.4. Soft-switching condition criteria

The switches are activated with gate pulses during forward-biasing of their corresponding anti-parallel diodes, but switches do not conduct as it creates zero voltage across switches due to conduction of anti-parallel diodes. So this leads to ZVS operation. When these anti-parallel diodes come out of forward-biased condition, the switches start to conduct which leads to ZCS operation. Above all, it can be referred that switches are turned on under ZVS, followed by ZCS.

When switches are turned off, their corresponding snubber capacitors bypass the currents of the switches. The charging period of these capacitors needs to be more than the turn-off time of the switching device. So the snubber capacitors assist the switches to turn off ZVS operation.

4. Simulation and Experimental Results

The designed parameters of the proposed topology (i.e., at possibly maximum duty ratio [say k_{max} – 0.85], load resistance R_L = 15 Ω, switching frequency f_{sw} = 40 kHz and source voltage V_s = 30 V) are computed. Filter inductance = 10 μH, filter capacitor = 100 μF, snubber capacitances (C_{S1}, C_{S2}) = 0.15 μF and dead time (T_{dead}): 2μs.

4.1. Simulated results

The simulated results under MATLAB/Simulink environment under steady-state conditions are depicted in Figures 5–15. Figure 5 shows that the relevant waveforms are associated with switch SW_1 at a duty ratio of 30%. The current waveforms of switch (SW_1), snubber capacitor (C_{S1}), diode current (D_1), filter inductor (L_F) and voltage across SW_1 (i.e., same as V_{CS1}) corresponding to its gate pulse V_g (SW_1) are shown. It is observed that the current lags behind the initiation of the gate pulse V_g (SW_1) by a delay time T_d (SW_1), as evident from the waveform. This delay is due to the conduction of its anti-parallel diode (D_1). At this moment, the voltage across switch SW_1 is zero, leading to the switch turning on under both ZVS, followed by ZCS.

Similar waveforms of currents and voltage across switch SW_2 corresponding to its gate pulse V_g (SW_2) are shown in Figure 6 at a duty ratio of 30%. It also shows the time delay in conduction of SW_2 with respect to its gating pulse due to the conduction of the anti-parallel diode D_2. Interestingly, the turn-off processes of both switches are

simple as the currents in these switches are diverted to their respective parallel snubber capacitors, facilitating their soft-switching.

Figures 7 and 8 show the relevant waveforms of switches SW_1 and SW_2 at a duty ratio of 60%, along with the current in the filter inductor (L_F) with respect to the gating pulses of both switches. This differentiates the comparison of their soft-switching during the conduction of both switches. The current in the filter inductor is found to be bidirectional, and various part of it during different time intervals reflects the current through different components of this topology.

Figure 9 depicts the waveforms of currents in both SW_1 and SW_2, along with the filter inductor L_F with respect to its gating pulse of SW_1 at a duty ratio of 60%. So it can be differentiated with the instant of applying of gating pulses with dead time. In current waveform of the filter inductor shows the time delay of conduction of both switches with respect to their initiation of gating pulses.

Figure 10 shows the gate pulses, currents, voltage across both switches, currents in both snubbers and in parallel diodes, along with the current of the filter inductor at a duty ratio of 60% for both switches. So it can be distinguished between waveforms associated with SW_1 and SW_2.

The waveforms of currents in the filter inductor, filter capacitor and load, along with load voltage, are shown in Figure 11. According to Kirchhoff's law, the current of the filter inductor is the sum of currents in the filter capacitor and load. The output voltage is found to be around ripple-free.

Figures 12 and 3 show waveforms associated with SW_1 and SW_2 at a duty ratio of 30% and the average output voltage is nearly 8.3 V for an input of 30 V, which indicates buck operation. Also, the conduction of diode D_1 shows power recovery for a short interval in a switching cycle.

Figure 14 shows the currents in both switches with respect to their respective gating pulses at a duty ratio of 30%. It also shows the output voltage profile from transient to steady-state at the same duty ratio. Similar waveforms are shown in Figure 15 at a duty ratio of 40% with an output voltage of 11.5 V. The operation under both duty ratios of 30% and 40% ensures buck operation and indicates that their voltage profiles are 8.3 V and 11.5 V, which are close to their ideal values (9 V and 12 V).

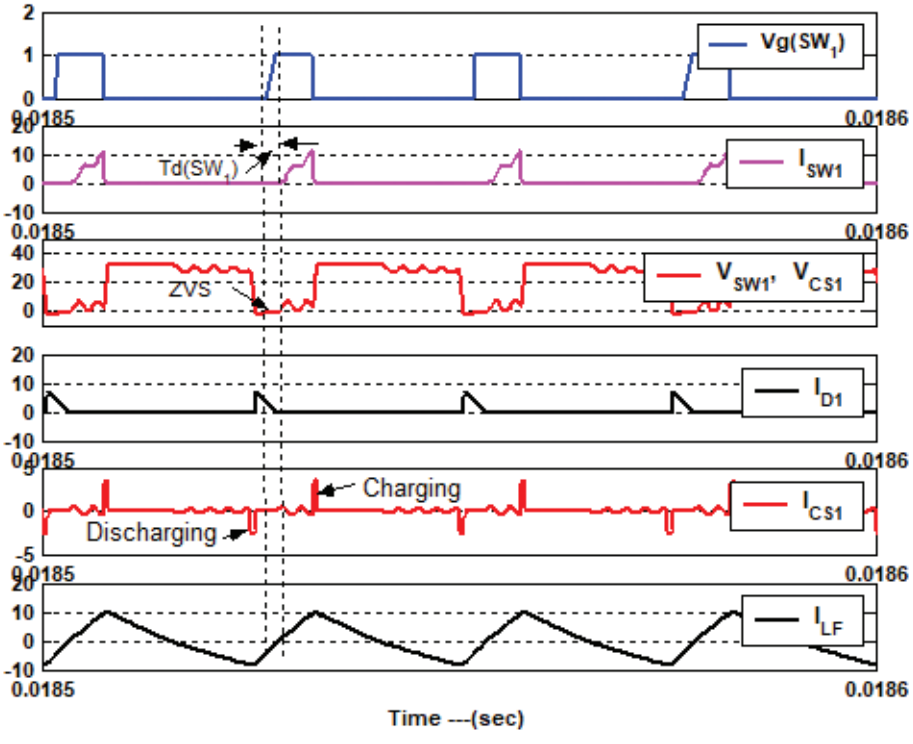


Figure 5. Waveforms of currents in SW_1, C_{S1}, D_1 and L_F and voltage across SW_1 and C_{S1} with respect to corresponding gate pulses at a duty-ratio of 30% and switching frequency f_{sw} = 40 kHz.

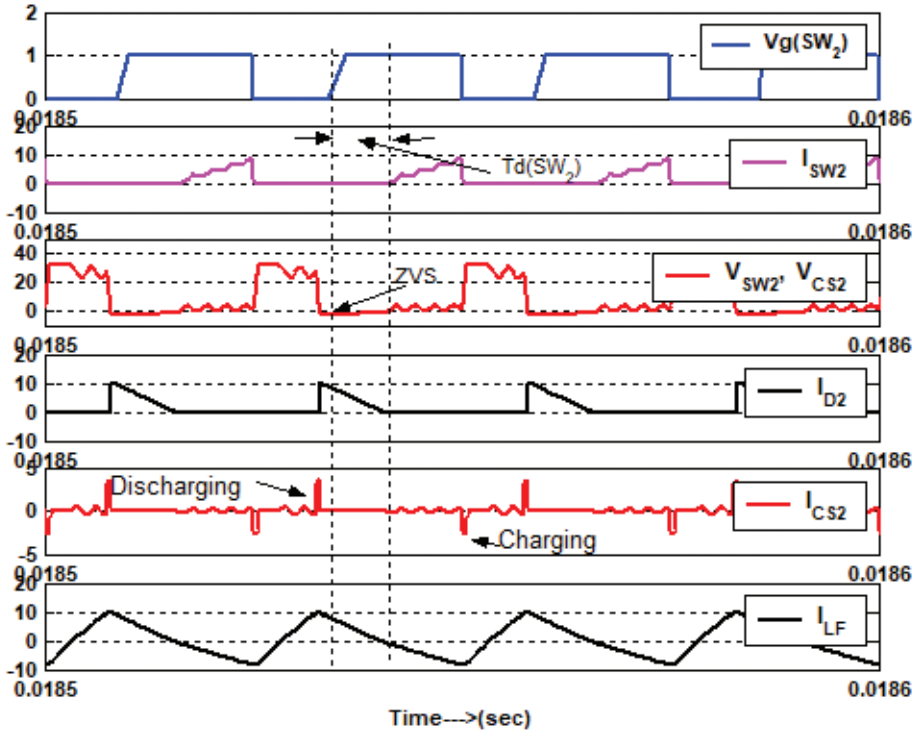


Figure 6. Waveforms of currents in SW_2, C_{S2}, D_2 and L_F and voltage across SW_2 and C_{S2} with respect to corresponding gate pulses at a duty ratio of 30% and switching frequency f_{sw} = 40 kHz.

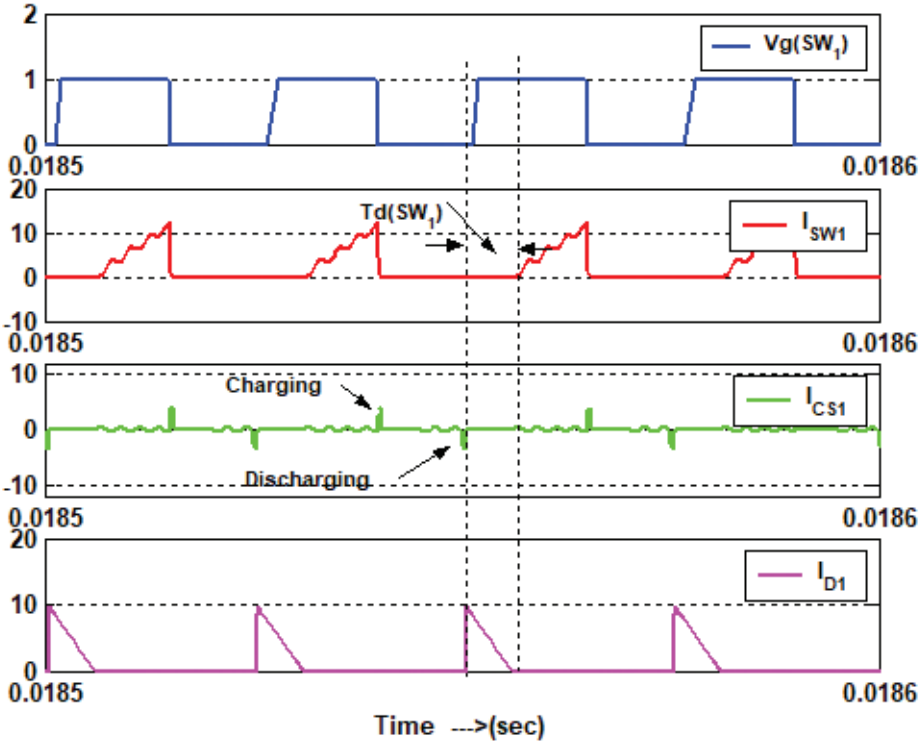


Figure 7. Waveforms of currents in SW_1, C_{S1} and D_1 with respect to the corresponding gate pulses V_g (SW_1) at a duty ratio of 60%.

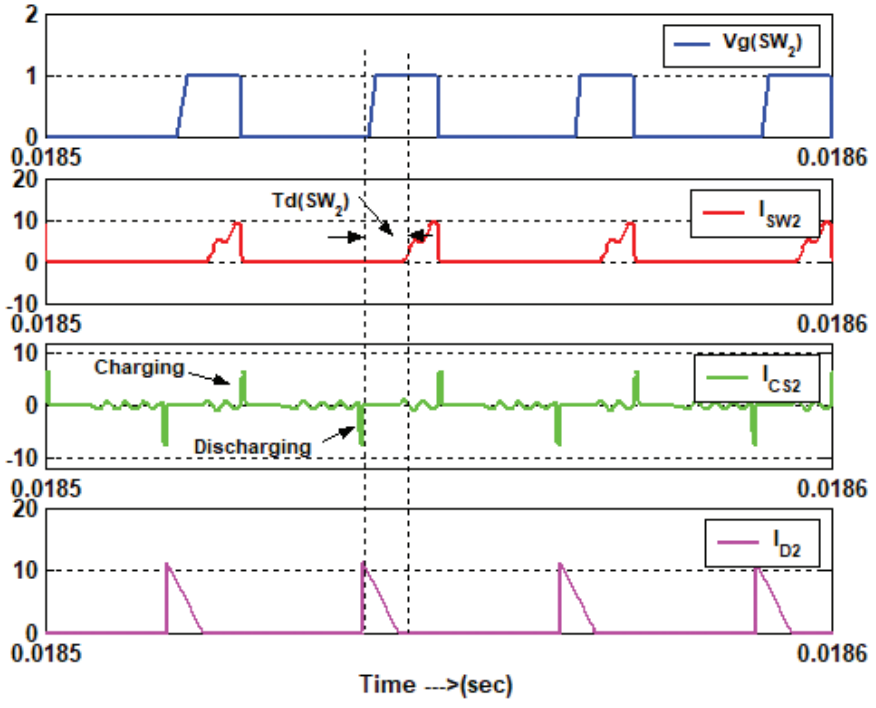


Figure 8. Waveforms of currents in SW_2, C_{S2} and D_2 with respect to the corresponding gate pulses V_g (SW_2) at a duty ratio of 60%.

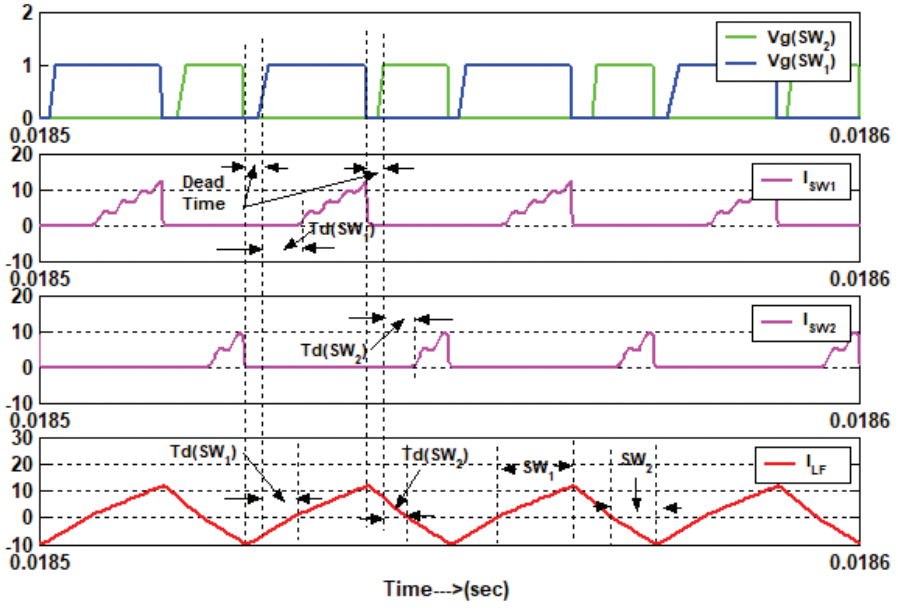


Figure 9. Waveforms of currents in SW_1 and SW_2, filter inductor L_F corresponding to their gating pulses of both switches at a duty ratio of 60% and switching frequency f_{sw} = 40 kHz.

The output voltage profile of the proposed converter is given in Table 1. It shows the comparison between the ideal buck converter and the proposed buck converter. So it is observed that the proposed converter gives the least difference from the ideal one (i.e., follows the equation [$V_o = k\ V_s$]). Hence, it shows close to the linear operation of an ideal buck converter with variation in duty ratios.

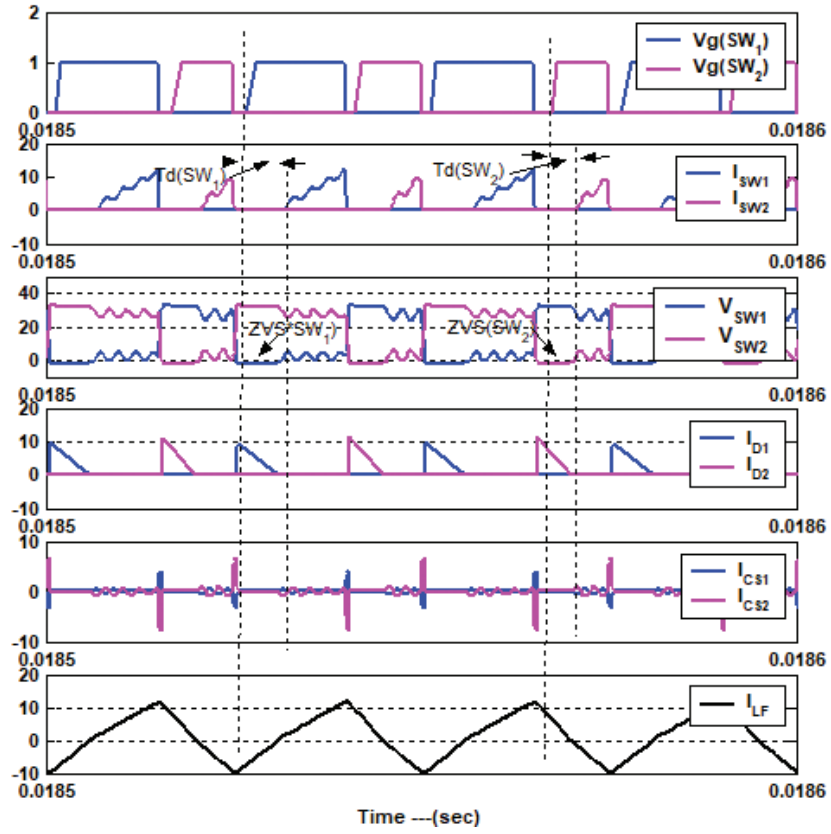


Figure 10. Waveforms of gate pulses, currents, voltage across switches (SW_1, SW_2), diode currents (D_1 and D_2), snubber capacitor currents (I_{CS1}, I_{CS2}) and current in filter inductor L_F corresponding to their gating pulses of both switches at a duty ratio of 60% and switching frequency of 40 kHz.

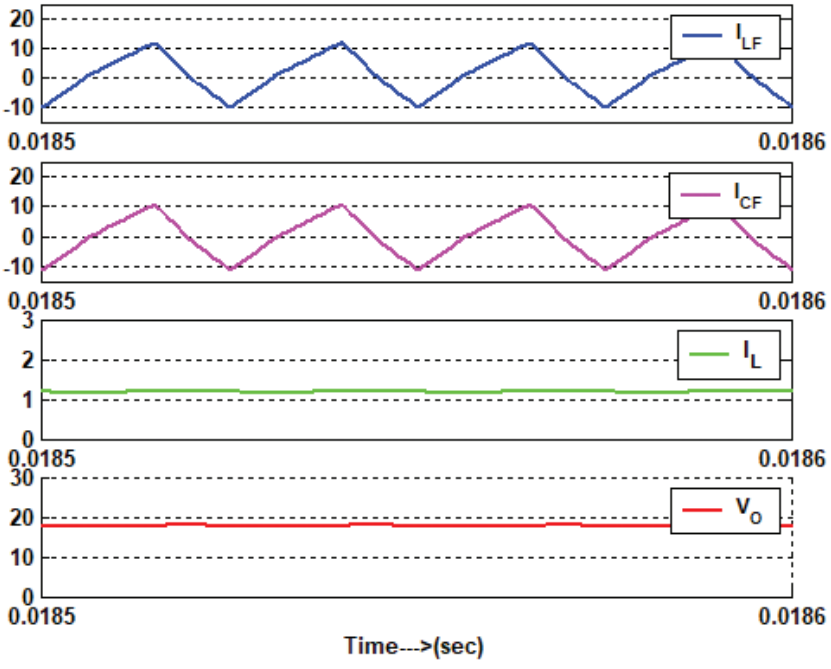


Figure 11. Waveforms of currents in filter inductor, filter capacitor, load and load voltage at a duty ratio of 60%.

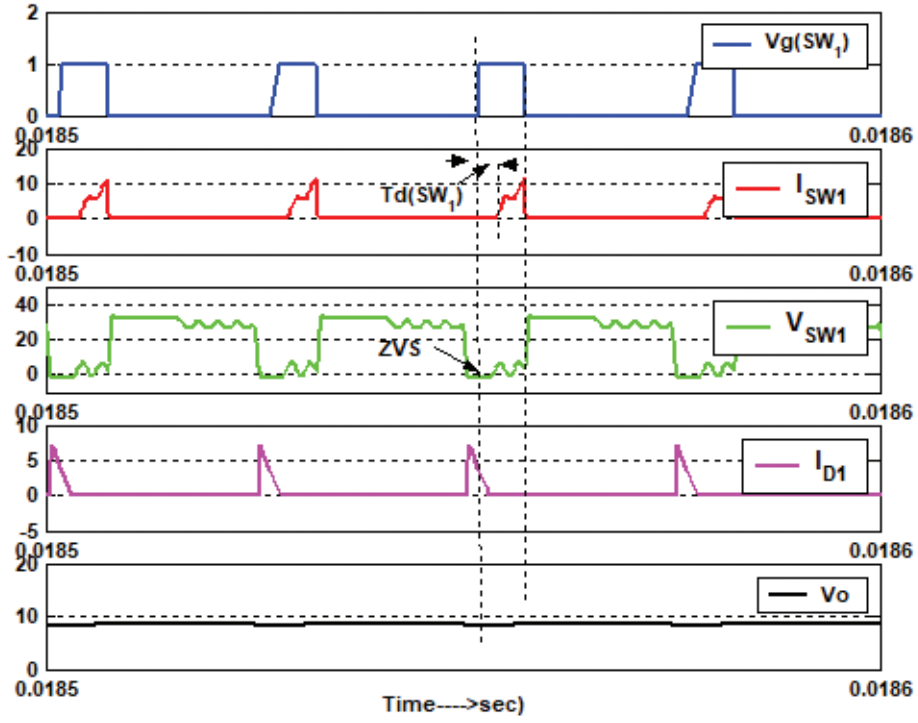


Figure 12. Waveforms of currents in I_{SW1}. I_{D1}, V_{SW1} and V_o at a duty ratio of 30%.

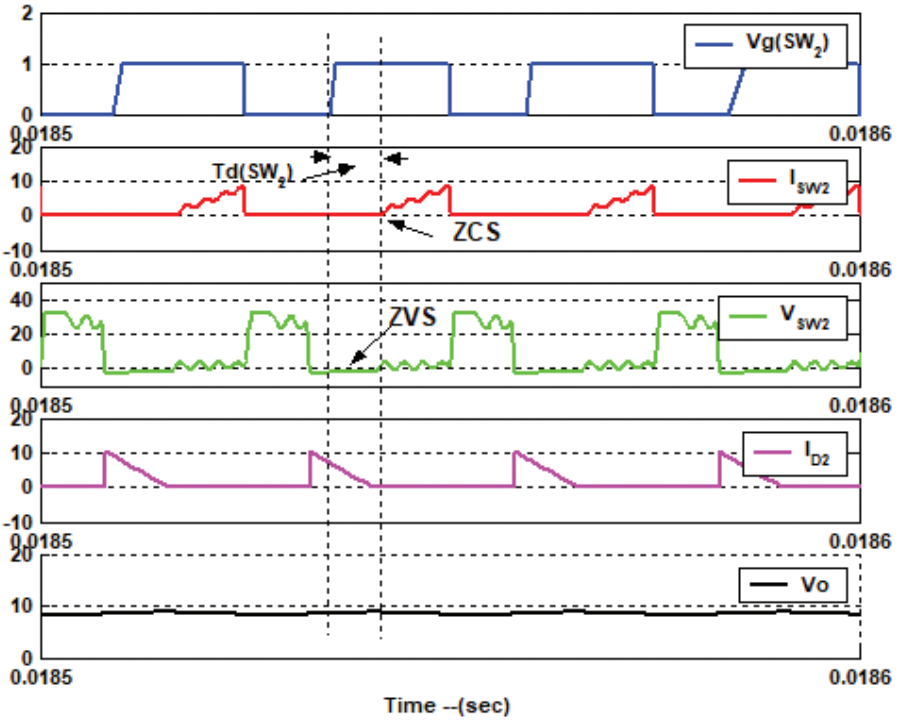


Figure 13. Waveforms of currents in I_{SW2}. I_{D2}, V_{SW2} and V_o at a duty ratio of 30%.

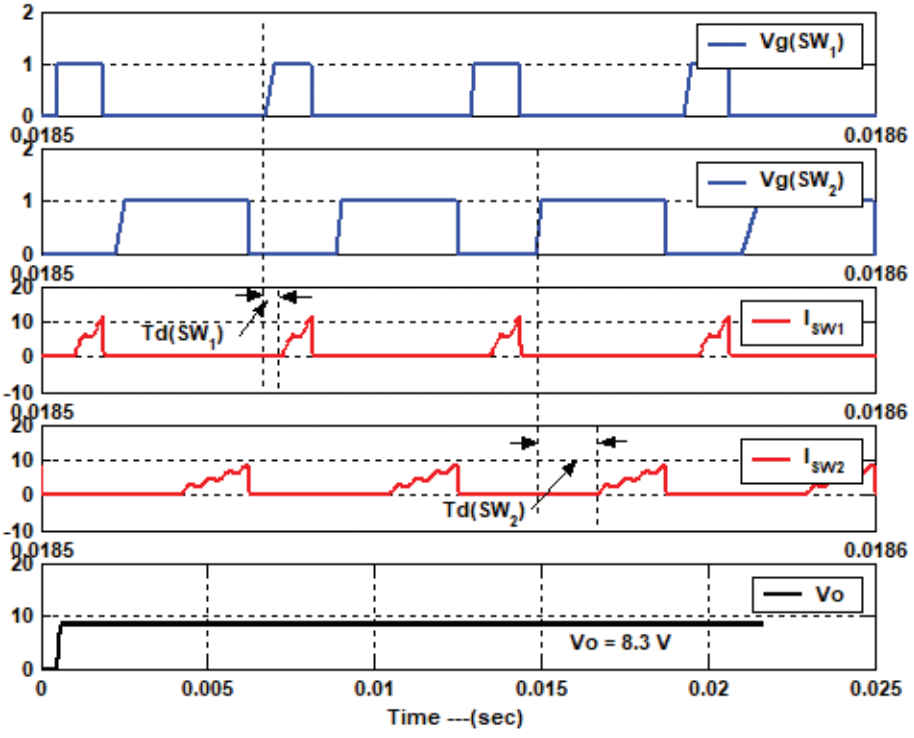


Figure 14. Waveforms of V_g (SW$_1$), V_g (SW$_2$), I_{SW1} and I_{SW2} for a few cycles and output voltage V_o at a duty ratio of 30% and input V_s = 30 V.

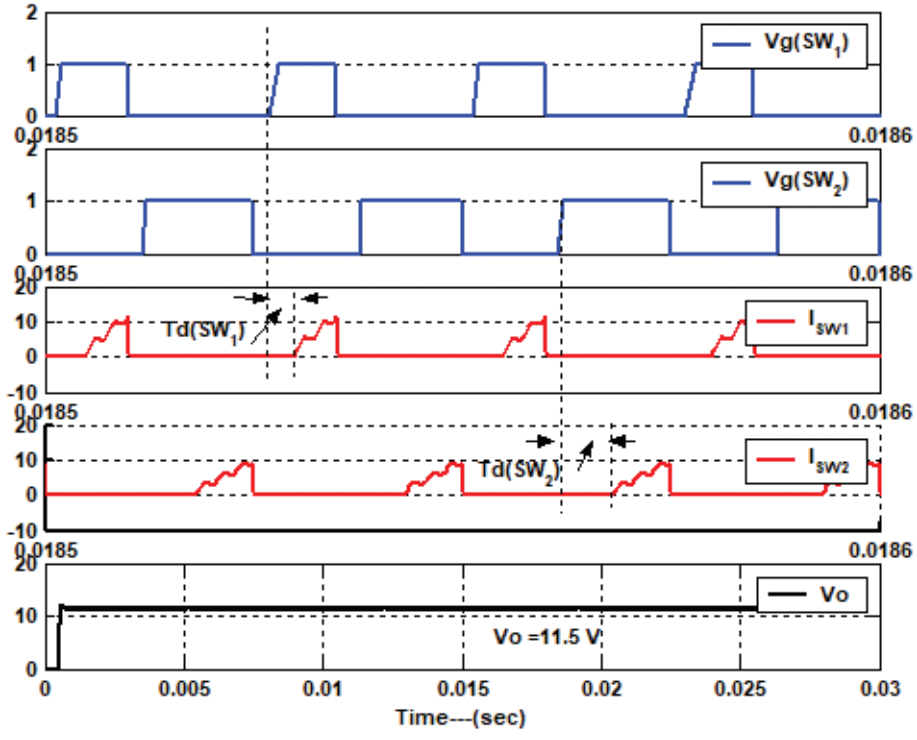


Figure 15. Waveforms of V_g (SW$_1$), V_g (SW$_2$), I_{SW1} and I_{SW2} for a few cycles and output voltage V_o at a duty ratio of 40% and input V_s = 30 V.

4.2. Experimental results

A prototype model is developed in the laboratory and experimented with the same parameters as considered in the simulation. The experimental results are given in Figures 16–18. Figures 16 and 17 show the experimental results of switch SW_1 and SW_2, respectively. Both figures show the current and voltage waveforms with respect to their gate pulses. These waveforms indicate that the currents in the switches are delayed with respect to the initiation of gating pulses. Simultaneously, it shows the ZVS on for the switches, followed by ZCS.

Figure 18 shows the experimental waveform of current in the filter inductor and load voltage (i.e., filter capacitor voltage) at a duty ratio of 60% with respect to gating pulses of both switches. The interval of dead time and delay time of both switches is reflected in the current waveform of the filter inductor. The current in the filter inductor shows bidirectional. So all these three experimental waveforms are justified with results obtained from simulation. The comparison between conventional and proposed half-bridge converters is given in Table 2. Also, Table 3 presents a comparison between the proposed structure and other structures published in past.

Table 1. Output voltage profile of the proposed buck converter for an input voltage of 30 V.

K (%)	Output voltage of buck converter (V)	Output voltage of proposed buck converter(V)
20	6	5.58
30	9	8.3
40	12	11.5
50	15	14.62
60	18	17.5
70	21	20.74
80	24	23.6
85	25.5	25.2

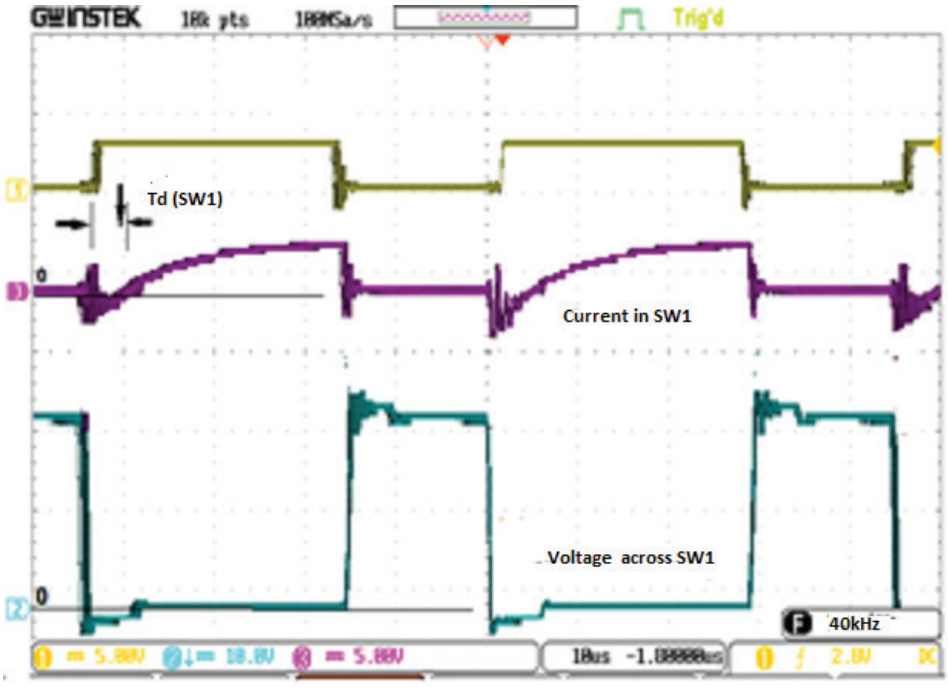


Figure 16. Waveforms of I_{SW1} and V_{SW1} at a duty ratio of 60%.

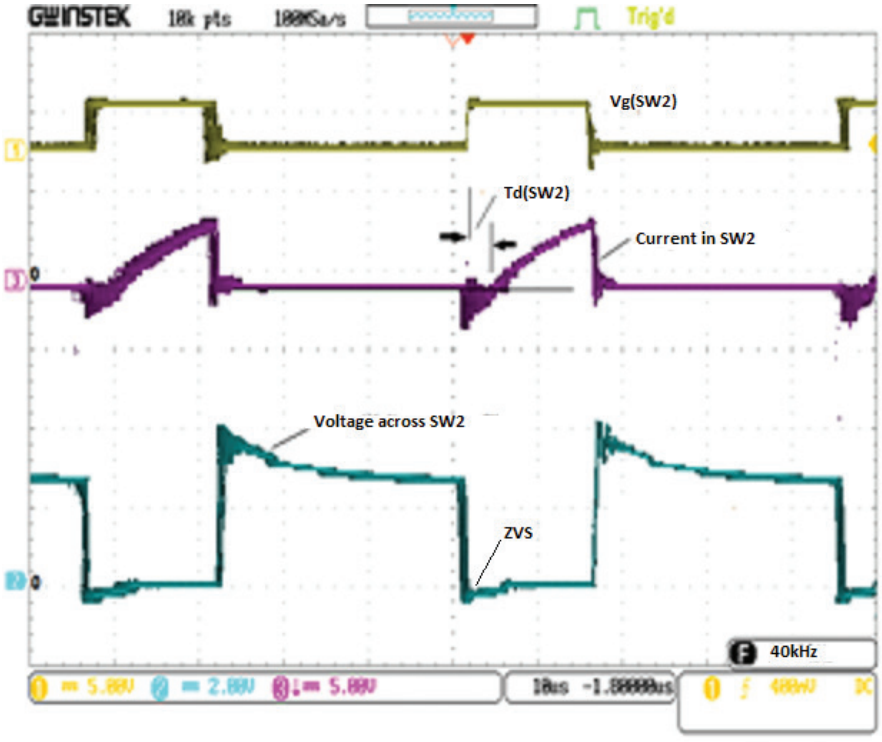


Figure 17. Waveforms of I_{SW2} and V_{SW2} at a duty ratio of 60%.

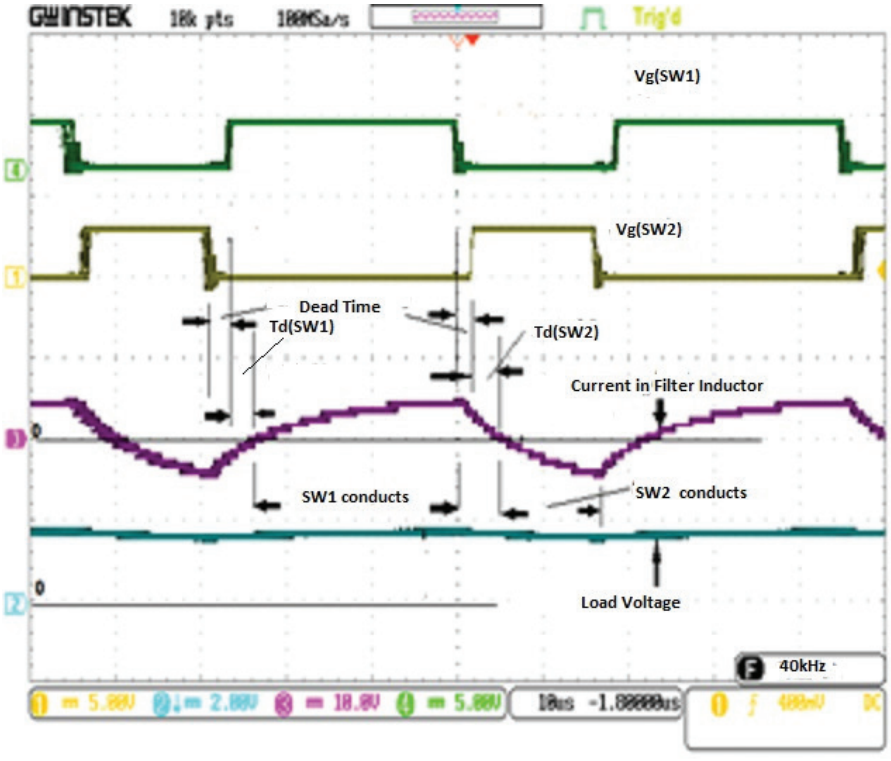


Figure 18. Waveforms of current in the filter inductor and load voltage with respect gating pulse of both switches at a duty ratio of 60%.

Table 2. Comparison between the conventional half-bridge and the proposed half-bridge structure.

Sl. No.	Conventional half-bridge converter	Proposed half-bridge structure
1	Snubber circuit contains three components (resistance, diode and capacitance)	The snubber circuit contains only capacitance
2	Filter ratings (L_F and C_F) are as per their designed values	A modified filter is required. The rating of the filter inductor is quite less, and the rating of the filter capacitor is very large as compared to a conventional one
3	Unidirectional current in the filter inductor	Bidirectional current in the filter inductor during each switching cycle
4	Hard switching of devices	Soft-switching of devices

Table 3. Performance comparison of various topologies.

Components	Yen and Chao	Khalili et al.	Montezerolghaem et al.	Proposed structure
Switches	4	2	2	2
Diodes	2	3	4	2
Inductors coupling inductors	2 1:2	1 No	4 1:1 (2)	1 No
Capacitors	1	5	4	3
ZVS/ZCS	ZVS	ZVS	ZVS	Turn on under ZVS and ZCS. Turn off under ZVS

ZCS, zero-current switching; ZVS, zero-voltage switching.

5. Conclusion

The idea of employing the suggested two-switch topology to achieve soft-switching is completely original and very different from previously suggested topologies. This topology is functioning satisfactorily under soft-switching on/off between specific duty-ratio ranges (i.e., 0.15 < = k < = 0.85). The dead time was introduced between switches to prevent short circuits over DC links and enable soft-switching of devices (i.e., by charging, discharging snubber capacitors and conduction of anti-parallel diodes). Bidirectional continuous current was discovered to flow through the filter inductor. Without dissipating through their respective switches, it was discovered that the snubber capacitors C_{S1} and C_{S2} return their energies to the source (i.e., while discharging) and load, respectively. The series and shunt switches turned on under both ZVS, followed by ZCS (i.e., ZVS due to conduction of anti-parallel diodes across switches and ZCS due to the delay in conduction of the switch). On the contrary, the switches were found to be turned off under ZVS due to its parallel snubber capacitors across them. The experimental results agree with the results obtained from the simulation. The proposed topology can be more suited to low to medium-power applications and can be extended to renewable applications.

Author's Contribution

Siddhartha Behera—research concept and design, collection and/or assembly of data, data analysis and interpretation, writing the article, critical revision of the article. Saroja Kumar Dash—research concept and design, collection and/or assembly of data. Manoj Kumar Sahu—research concept and design, collection and/or assembly of data, writing the article, critical revision of the article, final approval of the article.

References

Abbasian, S., Gohari, H. S., Farsjani, M., Abbaszadeh, K., Hafezi, H. and Filizadeh, S. (2022). Single-Switch Resonant Soft-Switching Ultra-High Gain DC-DC Converter with Continuous Input Current. *IEEE Access*, 10, pp. 33482–33491. doi: 10.1109/ACCESS.2022.3161456

Barreto, L. H. S. C., Coelho, E. A. A., Faris, V. J., de Oliveira, J. C., de Freitas, L. C. Jr. and Vieira, J. B. (2005). A Quasi-Resonant Quadratic Boost Converter Using a Single Resonant Network. *IEEE Transactions on Industrial Electronics*, 52(2), pp. 552–557. doi: 10.1109/TIE.2005.844255

Behera, S., Kumar, S., Behera, R., Panigrahi, B. P., Behera, R. K. and Bagarty, D. P. (2020). Regulated soft-switching power supply using buck-boost converter. *IEEE International Conference on Computational Intelligence for Smart Power System and Sustainable Energy (CISPSSE), 29–31 July 2020, Keonjhar, India*. pp. 29–31. doi: 10.1109/CISPSSE49931.2020.9212245

Cheng, X., Liu, C., Wang, D. and Zhang, Y. (2021). State-of-the-Art Review on Soft-Switching Technologies for Non-Isolated DC-DC Converters. *IEEE Access*, 9, pp. 119235–119249. doi: 10.1109/ACCESS.2021.3107861

Danyali, S. (2022). New Dual-Source High-Gain ZVS DC-DC Converter for Integrating Renewable Power Source and Battery Storage. *Journal of Electric Power System Research*, 213, pp. 1–10. doi: 10.1016/j.epsr.2022.108740

Do, H. L. (2010). A Soft-Switching DC/DC Converter with High Voltage Gain. *IEEE Transactions on Power Electronics*, 25(5), pp. 1193–1200. doi: 10.1109/TPEL.2009.2039879

Dobakhshari, S. S., Milimonfared, J., Taheri, M. and Moradisizkoohi, H. (2017). A Quasi-Resonant Current-Fed Converter with Minimum Switching Losses. *IEEE Transactions on Power Electronics*, 32(1), pp. 353–362. doi: 10.1109/TPEL.2016.2528893

Forouzesh, M. (2022). A novel soft-switched three-phase three-wire isolated AC-DC converter with power factor correction. *IEEE Applied Power Electronics Conference and Exposition (APEC)*, *20–24 March 2022, Houston, TX, USA*. doi: 10.1109/APEC43599.2022.9773554

Guan, Y., Cheng, Y., Yao, T., Wang, Y., Wang, W. and Xu, D. (2022). A High-Performance DC–DC Converter with Soft Switching Characteristic and High Voltage Gain. *IEEE Transactions on Power Electronics*, 37(10), pp. 12279–12288. doi: 10.1109/TPEL.2022.3172904

Gu, Y., Zhang, D. and Zhao, Z. (2014). Input Current Ripple Cancellation Technique for Boost Converter Using Tapped Inductor. *IEEE Transactions on Industrial Electronics*, 61(10), pp. 5323–5333. doi: 10.1109/TIE.2014.2300045

Hasanpour, S., Forouzesh, M., Siwakoti, Y. P. and Blaabjerg, F. (2021). A Novel Full Soft-Switching High-Gain DC/DC Converter Based on Three-Winding Coupled-Inductor. *IEEE Transactions on Power Electronics*, 36(11), pp. 12656–12669. doi: 10.1109/TPEL.2021.3075724

Hosseinzadeh, Z., Molavi, N. and Farzanehfard, H. (2019). Soft-Switching High Step-Up/Down Bidirectional DC–DC Converter. *IEEE Transactions on Industrial Electronics*, 66, pp. 4379–4386. doi: 10.1109/TIE.2018.2863216

Jahangiri, S., Delshad, M. and Vesali, M. (2022). A New Single-Switch ZCS Flyback-Forward Converter with High Power Density. *IETE Journal of Research*, 68(5), pp. 3428–3438. doi: 10.1080/03772063.2020.1768160

Kalahasthi, R. B., Ramteke, M. R., Suryawanshi, H. M. and Kothapalli, K. R. (2022). A High Gain Soft Switched DC–DC Converter for Renewable Applications. *International Journal of Electronics*, 110(8), pp. 1447–1467. doi: 10.1080/00207217.2022.2117423

Kalahasthi, R. B., Ramteke, M. R., Suryawanshi, H. M. and Singh, A. K. (2023). A ZVS-Based Non-Isolated High Step-Up DC–DC Converter With Low Voltage Stress for Renewable Applications. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 11(3), pp. 2793–2804. doi: 10.1109/JESTPE.2023.3237076

Khallili, S., Esteki, M., Packnezhad, M., Farzanehfard, H. and Khajehoddin, S. A. (2023). Fully Soft-Switched Non-Isolated High Step-Down DC–DC Converter with Reduced Voltage Stress and Expanding Capability. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 11(1), pp. 796–805. doi: 10.1109/JESTPE.2022.3180782

Lalitha, A. S., Chakraborty, S. and Kumar, S. S. (2022). A zero voltage switching based soft switching boost DC-DC converter for vehicle to grid applications with enhanced energy efficiency. *IEEE 3rd International Conference for Emerging Technology (INCET)*, *27–29 May 2022, Belgaum, India*. doi: 10.1109/INCET54531.2022.9824207

Li, H., Du, H., Zeng, Y., Qiu, Z., Jiang, X. and Chen, Z. (2022). A Modified Interleaved Capacitor Clamped DC–DC Converter with Non-Resonant Soft Switching. *IEEE Transactions on Power Electronics*, 37(10), pp. 12221–12236. doi: 10.1109/TPEL.2022.3163010

Li, F., Huo, C., Zhao, Z. and Qu, K. (2014). A novel soft-switching DC-DC converter with high-step-down conversion. *IEEE International Power Electronics and Application Conference and Exposition*, *Sanghai, China*. doi: 10.1109/ICEMS.2014.7013806

Li, W., Xu, D., Wu, B., Zhao, Y., Yang, H. and He, X. (2012). Zero-Voltage-Switching Dual-Boost Converter with Multi-Functional Inductors and

Improved Symmetrical Rectifier for Distributed Generation Systems. *IET Power Electronics*, 5(7), pp. 969–977. doi: 10.1049/iet-pel.2012.0031

Maulik, A., Pal, A. and Saha, S. S. (2020). A new soft-switched DC-DC buck converter with large step down ratio. *IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*. pp.1-6. doi: 10.1109/PEDES49360.2020.9379772

Mohammadi, M., Dehbashi, A., Gharehpetian, G. B., Khoshsaadat, A. and Mattavelli, P. (2021). A Family of Soft-Switching DC-DC Converters with Two Degrees of Freedom. *IEEE Transactions on Industrial Electronics*, 68(10), pp. 9398–9409. doi: 10.1109/TIE.2020.3021639

Mohseni, P., Hosseini, S. H. and Maalandish, M. (2020). A New Soft Switching DC-DC Converter with High Voltage Gain Capability. *IEEE Transactions on Industrial Electronics*, 67(9), pp. 7386–7398. doi: 10.1109/TIE.2019.2941130

Montazerolghaem, R., Adib, E., Semiromizadeh, J. and Wheeler, P. (2023). Zero-Voltage-Switching High-Step-Down Buck Converter with Continuous Output Current. *IEEE Transactions on Power Electronics*, 38(10), pp. 12886–12894. doi: 10.1109/TPEL.2023.3294492

Pakdel, M., Taheri, A. and Jalilzadeh, S. (2019). A Novel Soft Switching DC–DC Boost Converter with Higher Efficiency. *IETE Journal of Research*, 67(4), pp. 559–568. doi: 10.1080/03772063.2019.1565949

Pastor, M., Durdrik, J. and Michal, R. (2022). High-frequency soft-switching DC-DC converter with simple secondary turn-off snubber. *IEEE 20th International Power Electronics and Motion Control Conference* (*PEMC*), *25–28 September 2022, Brasov, Romania*. doi: 10.1109/PEMC51159.2022.9962897

Prabhala, V. A. K., Fajri, P., Gouribhatla, V. S. P., Baddipadiga, B. P. and Ferdowsi, M. (2016). A DC-DC Converter with High Voltage Gain and Two Input Boost Stages. *IEEE Transactions on Power Electronics*, 31(6), pp. 4206–4215. doi: 10.1109/TPEL.2015.2476377

Rashid, M. H. (2004). *Power Electronics Circuits, Devices and Applications*, 3rd ed. New Delhi: Pearson Publication, pp. 186–190.

Rathore, A. K., Patil, D. R. and Srinivasan, D. (2016). Non-Isolated Bidirectional Soft-Switching Current-Fed LCL Resonant DC/DC Converter to Interface Energy Storage in DC Microgrid. *IEEE Transactions on Industrial Applications*, 52(2), pp. 1711–1722. doi: 10.1109/TIA.2015.2498127

Siwakoti, Y. P., Blaabjerg, F., Loh, P. C. and Town, G. E. (2014). High Voltage Boost Quasi-Z-Source Isolated DC/DC Converter. *IET Power Electronics*, 7(9), pp. 2387–2395. doi: 10.1049/iet-pel.2013.0845

Wu, H., Lu, Y., Mu, T. and Xing, Y. (2015). A Family of Soft-Switching DC-DC Converters Based on a Phase-Shift-Controlled Active Boost Rectifier. *IEEE Transactions on Power Electronics*, 30(2), pp. 657–667. doi: 10.1109/TPEL.2014.2308278

Yan, Z., Li, J., Xu, S., Yang, N., Zeng, J., Liu, J., Wu, W., Hu, R. and Qi, H. (2023). Ripple-Free Bidirectional DC–DC Converter With Wide ZVS Range for Battery Charging/Discharging System. *IEEE Transactions on Industrial Electronics*, 70(10), pp. 9992–10002. doi: 10.1109/TIE.2022.3222659

Yen, W. and Chao, P. (2022). A ZVS Phase-Shift Full-Bridge Converter With Input Current Steering to Reduce EMI Noise. *IEEE Transactions on Power Electronics*, 37(10), pp. 11937–11950. doi: 10.1109/TPEL.2022.3170234

Zhou, M., Liu, C., Zhang, M., Mao, X. and Zhang, Y. (2023). High Step-Up Soft-Switching DC–DC Converter Integrated With Y-Source Network. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 11(3), pp. 3348–3358. doi: 10.1109/JESTPE.2023.3264984

Appendix

Assuming that the load has both resistance and inductance. In case the load is resistive, the inductance can be replaced by a very small value of nH/pH, so that the effect of load inductance can be ignored.

The initial voltages across Snubber capacitors are $V_{CS1O} = 0$ and $V_{CS2O} = V_s$.

Mode I

The current starts to flow linearly from zero through SW_1, L_F and a parallel combination of filter capacitor C_F and load

$$V_s = L_F \frac{\mathrm{di_{LF}}}{dt} + V_{\mathrm{CF}} \tag{1}$$

$$V_{CF} = L_L \frac{\mathrm{di}_L}{dt} + R_{\mathrm{L}} i_L \tag{2}$$

$$V_{CF} = -\frac{1}{C_F}\int i_{CF}\ \mathrm{dt} + V_{\mathrm{CFO}} = -\frac{1}{C_F}\int (i_{LF} - i_L)dt + \mathrm{V_{CFO}}, \tag{3}$$

where R_L, L_L, L_F and C_F are load resistance, load inductance, filter inductance and filter capacitor, respectively.

V_{CF} and V_{CFO} are the voltage and initial voltage ($t = 0$) across the filter capacitor, respectively.

These three equations can be transformed into state space form

$$\begin{bmatrix} di_{LF}/dt \\ dv_{CF}/dt \\ di_L/dt \end{bmatrix} = \begin{bmatrix} 0 & -1/L_F & 0 \\ -1/C_F & 0 & 1/C_F \\ 0 & 1/L_L & -R_L/L_L \end{bmatrix} \begin{bmatrix} i_{LF} \\ v_{CF} \\ i_L \end{bmatrix} + \begin{bmatrix} 1/L_F \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} V_S \end{bmatrix}. \tag{4}$$

Mode II

When SW_1 is turned off, C_{S1} comes in series with a filter inductor for charging.

$$V_s = L_F \frac{\mathrm{di_{LF}}}{dt} + V_{\mathrm{CS1}} + V_{\mathrm{CF}} \tag{5}$$

$$V_{CF} = L_L \frac{\mathrm{di}_L}{dt} + R_L i_L \tag{6}$$

$$V_{CF} = -\frac{1}{C_F}\int (i_{LF} - i_L)\mathrm{dt} + V_{\mathrm{CFO}} \tag{7}$$

$$V_{CS1} = -\frac{1}{C_{S1}}\int i_{CS1}\ \mathrm{dt} + V_{\mathrm{CS1O}} \tag{8}$$

$$V_{CS2} = -\frac{1}{C_{S2}}\int i_{CS2}\ \mathrm{dt} + V_{\mathrm{CS2O}} \tag{9}$$

$$V_S = V_{\mathrm{CS1}} + V_{\mathrm{CS2}} \tag{10}$$

$$V_{\mathrm{CS2}} = V_S - V_{\mathrm{CS1}}. \tag{11}$$

$$\text{On differentiating Eq. (10): } i_{\mathrm{CS1}} + i_{\mathrm{CS2}} = 0 \text{ and } i_{\mathrm{CS1}} = -i_{\mathrm{CS2}}\ or\ i_{\mathrm{CS2}} = -i_{\mathrm{CS1}} \tag{12}$$

From above Eq. (12), it indicates that as the C_{S1} charges, at the same rate C_{S2} discharges and vice versa.

So the state-space form can be built from Eqs (5)–(9)

$$\begin{bmatrix} di_{\mathrm{LF}}/\mathrm{dt} \\ dv_{\mathrm{CF}}/\mathrm{dt} \\ di_L/\mathrm{dt} \\ dv_{\mathrm{CS1}}/\mathrm{dt} \\ dv_{\mathrm{CS2}}/\mathrm{dt} \end{bmatrix} = \begin{bmatrix} 0 & -1/L_F & 0 & -1/L_F & 0 \\ -1/C_F & 0 & 1/C_F & 0 & 0 \\ 0 & 1/L_L & R_L/L_L & 0 & 0 \\ -1/C_{\mathrm{S1}} & 0 & 0 & 0 & 0 \\ 1/C_{\mathrm{S2}} & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{\mathrm{LF}} \\ v_{\mathrm{CF}} \\ i_L \\ v_{\mathrm{CS1}} \\ v_{\mathrm{CS2}} \end{bmatrix} + \begin{bmatrix} 1/L_F \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} [V_S]. \tag{13}$$

This mode will continue till V_{CS1} attains the input value V_s and $V_{CS2} = 0$.

Mode III

During this mode, the variables of snubber capacitor V_{CS1} and V_{CS2} are removed, and $V_s = 0$ and the relevant matrix is obtained using $V_s = 0$ in Eq. (4) as diode D_2 is conducting

$$\begin{bmatrix} di_{\mathrm{LF}}/\mathrm{dt} \\ dv_{\mathrm{CF}}/\mathrm{dt} \\ di_L/\mathrm{dt} \end{bmatrix} = \begin{bmatrix} 0 & -1/\mathrm{L_F} & 0 \\ -1/\mathrm{C_F} & 0 & 1/\mathrm{C_F} \\ 0 & 1/\mathrm{L_L} & -\mathrm{R_L}/\mathrm{L_L} \end{bmatrix} \begin{bmatrix} i_{\mathrm{LF}} \\ v_{\mathrm{CF}} \\ i_L \end{bmatrix} + \begin{bmatrix} 1/L_F \\ 0 \\ 0 \end{bmatrix} [0]. \tag{14}$$

During this mode, the current in the filter inductor starts decaying due to the free-wheeling action of diode D_2.

Mode IV

As the shunt switch SW_2 is closed during conduction of diode D_2, this switch does not conduct instantly, and hence the same state Eq. (14) continue to run till the current falls to zero or diode D_2 becomes reverse-biased.

Mode V

In this mode, the current in the filter inductor L_F reverses due to the discharging of stored energy in the filter capacitor across SW_2. So the state Eq. (14) continues to run till the gate signal is withdrawn from SW_2.

Mode VI

Since the gate signal is removed from SW_2, both snubber capacitors come into action. The snubber capacitor C_{S2} would start charging, and simultaneously C_{S1} would discharge. Hence, in state Eq. (13), the coefficients of dV_{CS1}/dt and dV_{CS2}/dt are to be interchanged in signs in its system matrix.

$$\begin{bmatrix} di_{\mathrm{LF}}/\mathrm{dt} \\ dv_{\mathrm{CF}}/\mathrm{dt} \\ di_L/\mathrm{dt} \\ dv_{\mathrm{CS1}}/\mathrm{dt} \\ dv_{\mathrm{CS2}}/\mathrm{dt} \end{bmatrix} = \begin{bmatrix} 0 & -1/L_F & 0 & -1/L_F & 0 \\ -1/C_F & 0 & 1/C_F & 0 & 0 \\ 0 & 1/L_L & R_L/L_L & 0 & 0 \\ 1/C_{\mathrm{S1}} & 0 & 0 & 0 & 0 \\ -1/C_{\mathrm{S2}} & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{\mathrm{LF}} \\ v_{\mathrm{CF}} \\ i_L \\ v_{\mathrm{CS1}} \\ v_{\mathrm{CS2}} \end{bmatrix} + \begin{bmatrix} 1/L_F \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} [V_S]. \tag{15}$$

This mode will continue till the snubber capacitors C_{S2} charge to the source voltage and C_{S1} discharges to zero because of negative current in the filter inductor.

Mode VII

As the potential across SW_1 falls to zero due to the previous action, the diode D_1 across SW_1 starts conducting due to the still existing negative current in the filter inductor. The state space Eq. (4) is utilised without any change.

$$\begin{bmatrix} di_{\mathrm{LF}}/\mathrm{dt} \\ dv_{\mathrm{CF}}/\mathrm{dt} \\ di_L/\mathrm{dt} \end{bmatrix} = \begin{bmatrix} 0 & -1/L_F & 0 \\ -1/C_F & 0 & 1/C_F \\ 0 & 1/L_L & -R_L/L_L \end{bmatrix} \begin{bmatrix} i_{\mathrm{LF}} \\ v_{\mathrm{CF}} \\ i_L \end{bmatrix} + \begin{bmatrix} 1/L_F \\ 0 \\ 0 \end{bmatrix} [V_S]. \tag{16}$$

As diode D_1 continues to conduct during this mode, energy feedback occurs for a short interval of this mode.

Mode VIII

During this mode, the SW_1 is turned on, but it remains in the off state, as the diode D_1 across it still continues to conduct. This state Eq. (16) is allowed to run till D_1 becomes reverse-biased due to the fall of current in the filter inductor to zero. After this, the switching cycle is completed and repeats with Mode I again.