

A High-Gain, High-Bandwidth, Bidirectional Discrete GaN-Based SyncFET dv/dt Sensor for MHz Power Converters

Research paper

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Received: 18 August, 2025; Received in the revised form: 24 September, 2025; Accepted: 15 October, 2025

Abstract: This paper presents a high-gain, high-bandwidth discrete dv/dt sensing and control architecture for megahertz gallium nitride (GaN)-based power converters. In conventional capacitor-only dv/dt sensing, the external sensing capacitor must remain smaller than the device's reverse transfer capacitance to avoid loading effects, which inherently limits current gain and yields weak feedback signals. To overcome this constraint, the proposed approach introduces a synchronous GaN field-effect transistor (SyncFET) configured as a current amplifier, which boosts the weak capacitor current while preserving high-bandwidth operation. The amplified feedback current is processed by an active gate driver (AGD), realised with discrete GaN devices, that provides the necessary gain and bandwidth for precise dv/dt regulation. Together, the SyncFET and AGD form a dual-stage amplification system that enables effective dv/dt control without large sensor capacitance, high bus voltage or complex IC integration. Simulation and experimental validation in a 24 V, 10 MHz buck converter demonstrate that the combined SyncFET-AGD circuit reduces turn-on dv/dt from 15 V/ns to 10 V/ns while lowering switching loss by 16.7% compared with the conventional passive control. These results confirm that the proposed discrete gate-driving strategy mitigates the limitations of capacitor-only dv/dt sensing, offering dv/dt suppression and enhanced reliability in compact GaN-based converters.

Keywords: GaN • synchronous capacitive dv/dt sensor • high-frequency power converters • active gate driver • dv/dt control

1. Introduction

The push towards miniaturisation and efficiency in power electronics has driven the adoption of megahertz (MHz) switching converters, powered by gallium nitride (GaN) devices. As wide-bandgap (WBG) semiconductors, GaN transistors offer high-speed switching with reduced conduction and switching losses, improved thermal performance and reduced size, benefits that are particularly valuable in applications including electric mobility, renewable energy integration and precision motor control (Jones et al., 2016; Ma and Gu, 2019). However, the same fast-switching transitions (dv/dt in the tens to hundreds of V/ns) introduce significant design challenges. These include elevated electromagnetic interference (EMI), stress on isolation barriers, parasitic turn-on, crosstalk and common-mode noise, all of which degrade system reliability and performance (Jiang et al., 2021; Qin et al., 2024; Yu et al., 2023). To preserve the benefits of MHz operation, especially in space- and weight-constrained systems, it is crucial to actively and efficiently regulate dv/dt .

Conventional passive techniques, such as gate resistors and gate-source (GS) capacitors, reduce dv/dt but introduce trade-offs. Gate resistors slow switching, increase losses and degrade transient response, while external

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GS capacitors can lead to excessive gate delay, high peak gate currents and false triggering due to the low input capacitance of GaN transistors (Zhao et al., 2021). These limitations make passive dv/dt control unsuitable for MHz-scale GaN converters. To enable closed-loop dv/dt control, recent studies have explored capacitive sensing circuits using a small external sense capacitor (C_s) to emulate the gate-drain capacitance and generate a dv/dt-proportional signal (Groeger et al., 2017). However, achieving accurate sensing at MHz frequencies requires the C_s to withstand high voltages, exhibit minimal delay and deliver high gain, despite its low capacitance (<1 pF), as it should remain below the GaN's reverse transfer capacitance (C_{RSS}).

Various sensing methods, ranging from discrete bipolar junction transistors (BJTs) (Sun et al., 2016) to complementary metal–oxide–semiconductor (CMOS)-integrated sensors (Bau et al., 2020) and active gate drivers (AGD) (Kemeng et al., 2024; Zhu et al., 2021), have advanced dv/dt control. While integrated solutions offer performance advantages, they often suffer from limited flexibility, high-voltage handling issues and vulnerability to common-mode transients due to complex level shifters. Other methods, such as Miller plateau tracking (Chen and Ma, 2021; Yang et al., 2024) and N-channel laterally diffused metal-oxide-semiconductor (NLDMOS)-based double-edge detectors (Liu et al., 2024), have improved response time and EMI performance but at the cost of circuit complexity and limited reconfigurability.

This paper tackles these challenges by introducing a high-gain, high-bandwidth, bidirectional discrete synchronous GaN field-effect transistor (SyncFET)-based dv/dt sensor integrated with a fully discrete AGD, enabling real-time dv/dt regulation in megahertz GaN power converters. The proposed SyncFET-based sensor overcomes the limitations of passive resistor-capacitor (RC) methods and integrated ICs by offering the following:

- (a) High-gain dv/dt detection using a compact 0.1 pF C_s under low-voltage operation;
- (b) Bidirectional high-speed sensing for both rising and falling edges of switching transitions;
- (c) Seamless integration with a discrete AGD architecture that enables fast, dynamic dv/dt regulation without level shifters or complex ICs.

The AGD actively regulates turn-on dv/dt using the sensed signal, thereby improving switching performance, reliability and reducing switching losses. Since dv/dt directly influences EMI generation, the proposed approach may have the potential to improve EMI performance, although detailed EMI testing is left for future work. Unlike conventional AGDs, the proposed driver offers MHz-speed operation with improved responsiveness, modularity and immunity to common-mode transients.

The remainder of this paper is organised as follows: Section 2 presents the design of the proposed SyncFET-enhanced dv/dt sensor and its integration with a discrete AGD for turn-on dv/dt suppression. Section 3 presents simulation and experimental validation of the sensor-AGD system in an MHz GaN converter. Section 4 analyses key performance metrics, including dv/dt suppression, gain, system stability and switching loss reduction. Section 5 concludes the paper by summarising the key findings and highlighting potential avenues for future research.

2. Methodology

2.1. Introduction to dv/dt sensor in GaN power converter circuits

In conventional configurations, a capacitor-based dv/dt sensor regulates the switching profile of power devices, particularly in GaN circuits, by producing a feedback current proportional to the dv/dt during switching transients (Figure 1). This current is then supplied to the AGD to modulate the switching behaviour.

The inherent gate-drain capacitance (C_{GD}) generates current i_{CM} (see Eq. (1)) due to the drain-source slew rate $\left(\frac{d_{V_{DS}}}{d_t}\right)$. This approach has been successfully demonstrated in laterally diffused metal-oxide-semiconductor (LDMOS) transistors, which utilise their inherent capacitances to measure dv/dt. However, GaN devices, unlike LDMOS, pose challenges for dv/dt sensing due to smaller parasitic capacitances and rapid switching, which introduce noise and instability. To enhance feedback current (i_{FB}) in GaN devices, an external sense capacitor C_s is added, generating i_{FB} as shown in Eq. (2):

$$i_{CM} = C_{GD} \cdot \frac{d_{V_{DS}}}{d_t} \quad (1)$$

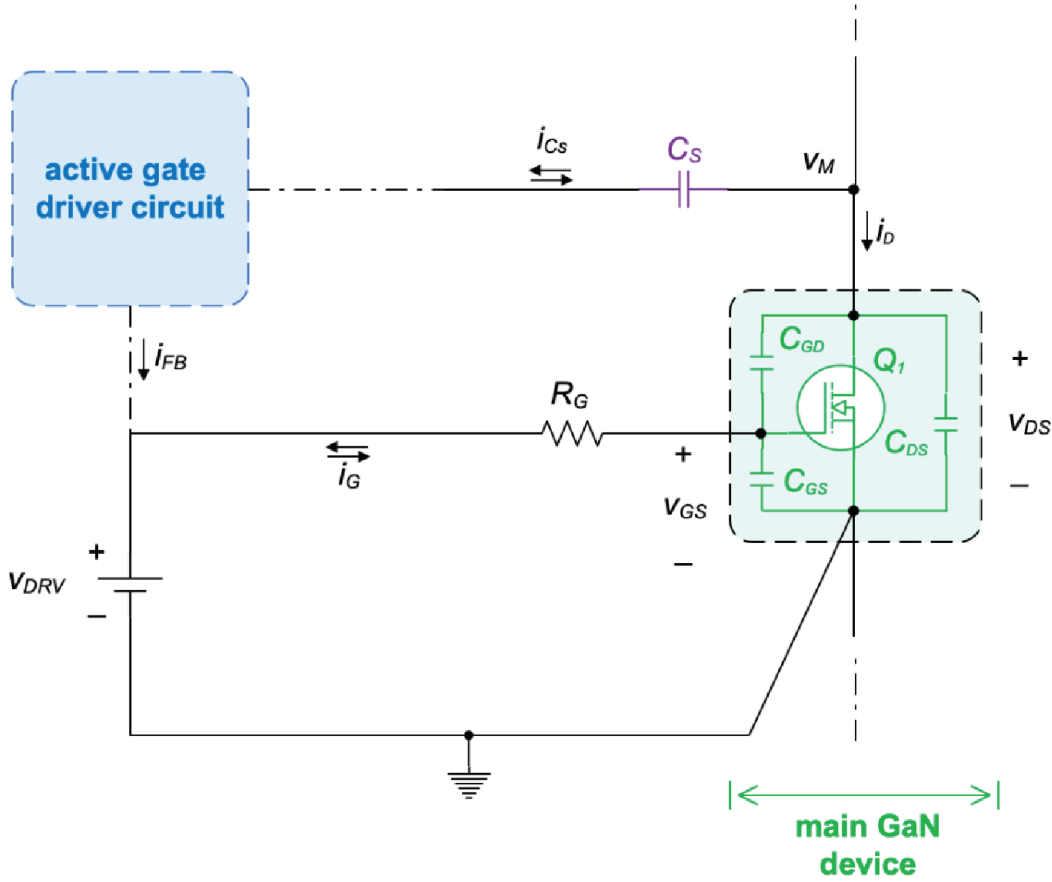


Figure 1. Traditional capacitor-based dv/dt sensor circuit for dv/dt control in GaN devices. GaN, gallium nitride.

$$i_{FB} = \pm G \cdot C_s \cdot \frac{d v_{DS}}{d t} \quad (2)$$

where G is a tunable feedback gain. During turn-on, G is negative, and during turn-off, it is positive. In practice, the sensing capacitor (C_s) is selected to be much smaller than the GaN device's reverse transfer capacitance (C_{RSS}), typically <10 pF. As a result, increasing C_s to achieve higher current gain is impractical for GaN power converters. Therefore, dv/dt sensors for GaN must employ high gain to produce adequate feedback currents.

2.2. Development of proposed discrete synchronous capacitive dv/dt sensor for GaN devices

The proposed synchronous capacitive dv/dt sensor builds upon the conventional capacitor-based approach by incorporating a GaN field-effect transistor (SyncFET) configured as a common-source amplifier (CSA), as illustrated in Figure 2, thereby significantly enhancing the feedback gain.

The SyncFET dv/dt sensor circuit was constructed using four main building blocks: a CSA stage, a charge pump network, a source degeneration resistor and the sensing capacitor.

2.2.1. CSA (SyncFET stage)

The SyncFET operates in saturation as a CSA. It converts the displacement current generated by the sensing capacitor into an amplified drain current, which serves as the feedback signal for the AGD.

2.2.2. Charge pump network

A compact charge pump, realised with two diodes (D_1 and D_2) and two capacitors (C_1 and C_2), establishes the required bias conditions. The anode of D_1 is tied to V_{CC} , with its cathode connected to one side of C_1 . The other side of C_1 connects to the gate of the main GaN device. The junction between C_1 and D_1 also connects to the anode

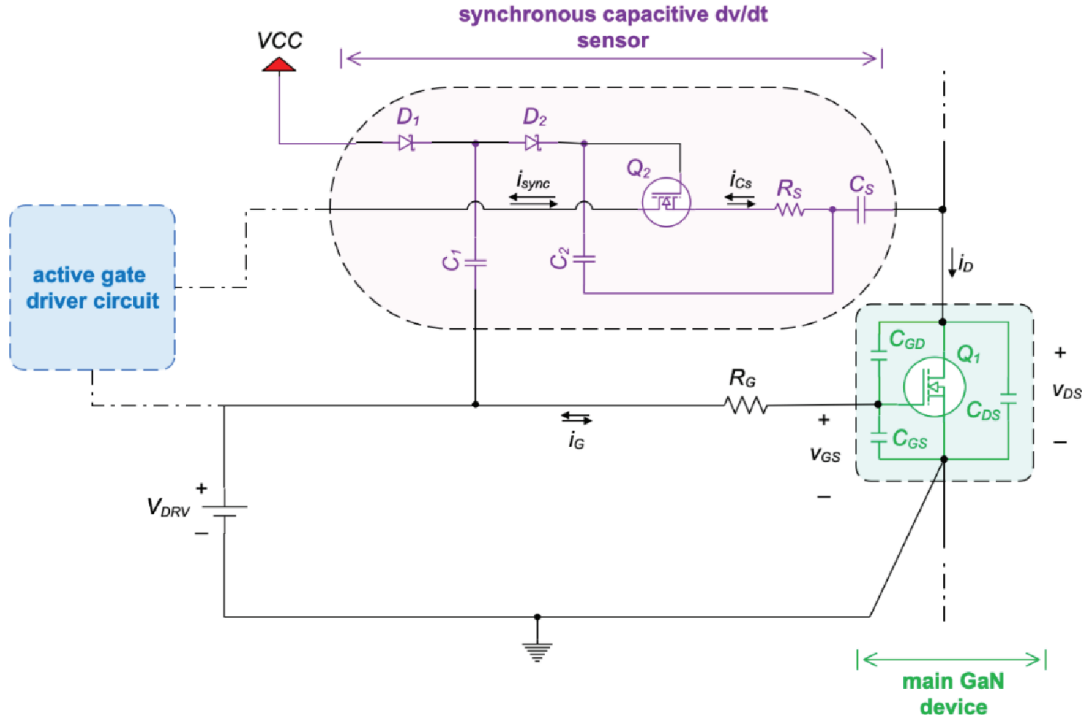


Figure 2. Proposed synchronous capacitive dv/dt sensor circuit for dv/dt control in MHz frequency GaN devices. GaN, gallium nitride; MHz, megahertz.

of D_2 . The cathode of D_2 is tied to one side of C_2 , whose other side is connected to the source of the SyncFET. The junction of D_2 and C_2 is further connected to the gate of the SyncFET, providing its gate bias. During the off-time, D_1 conducts and charges C_1 to V_{CC} . During the on-time, D_1 is reverse-biased and the stored charge in C_1 is transferred to C_2 through D_2 (forward-biased). This action biases the SyncFET gate while ensuring it remains at a positive potential.

2.2.3. Source degeneration resistor (R_s)

A resistor is placed at the SyncFET source to stabilise the amplifier, improve linearity and allow the sensed current to be accurately reflected as a feedback control signal.

2.2.4. Sensing capacitor (C_s)

A small capacitor couples the high-frequency voltage transients at the switching node into the SyncFET source. The resulting displacement current interacts with the source resistor, producing voltage variations that are amplified by the SyncFET.

Through this configuration, the dv/dt of the main GaN device is synchronously sensed and converted into a feedback current, enabling active regulation of switching transients. This detailed construction clarifies the implementation of the schematic shown in Figure 2.

2.3. Operating principle of the proposed synchronous capacitive dv/dt sensor circuit

The goal is to convert the high dv/dt at the switch node into a strong, controllable current signal that can be used for active dv/dt regulation. During switching transients, C_s generates a current proportional to the voltage slope at the drain of the low-side GaN FET (see Eq. (2)). This current flows into the source terminal of the SyncFET, which operates as a voltage-controlled current source. A charge pump maintains a constant gate voltage (V_{G_sync}) above the device threshold (V_{TH}), determined by the supply voltage V_{CC} , which is referenced to the system ground. This biasing ensures that the SyncFET remains in the saturation region during operation. Since

the source voltage (V_{S_sync}) varies with the transient current from the capacitor sensor, the GS voltage (V_{GS_sync}) also varies dynamically, producing a modulated drain current (i_{sync}).

The SyncFET thus acts as a current amplifier. The drain current, i_{sync} , becomes the sensor output, feeding into the high-output-impedance AGD, which acts as an active load. This configuration achieves high current gain while voltage gain remains negligible. The current gain (A_i) of the SyncFET stage is given in Eq. (3):

$$A_i = \frac{\Delta i_{sync}}{\Delta V_{IN}} = \frac{gm \times V_{GS_sync}}{V_{GS_sync}} = gm \quad (3)$$

where $V_{IN} = V_{GS_sync}$ represents the sensor input voltage, and gm denotes the transconductance of the GaN device.

To improve linearity and control the gain, a source degeneration resistor, R_s , is introduced, modifying the effective input voltage as shown in Eq. (4):

$$V_{IN} = V_{GS_sync} - I_s \times R_s \quad (4)$$

where I_s is the current through R_s .

The resulting effective current gain is shown in Eq. (5):

$$A_i = \frac{\Delta I_D}{\Delta V_{IN}} = \frac{\frac{gm}{1+gm \times R_s} \times V_{IN}}{V_{IN}} = \frac{gm}{1+gm \times R_s} \quad (5)$$

This gain can be tuned by adjusting V_{CC} or R_s , keeping V_{GS_sync} within the safe operating limit for GaN devices (typically <6 V). The bidirectional nature of the GaN SyncFET ensures symmetrical response to positive and negative dv/dt transients, making the sensor suitable for high-speed dv/dt sensing during transients in MHz-frequency power converters.

2.4. Characterisation of proposed SyncFET dv/dt sensor circuit with an AGD: turn-on dv/dt control

This paper addresses turn-on dv/dt control in MHz GaN converters, a critical factor in addressing issues such as crosstalk, EMI, device stress and reliability (Bau et al., 2020). While turn-off dv/dt is also important, in GaN devices it causes minimal energy loss due to high transconductance and short crossover time (Lee et al., 2016). Although this paper focuses on turn-on dv/dt control, it is useful for turn-off dv/dt control as the proposed SyncFET dv/dt sensor circuit allows for bidirectional dv/dt sensing.

Figure 3 illustrates the proposed dv/dt sensor connected to an AGD. While Figure 2 presents the standalone SyncFET-based dv/dt sensor circuit, Figure 3 shows its integration with a modified GaN-based current-mirror AGD as proposed in Banzie et al. (2025). In this configuration, the amplified feedback current generated by the dv/dt sensor is injected into the AGD input stage, enabling closed-loop regulation of the turn-on transition. This combined setup highlights how the sensor circuit interfaces with the gate driver to achieve practical dv/dt control in MHz GaN converters.

During turn-on, a rapid negative dv/dt across the capacitor dv/dt sensor induces a negative current (i_{CS}), which flows out of the source of the SyncFET. This lowers the V_{S_sync} , thereby increasing the V_{GS_sync} (as $V_{GS_sync} = V_{G_sync} - V_{S_sync}$); V_{G_sync} is a fixed positive voltage set by the charge pump circuit. The increase in V_{GS} induces i_{sync} , governed by the transistor's transfer characteristics in the saturation region, and flows into the AGD opposite to the i_{CS} (see Figure 5). Implemented as a cascode current mirror topology employing four discrete n-channel GaN devices, the AGD offers high impedance and high bandwidth, avoiding significant capacitive loading on the gate while enabling fast, precise control (Banzie et al., 2025). The current mirror stabilises the SyncFET's output and effectively mirrors the amplified dv/dt-induced current.

During turn-on, a portion of the driver current, i_s , is injected into Q_5 , increasing its drain current i_{D5} and voltage V_{D5} . Since the equivalent output resistance seen by Q_5 , R_{D5} is small, $V_{D5} \approx V_{GS}$ (GS voltage of the main GaN device). The total sink current applied by Q_5 is shown in Eq. (6):

$$i_{R5} = i_s + i_{FB} \quad (6)$$

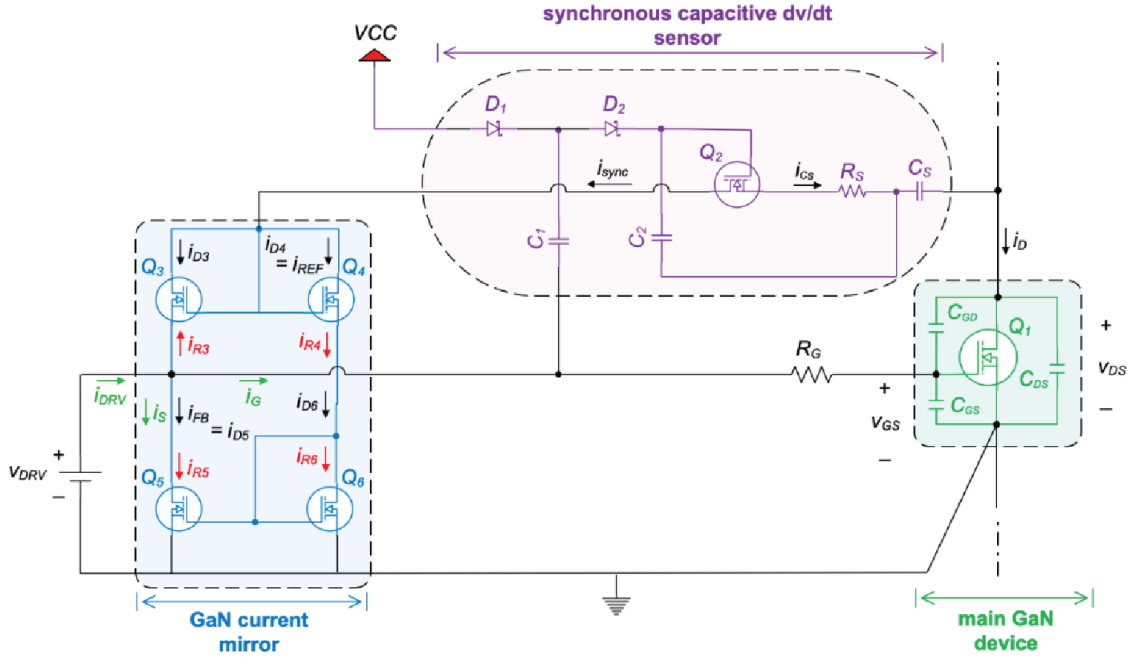


Figure 3. The proposed SyncFET dv/dt sensor and AGD for turn-on dv/dt control. AGD, active gate driver; GaN, gallium nitride; SyncFET, synchronous GaN field-effect transistor.

where i_{R5} is the resultant sink current, i_s is the sink current derived from the driver output, and i_{FB} is the feedback current due to the SyncFET dv/dt sensor. Simultaneously, the rise in V_{DS} raises the source voltage of Q_3 , reducing its GS voltage (V_{GS3}) and biasing it into third-quadrant mode. This produces a second sink current i_{R3} from Q_3 , flowing opposite to i_{FB} but contributing to gate current reduction. The combined dv/dt control law is provided in Eq. (7):

$$i_G = i_{DRV} - (i_{R5} + i_{R3}) \quad (7)$$

where i_G is the net gate current and i_{DRV} is the driver's source current. The SyncFET therefore enhances the current-sinking capability of the AGD, improving dv/dt reduction during turn-on. The SyncFET dv/dt sensor with the AGD addresses the following key CSA limitations:

- The Miller effect is minimised by GaN's small C_{GD} , boosting bandwidth.
- Low C_{GS} and C_{DS} reduce capacitive loading, improving frequency response.
- Source degeneration improves linearity and bandwidth by reducing gain.
- Active load (AGD) provides high output impedance, increasing the gain-bandwidth product and current transfer efficiency.

2.5. SyncFET-AGD circuit simulation setup and implementation for turn-on dv/dt control in MHz frequency power converters

The proposed SyncFET-AGD circuit was first evaluated in simulation to validate its dv/dt control capability before hardware prototyping. Simulations were conducted in PSpice using manufacturer-provided GaN transistor models that incorporate parasitic capacitances and gate charge dynamics. The set-up replicated the test circuit parameters summarised in Table 1: a 24 V DC bus, 10 MHz switching frequency, EPC2106 GaN half-bridge as the main device, EPC2037 SyncFET, TI LMG1210 driver integrated circuit (IC), 3.5 μ H load inductor and 120 mA load current. A 0.1 pF external sensing capacitor and 4 Ω source degeneration resistor were employed to implement the

proposed dv/dt sensor. The simulation was run under steady-state conditions, and dv/dt was extracted during turn-on transitions for comparison with experimental measurements.

The circuit was validated at 10 MHz, representative of emerging industrial GaN-based converter applications (Chen and Ma, 2021; Li et al., 2019; Wang et al., 2020; Yan et al., 2020). While lower frequencies simplify the design due to reduced parasitics, higher frequencies demand tighter PCB layout control. The 10-MHz benchmark aligns with emerging industrial trends and provides a practical test case.

Simulation validation using PSpice models with estimated parasitics is followed by hardware implementation on a custom four-layer PCB. Signal and power traces are routed on the outer layers, with inner ground planes minimising loop inductance. An EPC2106 GaN half-bridge is used for switching, chosen for its compact layout and reduced parasitics. Gate drivers and decoupling capacitors are positioned close to the half-bridge to limit inductive effects.

The dv/dt sensor targets the low-side GaN FET, using a 0.1 pF sensing capacitor to ensure high bandwidth and minimal loading. The EPC2037 is selected as the SyncFET for its fast-switching characteristics and low input capacitance, while a 4 Ω source degeneration resistor balances gain and stability. Supporting components are placed tightly around the sensing node to maintain signal integrity. A 2.5 V supply ensures that the SyncFET operates within safe GS limits.

The AGD employs a modified cascode current mirror built from two EPC2106 half-bridges to enhance mirroring accuracy and high-frequency performance. Component values were optimised through simulation sweeps and experimentally validated, as summarised in Table 1. Despite a nominal 24 V input, turn-off transients can push V_{DS} up to ~43 V (Figure 11), so both EPC2037 and EPC2106 are selected for their 100 V rating to ensure reliability under MHz switching.

The prototype is realised using discrete GaN FETs (EPC2106, EPC2037), a commercial driver IC (TI LMG1210) and off-the-shelf passives (e.g. Vishay, Würth inductor). While this discrete implementation increases printed circuit board (PCB) footprint and cost compared with monolithic driver ICs, it offers modularity, higher breakdown margins and flexibility for MHz operation. Looking ahead, with ongoing GaN IC integration trends, the SyncFET–AGD concept could be embedded into driver ICs, reducing cost and improving manufacturability. AGD, active gate driver; GaN, gallium nitride; MHz, megahertz; SyncFET, synchronous GaN field-effect transistor.

Table 1. Prototype circuit components, parameters and measurement set-up

Name	Parameter
Bus voltage (DC)	24 V
Operating frequency	10 MHz
Main transistors	100 V (EPC2106)
Current mirror transistors	100 V (EPC2106)
SyncFET	100 V (EPC2037)
Reverse transfer capacitance (C_{RSS})	0.5 pF
Sensing capacitor (C_S)	0.1 pF (Vishay VJ0402D0R1VXBAJHT)
Degeneration resistor (R_S)	4 Ω
Charge pump circuit supply (V_{cc})	2.5 V
Gate drive voltage (V_{DRV})	4.5 V
Gate resistor (R_G)	7 Ω
Gate driver IC	200 V (Texas Instruments LMG1210)
Load inductor	3.5 μ H (Würth Elektronik 744771003)
Load current (i_L)	120 mA
Oscilloscope	UNI-T UPO3352E (350 MHz 2.5 GSa/s)
Probe	UT-P08A (350 MHz)

3. Results

3.1. Simulation results

Simulation validates the proposed SyncFET–AGD combo for turn-on dv/dt regulation. As shown in Figure 4, increasing V_{CC} to 5 V causes V_{GS_sync} to exceed the GaN device's safe operating limit (6 V) and introduces oscillations due to parasitic interactions between the sensing capacitor and device capacitances. This shows the importance of carefully biasing the SyncFET; while higher V_{CC} increases sensor gain, it also risks instability and device overstress. Therefore, V_{CC} must be maintained <5 V for safe, stable operation.

The proposed sensor responds to both turn-on and turn-off transients, confirming its bidirectional dv/dt sensing capability. However, since the AGD is currently optimised only for turn-on control, turn-off dv/dt suppression remains a direction for future work.

In Figure 5, significant feedback current amplification is observed from the 0.1 pF capacitor when using the SyncFET during turn-on. This gain scales with V_{GS_sync} , and while higher gain improves sensing, it also narrows the safe operating range of V_{CC} . This trade-off reflects the balance between sensitivity and reliability that is common to capacitive dv/dt sensors. Despite the amplification, the sensor current remains smaller than the primary gate drive current, confirming the need for additional amplification through an AGD stage, consistent with earlier findings by Sun et al. (2016) and Bau et al. (2020).

As shown in Figure 6, increasing V_{CC} also enhances the AGD output currents i_{R3} and i_{R5} , improving current mirroring accuracy and extending the effective control range. Figure 7 illustrates improved gate current shaping when the SyncFET is integrated with the AGD. The combination introduces an active 'soft charging' mechanism at the gate during turn-on, effectively emulating a larger Miller capacitance. This dynamic shaping slows the charging of C_{GD} , directly reducing dv/dt at the switching node. Figure 8 confirms this effect, showing a measurable reduction in turn-on dv/dt compared with the baseline case without feedback amplification.

Compared with Sun et al. (2016), where large capacitors and high bus voltages were required to obtain sufficient gain, this paper demonstrates effective dv/dt regulation using a 0.1 pF sensing capacitor at only 24 V, reducing parasitics and circuit complexity.

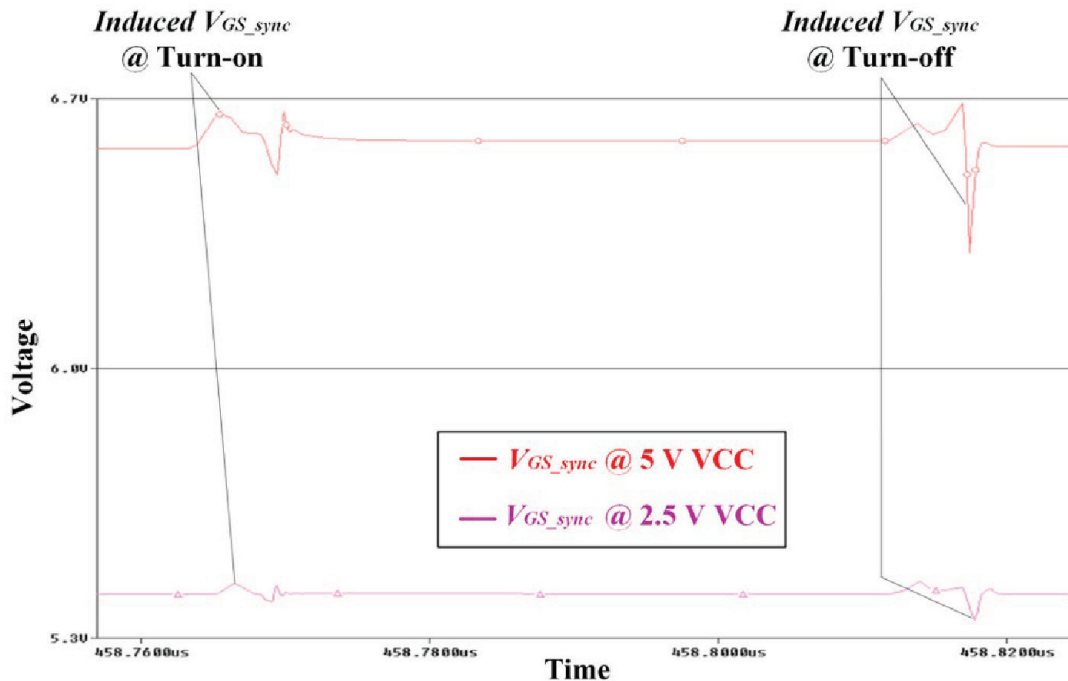


Figure 4. Simulated V_{GS_sync} waveforms of the SyncFET circuit at different V_{CC} voltages. SyncFET, synchronous GaN field-effect transistor.

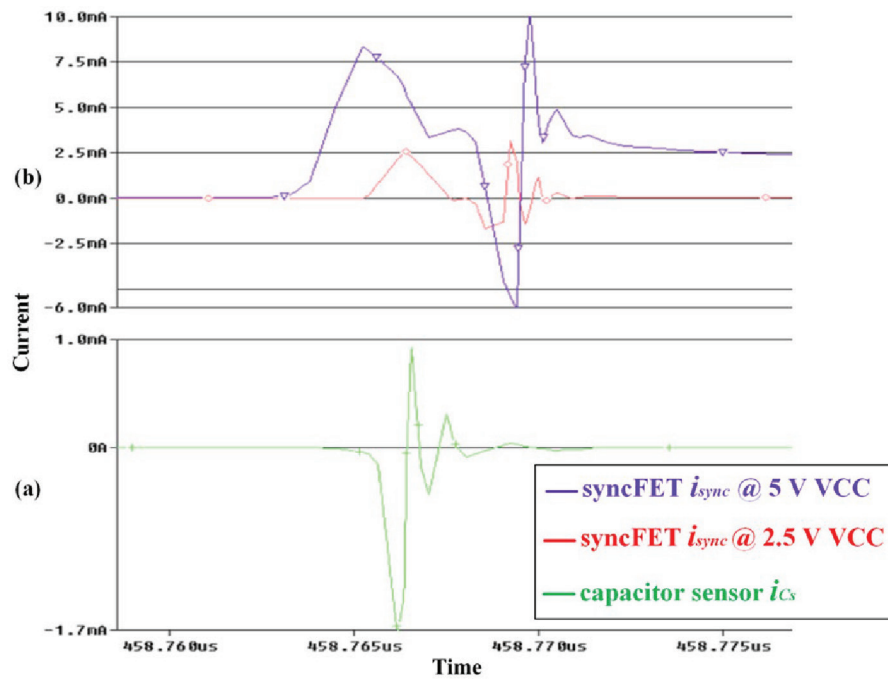


Figure 5. Simulated feedback current waveforms: (a) output from the 0.1 pF capacitor-only dv/dt sensor and (b) output from the 0.1 pF capacitor sensor enhanced by the proposed SyncFET circuit. SyncFET, synchronous GaN field-effect transistor.

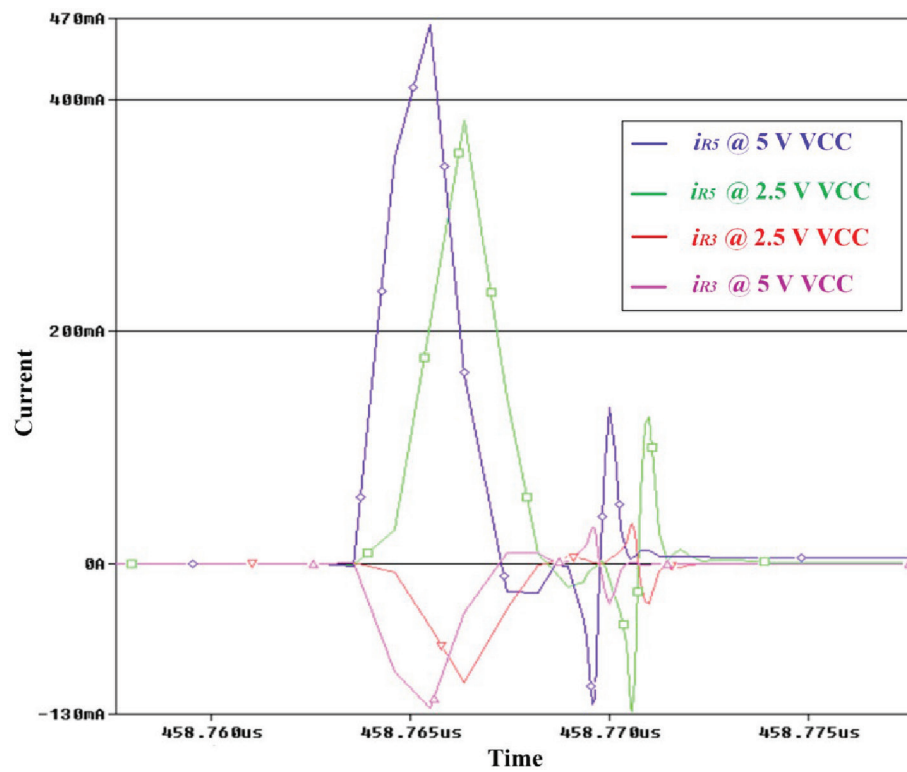


Figure 6. Simulated waveforms of the resultant currents generated by the proposed AGD at different V_{CC} voltages. AGD, active gate driver.

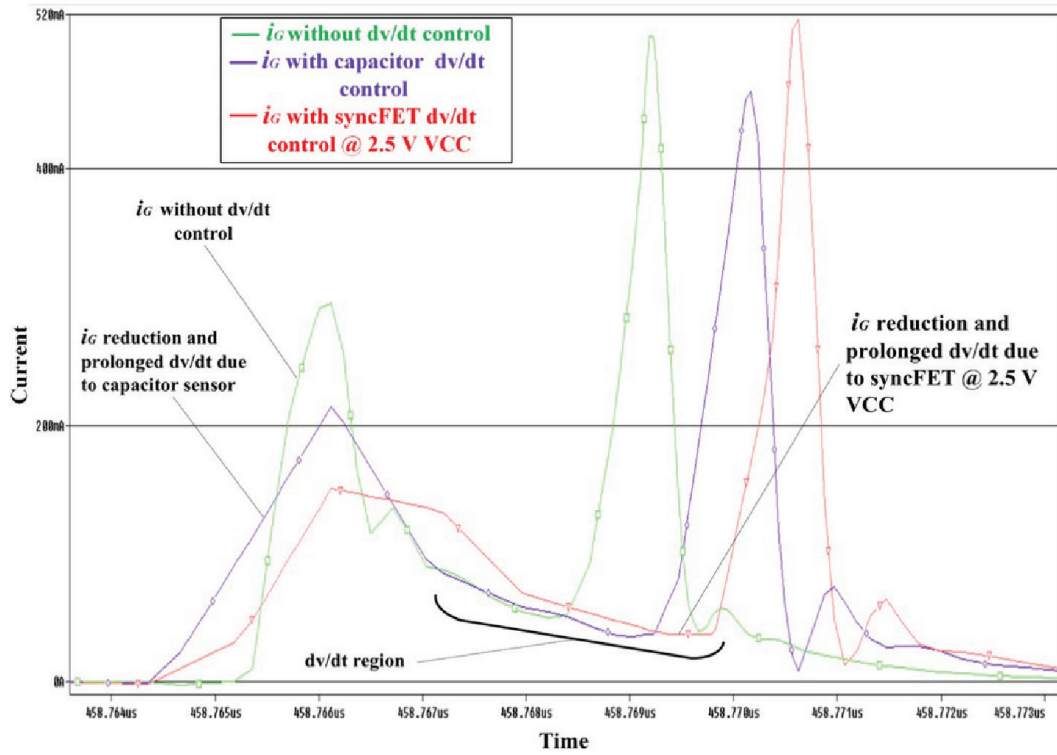


Figure 7. Comparison between simulated waveforms of the gate currents at different operating conditions.

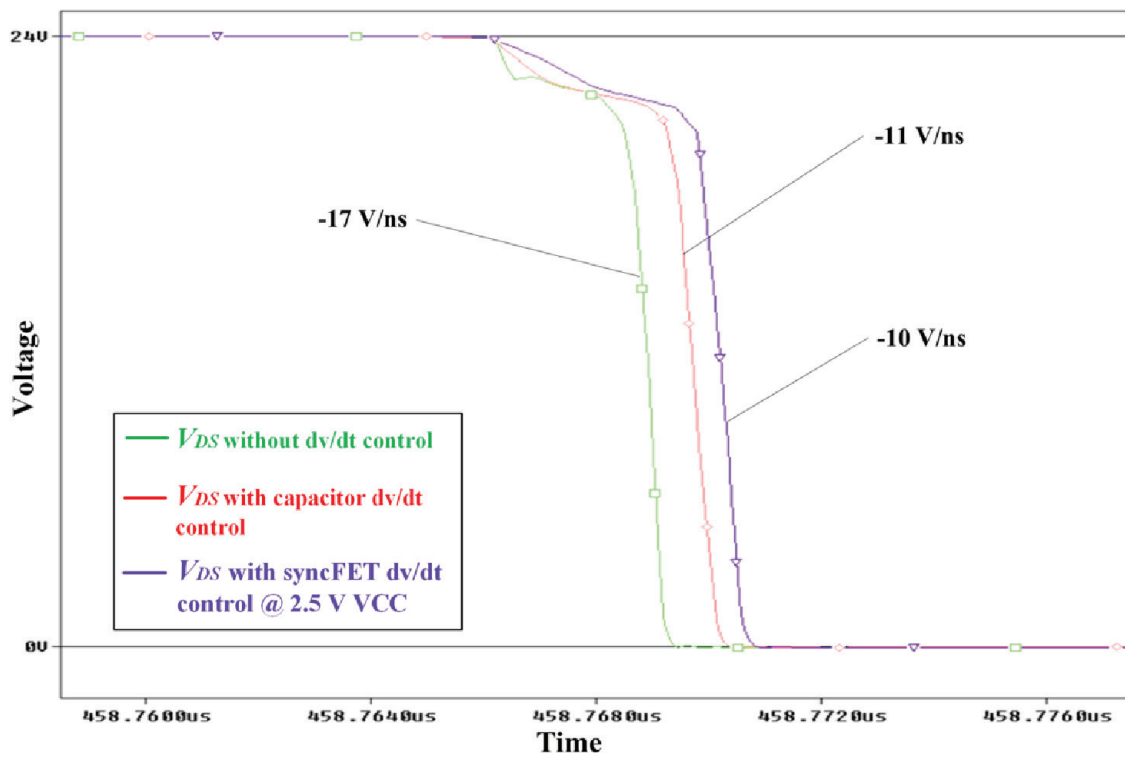


Figure 8. Simulated V_{DS} waveforms of the low-side GaN half-bridge under different operating conditions. GaN, gallium nitride.

Overall, these results demonstrate that the proposed SyncFET–AGD not only validates the necessity of SyncFET-assisted sensing but also achieves MHz-class dv/dt control with a compact, scalable design suitable for GaN converters in the 10 MHz range.

Turn-on switching loss ($P_{\text{ON_loss}}$) in simulation was estimated using the analytical expression (Lidow et al., 2019), as shown in Eq. (8):

$$P_{\text{ON_loss}} = P_{Vt} + P_{Cr} = \frac{1}{2} \cdot V_{\text{BUS}} \cdot i_L \cdot (t_{VF} + t_{CR}) \cdot f_{\text{SW}} \quad (8)$$

where V_{BUS} is the bus voltage, i_L is the load current, t_{VF} is the drain–source voltage fall time, t_{CR} is the drain current rise time, and f_{SW} is the switching frequency. This relation captures the energy dissipated during the overlap of voltage and current in the switching transition, making it a standard approach for estimating GaN switching losses. Experimental measurements were not used for direct loss calculation due to bandwidth limitations of current probes; instead, measured waveforms were employed to validate the simulated switching trends. Table 2 shows a 16.7% reduction in $P_{\text{ON_loss}}$ compared with the traditional gate resistance (R_G)-based method, while achieving better dv/dt regulation.

3.2. Experimental validation

The performance of the proposed SyncFET dv/dt sensor and AGD was validated in a 24 V, 10 MHz buck converter circuit. The experimental validation was carried out on a PCB incorporating the buck converter test circuit. As shown in Figure 9, the PCB layout illustrates the integration of the proposed SyncFET-based dv/dt sensor and the AGD. Figure 10 shows the V_{GS} waveform of the low-side GaN half-bridge device operating at 4.5 V and 10 MHz. Oscillations were effectively suppressed to <6 V by employing a 7 Ω gate resistance, demonstrating the effectiveness of the design in minimising unwanted transients. As shown in Figure 11, a V_{DS} voltage overshoot of approximately 43 V is observed during the turn-off transient, despite a nominal input of 24 V. This occurs due to parasitic inductance in the layout and the abrupt interruption of current during turn-off. The effect is more pronounced during turn-off than turn-on, as the rapid decrease in current causes voltage ringing across parasitic elements in the power loop.

Figures 12 and 13 present experimental V_{DS} waveforms of the low-side GaN transistor under conditions with and without the proposed SyncFET-based dv/dt sensor and AGD. The results confirm that incorporating the control circuitry substantially moderates the switching transition. As shown in Figure 14, the proposed scheme lowers the dv/dt from 15 V/ns to 10 V/ns, demonstrating effective suppression of excessive switching speed. This improvement, achieved with sub-nanosecond responsiveness at a 10 MHz operating frequency, highlights the capability of the system to enhance switching stability, reliability and may potentially mitigate EMI-related issues in high-frequency GaN converters.

It is noted that the oscilloscope used (350 MHz bandwidth, 1.25 GS/s sampling rate) corresponds to a rise/fall-time resolution limit of approximately 1 ns. The measured fall-times of the GaN device range from 1.20 ns to 1.84 ns, which approach this resolution limit. This implies a relative timing uncertainty of about 55%–83% for the fastest transitions. As highlighted in efficient power conversion (EPC) application notes (Biswas et al., 2017), such bandwidth limitations affect the accuracy of absolute fall-time values but do not compromise the validity of relative comparisons, provided the same measurement setup is consistently used. Therefore, while the exact fall-time numbers may carry some error, the observed dv/dt reduction from 15 V/ns to 10 V/ns remains a reliable indicator of the proposed circuit's effectiveness in moderating switching speed.

Table 2. Comparison of $P_{\text{ON_loss}}$ for different dv/dt regulation techniques

Technique	R_G (Ω)	$P_{\text{ON_loss}}$ (mW)	dv/dt (V/ns)
Without dv/dt	7	35.96	17
Increasing R_G	13	61.79	11.12
Capacitor-only dv/dt control	7	54.03	11
SyncFET dv/dt control	7	55.78	10

SyncFET, synchronous GaN field-effect transistor.

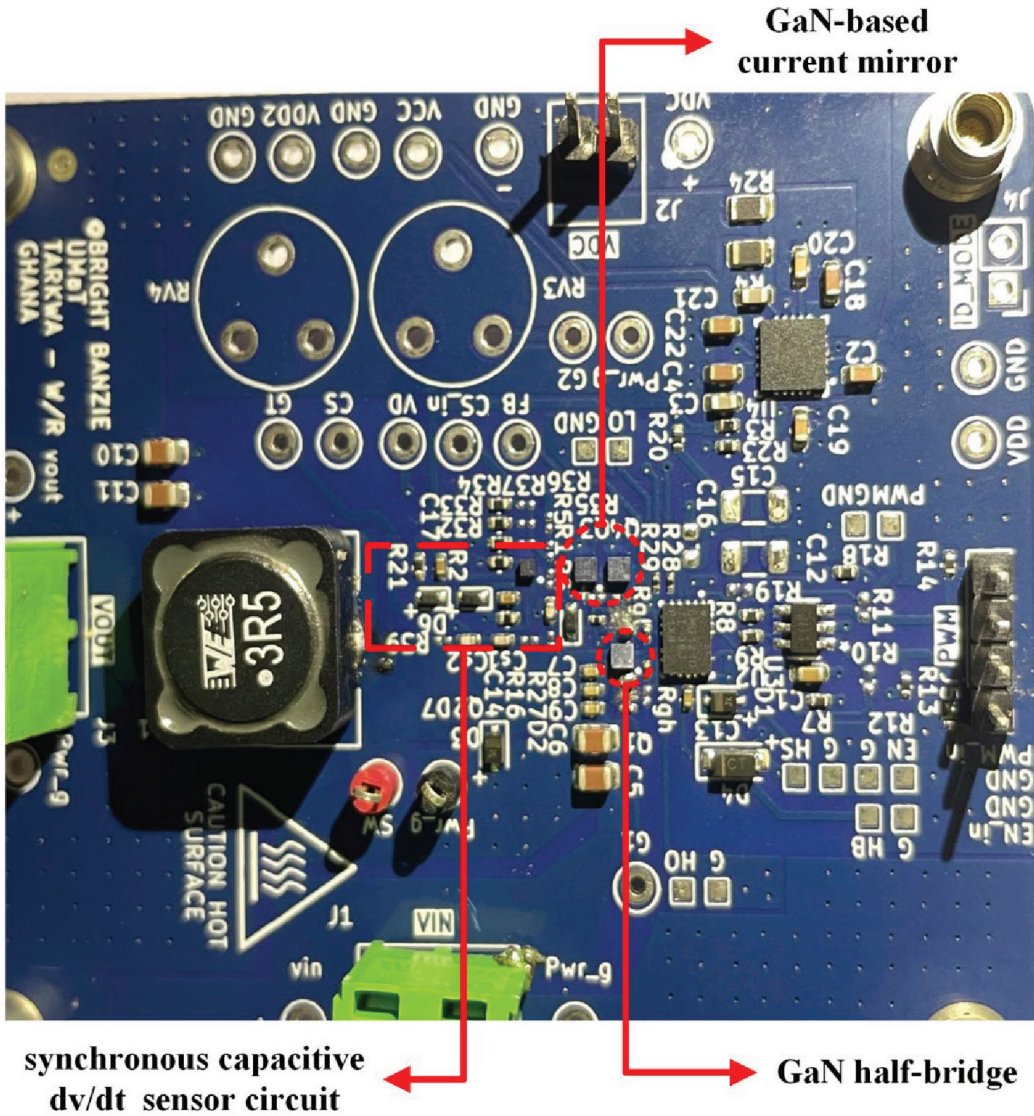


Figure 9. DC–DC buck converter test PCB (photograph). GaN, gallium nitride.

4. Discussion

Simulation results verify the capability of the proposed SyncFET to amplify the weak feedback current generated by a 0.1 pF dv/dt sensing capacitor. When combined with the AGD stage, this amplification achieves substantial dv/dt suppression. PSpice simulations in a 24 V, 10 MHz GaN DC–DC buck converter demonstrate a reduction in dv/dt from 17 V/ns to 10 V/ns, with experimental measurements confirming a comparable improvement from 15 V/ns to 10 V/ns under identical conditions. Minor deviations are due to environmental and device-level differences. This dv/dt reduction enhances system reliability and may improve EMI behaviour in high-frequency, noise-sensitive applications.

As summarised in Table 3, previous studies often relied on high bus voltages (>50 V), large sensor capacitors (>2 pF) or integrated circuits with tuned width (W)/length (L) ratios. By contrast, the proposed discrete solution achieves comparable or better performance with a 0.1 pF capacitor and 24 V input. The SyncFET acts as a preamplifier, enabling strong feedback from weak dv/dt signals without complex IC design or bulky components, supporting scalability to other topologies like boost converters and inverters.

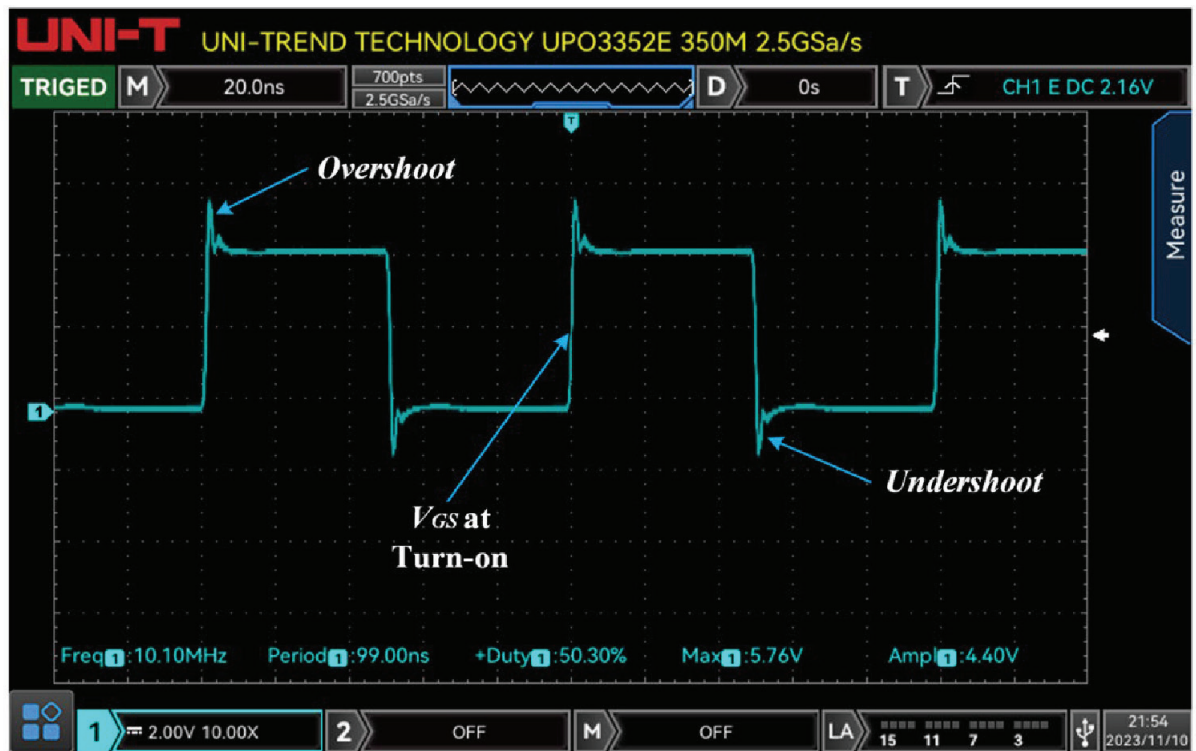


Figure 10. Measured V_{GS} waveform of the low-side GaN half-bridge at 4.5 V and 10 MHz. GaN, gallium nitride.

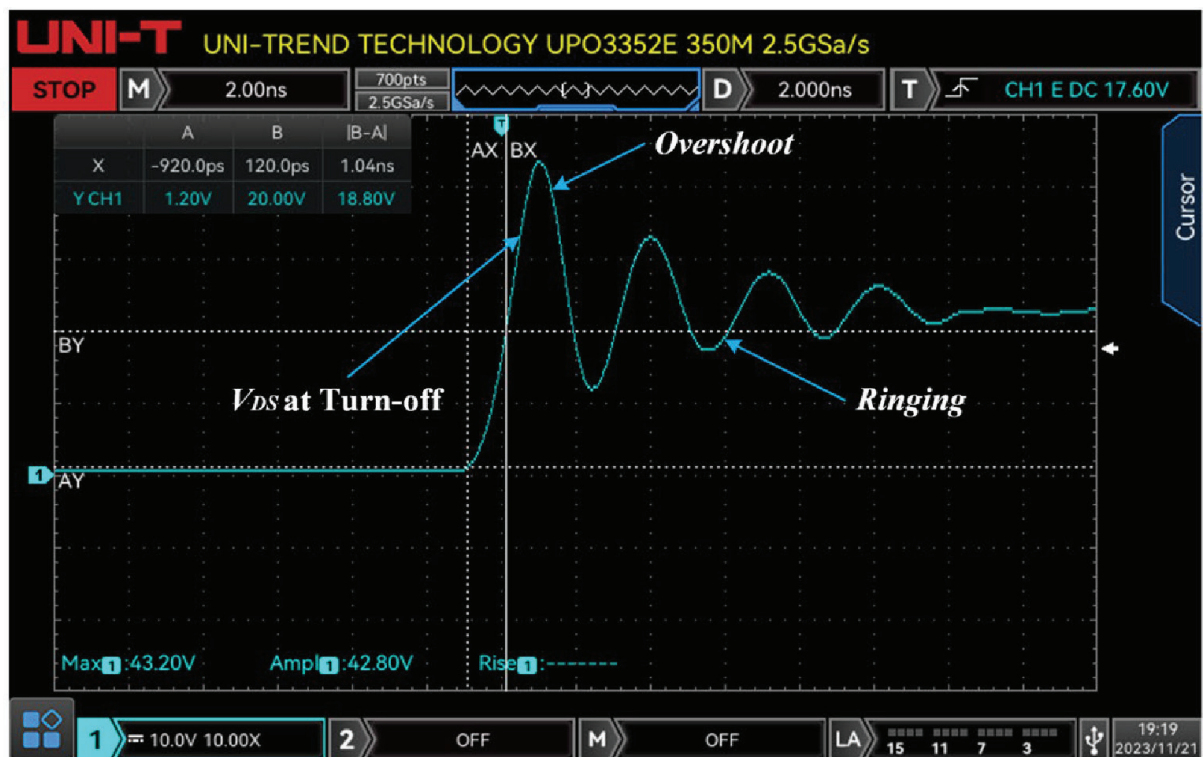


Figure 11. Measured V_{DS} waveform of the low-side GaN half-bridge during turn-off at 10 MHz. GaN, gallium nitride.

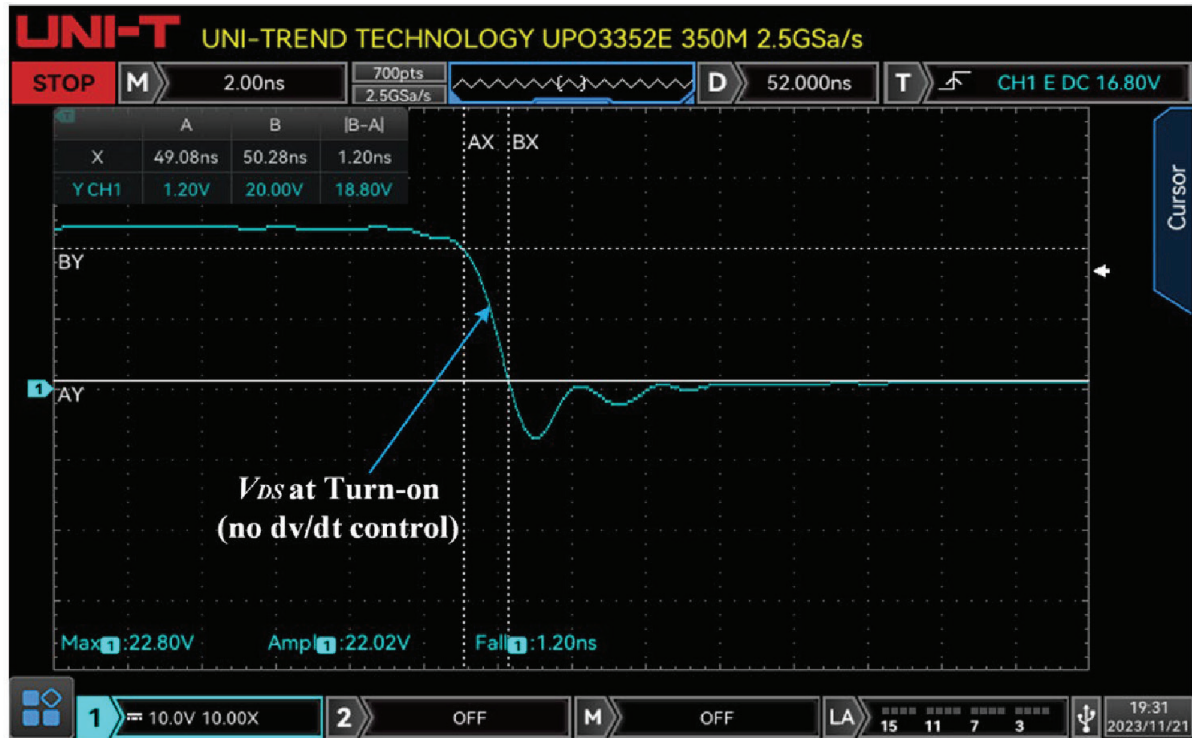


Figure 12. Measured V_{DS} waveform of the low-side GaN half-bridge during turn-on without dv/dt control. GaN, gallium nitride.

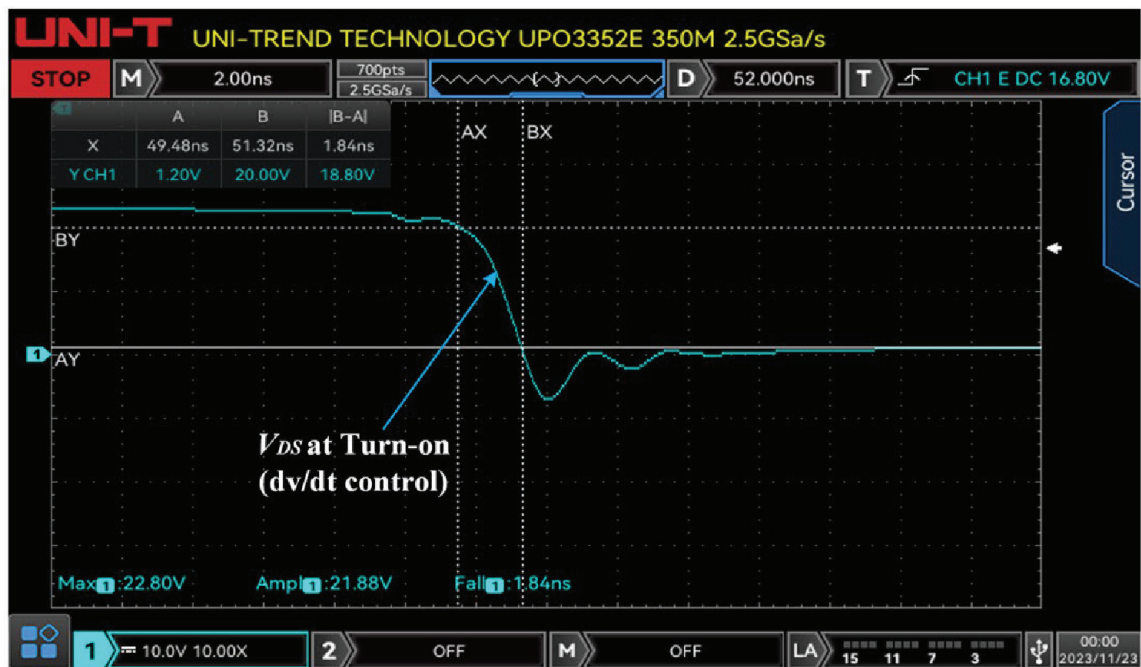


Figure 13. Measured V_{DS} waveform of the low-side GaN half-bridge during turn-on with the proposed dv/dt control. GaN, gallium nitride.

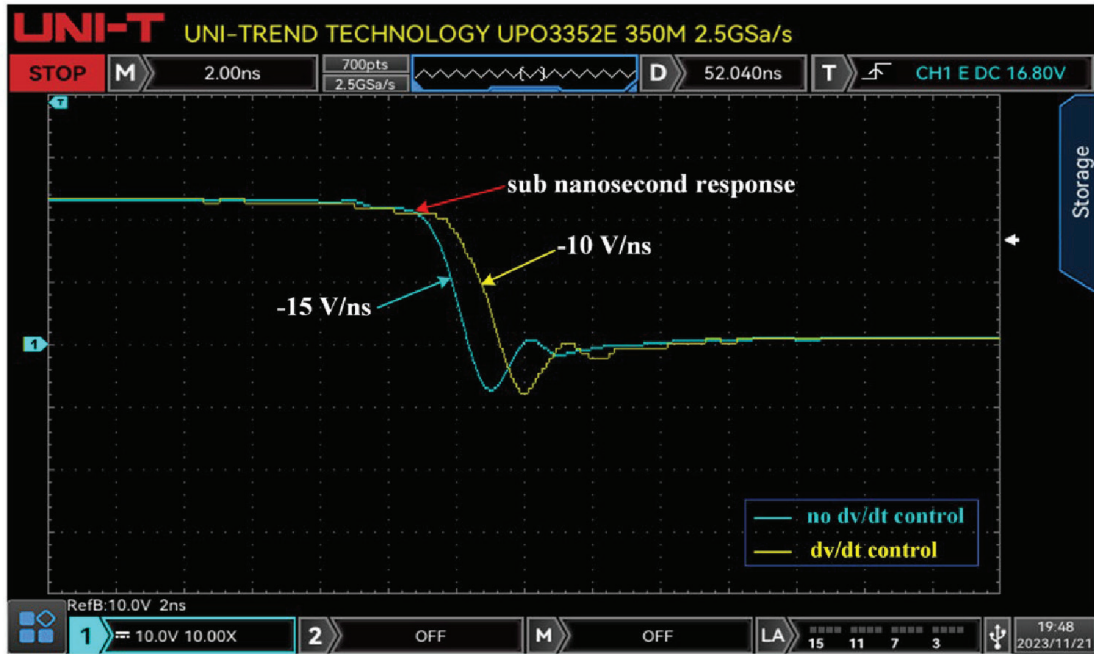


Figure 14. Comparison of measured V_{DS} waveforms of the low-side GaN device during turn-on with and without the proposed dv/dt control. GaN, gallium nitride.

Table 3. Comparative performance analysis of the proposed work and previous studies

Circuit parameters	Related literature					Proposed work
	Sun et al. (2016)	Bau et al. (2020)	Liu et al. (2023)	Yu et al. (2023)	Yang et al. (2024)	
Power switch	GaN	GaN	GaN	GaN	GaN	GaN
Bus voltage	300 V	50 V	300 V	400 V	200 V	24 V
Operating frequency	Not reported	1 MHz	1 MHz	1 MHz	1 MHz	10 MHz
Sensor capacitance	47 pF (discrete)	2 pF (discrete)	Not reported (parasitic C_{DS})	Not reported (parasitic C_{DS})	Not reported (integrated)	0.1 pF (discrete)
Gain amplification method	Gate current control	Width/length ratio adjustment	Width/length ratio adjustment	Width/length ratio adjustment	Comparator	SyncFET
Flexibility of gain amplification method	High (discrete voltage follower)	Low (integrated CMOS)	Low (integrated LDMOS)	Low (integrated high-voltage LDMOS)	Low (silicon-on-insulator)	High (discrete N-channel GaN SyncFET)
AGD implementation	Discrete	Integrated	Integrated	Integrated	Integrated	Discrete
Switching loss reduction	1.86%	15.85% @ 20 pF C_s	Not reported	16.2%	33.99%	16.7%
Response time	>2 μ s	<1 ns	Not reported	<3 ns	Not reported	<1 ns
dv/dt regulation	8.8 V/ns	6.3 V/ns	14.3 V/ns	63.7 V/ns	22 V/ns	10 V/ns

AGD, active gate driver; GaN, gallium nitride; SyncFET, synchronous GaN field-effect transistor.

Unlike earlier passive dv/dt control approaches, such as gate resistance tuning or GS capacitors (Zhao et al., 2021), which sacrifice switching speed, increase switching losses and degrade MHz-scale performance, the proposed SyncFET–AGD architecture achieves dv/dt control with high bandwidth and without introducing additional gate delays. Although the auxiliary circuit introduces a 4.87% switching loss overhead compared with capacitor-only control, it achieves a 16.7% reduction relative to gate resistance tuning (Table 2), making it a practical and efficient closed-loop solution.

This paper focuses on turn-on dv/dt due to its dominant effect on switching loss and gate drive behaviour. While turn-off dv/dt also affects switching loss and device reliability, its impact on switching loss is minor at MHz frequencies due to the fast crossover and high GaN transconductance. Future work could explore a dual-loop AGD to regulate both transitions more effectively.

5. Conclusion

This paper demonstrates the effectiveness of a discrete SyncFET-enhanced capacitive dv/dt sensor combined with current mirror AGD in achieving closed-loop dv/dt regulation during turn-on transients of a 24 V, 10 MHz DC–DC buck converter. The proposed SyncFET-based dv/dt sensor effectively amplifies the weak feedback signal generated by a 0.1 pF sensing capacitor and, despite its low-voltage operation, delivers high gain with nanosecond-scale response, thereby ensuring the bandwidth required for accurate dv/dt sensing in MHz-frequency converters. This demonstrates that a GaN-based discrete SyncFET can effectively enable reliable and efficient, high-speed dv/dt control in compact MHz-frequency converters. The proposed solution bridges the gap between passive techniques and integrated solutions, offering a practical, high-performance alternative using discrete GaN components.

Future research could focus on enhancing the SyncFET sensor's gain, optimising the design for higher power systems that require deeper dv/dt suppression, and developing new AGD architectures for simultaneous turn-on and turn-off dv/dt optimisation.

Acknowledgements

The authors gratefully acknowledge the support provided by the University of Mines and Technology (UMaT), Tarkwa, which made this research possible.

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