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Model Predictive Control of a New Low Cost 31-Level Inverter

Research paper

Mohamad N. Abdul Kadir[1,*], Harith Al-Badrani[2], Yasir M. Y. Ameen[1]

[1]Depatment of Electrical Engineering, University of Mosul, Mosul, Iraq
[2]Electronic Department, Ninevah University, Mosul, Iraq

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Abstract: This research presents the development of a compact and cost-effective asymmetric multilevel inverter (MLI) that preserves the advantages of high-resolution multilevel systems while significantly reducing the component count. The proposed single-phase 31-level inverter configuration utilises only 2 isolated DC sources, 2 flying capacitors (FCs) and 10 MOSFET switches, achieving a notable reduction in both complexity and cost. A dedicated Finite Control Set-Model Predictive Control (FCS-MPC) strategy has been designed to regulate the FC voltages, ensure accurate reference current tracking and minimise switching losses. The weighting coefficients of the three components in the FCS-MPC cost function have been optimised to enhance the inverter's overall performance. Using a one-step prediction horizon, simulation results demonstrate that the inverter achieves precise current tracking, with both RMS error and total harmonic distortion (THD) maintained <1%. The average switching frequency is approximately seven times the reference current frequency, indicating a considerable reduction in switching losses. The impact of extending the prediction horizon to two steps is also analysed with respect to switching losses and current tracking accuracy. Finally, a comparative evaluation with six recent high-resolution inverter designs confirms that the proposed system offers superior performance, achieving the lowest switch-to-level ratio, minimum total switch voltage ratings and capacitor voltage ratings, and the fewest series-connected switches per level in the current path.

Keywords: *asymmetrical multilevel inverter • model predictive control • capacitors voltage-balancing • flying capacitors*

1. Introduction

The development of DC–AC power inverters has progressed through multiple stages. There are three main factors that contribute to the enhancement of inverter performance: first, the growing demand for advanced high-performance applications; second, the development of semiconductor devices capable of handling larger amounts of power while minimising switching time and power losses; and third, the availability of high-performance low-cost digital controllers which enables the implementation of computationally demanding control algorithms.

The ability of a multilevel inverter (MLI) to closely resemble the desired sinusoidal output voltage has stimulated the tendency to construct MLI with a large number of levels. However, increasing the number of levels beyond a certain point becomes impractical in the basic MLI topologies due to the excessively large number of elements, which in turn increases complexity and cost while reducing reliability (Adly et al., 2023).

Several innovative topologies have been proposed building on the three basic topologies: Neutral-Point-Clamped (NPC) (Guennegues et al., 2009), Flying Capacitor (FC) (McGrath and Holmes, 2009) and Cascaded H-bridge (CHB) (Rodriguez et al., 2007). One of the earliest improvements, the asymmetrical CHB, is capable of achieving up to 3^n levels for n cascaded cells rather than the 1 + 2n levels from the basic design. The maximum number of levels is obtained when the cascaded cells are supplied by DC sources with a ratio of 3 (Abdul Kadir and Hussien, 2004). However, this approach requires multiple active supplies with bidirectional current capability. To reduce the number of costly and bulky DC supplies, FCs are employed to provide additional DC links. However,

* Email: makadr@uomosul.edu.iq

the capacitor voltage must be maintained close to its average value. To achieve this, most modulation approaches exploit the availability of redundant states that have opposite effects on the capacitor voltage (Chen et al., 2020; Ramu et al., 2025).

New types of MLIs have been created, including the 31-level inverter, which has better output voltage quality and lower total harmonic distortion (THD) (Rodriguez et al., 2007). Adding more voltage levels improves the waveforms and enhances the whole system's efficiency. This is why high-level MLIs are attractive for high-power and precise applications.

Several designs that deviate from the three basic topologies have been proposed with the aim of achieving the maximum number of voltage levels for a given number of elements and consequently, lower circuit complexity. The concept of nested uneven bridges has been employed to maximise the number of levels per switching device (Nanda et al., 2022). Although the number of levels increases exponentially with the number of nested bridges, this design lacks modularity.

Advanced control strategies are necessary to fully exploit the benefits of MLIs. Model predictive control (MPC) has emerged as a promising method that reduces harmonic distortion, improves DC-link voltage balance and provides fast dynamic response (Riar et al., 2015). MPC improves control performance by predicting the system future behaviour and changing the control signals accordingly. This is especially helpful for complicated MLI systems (Harbi et al., 2023).

Fixed-frequency MPC has been applied to reduce voltage ripples in FCs. For example, in a 5-level FC converter, this approach improves performance by ensuring accurate regulation of both FC and output voltages (Yang et al., 2024). However, this study does not address innovative inverter designs or other control targets, such as reducing switching losses and common mode voltage.

Finite Control Set-Model Predictive Control (FCS-MPC) has also been applied to optimise DC capacitor voltages in grid-connected and stand-alone inverters. For example, a nine-level Packed U-Cell inverter uses MPC to balance capacitor voltages while minimising THD and reducing capacitor voltage ripple. This control method allows the use of smaller DC capacitors in a nine-level Packed U-Cell inverter, making it suitable for various industrial applications, particularly for single-phase grid-connected devices (Noghani et al., 2019).

Karamanakos et al. (2018) demonstrated that the choice of error norm in the cost function significantly influences the performance of closed-loop systems in MPC with reference tracking. This study emphasises that the $\ell 1$-norm, which has been used in some works to simplify the cost function, leads to degraded performance and potential closed-loop instability. By contrast, the $\ell 2$-norm overcomes these limitations, providing improved stability. A case study based on a three-level inverter drive system highlighted the advantages of adopting the $\ell 2$-norm.

Hardware-in-the-loop (HIL) studies have been conducted to validate the real-time performance of MPC strategies in grid-connected converters. For instance, a simple predictive direct power control method has been tested through HIL studies to show its efficiency in reducing power ripple and Total Harmonic Distortion (THD) (Quang et al., 2024). The method was applied to a five-level Active Neutral Point Clamped (ANPC) inverter; however, its extension to innovative topologies is not straightforward.

Due to the complexities and ambiguities associated with tuning the individual cost function weighting parameters in FCS-MPC, some studies have considered sequential model predictive control (S-MPC) as an alternative. In this approach, a sequence of single-objective cost functions, ordered by their relative importance, is evaluated. The primary cost function generates a shortlist of N viable switching states, which are then further assessed by the secondary cost function. Ultimately, a switching vector that satisfies the constraints of both cost functions is selected and applied to the inverter. Bonaldo et al. (2025) conducted a comprehensive evaluation comparing S-MPC and FCS-MPC for a grid-connected NPC inverter and recommended S-MPC as a more robust alternative.

Another strategy involves a two-step optimisation process to balance FCs and neutral point (NP) voltages. In this approach, the first step focuses on FC voltage balancing, while the second step addresses NP voltage control. This method not only mitigates voltage fluctuations across the entire frequency range but also reduces the computational burden by dividing the optimisation process into manageable steps (Noori et al., 2023). However, this study did not discuss implementation challenges, and the considered nested NPC inverter does not optimise the inverter size.

In the present study, a single-phase 31-level inverter topology with a reduced component count is proposed, based on the concept presented by Omer et al. (2020). The present study aims to develop an effective voltage control strategy for this circuit. While the original inverter requires four isolated DC supplies, the proposed design uses merely two supplies. The other two supplies are replaced by two capacitors. A FCS-MPC strategy has been developed with three targets: first, to track the target output current with minimum error; second, to maintain the

capacitor voltages near their nominal values; and third, to minimise the switching losses, considering that the switching devices are subjected to different voltage levels.

The paper is organised as follows: Section 2 introduces the proposed inverter circuit and defines its switching variables and switching states. Section 3 outlines the FCS-MPC control strategies and the associated computational methods. Section 4 presents the inverter model and simulation results. Section 5 discusses and compares the results with other studies. Section 6 presents the conclusions.

2. Proposed MLI Topology and Switching States

The proposed inverter design, which features a reduced component count, is shown in Figure 1. The existing equivalent 31-level inverter has four isolated DC voltage supplies related by the ratio 1:2:5:10 (Omer et al., 2020). The first contribution of this work is the replacement of two of the four isolated DC supplies with capacitors. The capacitor voltages are E and $2E$, where E is the voltage step and the maximum inverter output voltage is $15E$. The 10 switching devices forming the inverter circuit, depicted in Figure 1 as MOSFETs, are grouped into five complementary pairs, that is, the state of switch S_i is the opposite of switch S_i', where $i \in \{1, 2, 3, 4, 5\}$. The switching variable x_i determines the state of switch S_i, with 0 and 1 representing the OFF and ON states, respectively. The five-digit binary number ($x_5\ x_4\ x_3\ x_2\ x_1$) represents the inverter switching state.

From Figure 1, the output voltage is expressed as follows:

$$v_o = v_{AA'} + v_{A'B'} + v_{B'B} \tag{1}$$

The relationships between the switching state and the output voltage, as well as between the inverter switching state and the capacitor voltage variation, can be deduced by examining Figure 2. In Figure 2(a), the production of the voltage $V_{AA'}$ is explained. This voltage is determined by the switching variables x_3 and x_1. The relationship can be summarised as follows:

$$v_{AA'} = (4x_3 + x_1)E \tag{2}$$

In Figure 2(b), the production of the voltage $V_{BB'}$ is shown. This voltage is determined by the switching variables x_4 and x_2. The relationship can be summarised as follows:

$$v_{B'B} = (8x_4 + 2x_2)E \tag{3}$$

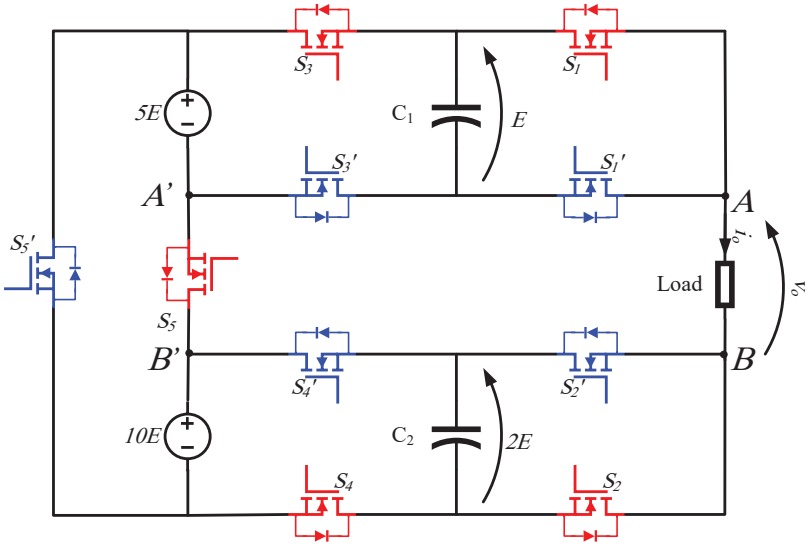


Figure 1. The proposed single-phase 31-level inverter circuit.

Figure 2(c) shows that the switching variable x_5 determines $V_{A'B'}$ as follows:

$$v_{A'B'} = 15E(x_5 - 1) \tag{4}$$

Substituting Eqs. (2)–(4) into Eq. (1), yields the output voltage as follows:

$$\frac{v_o}{E} = \left(\sum_{i=1}^{5} 2^{i-1} x_i\right) - 16 + \overline{x_5} \tag{5}$$

Figure 2 also shows the variation of the two capacitors voltages. These voltages depend on the load current (i_o) and the inverter switching state. The variation of the voltages of C_1 and C_2 over one switching interval (T_s) can be obtained by examining Figures 2(a) and 2(b), respectively:

$$\delta v_{C_1} = (x_3 - x_1)\frac{i_o T_s}{C_1} \tag{6}$$

$$\delta v_{C_2} = (x_4 - x_2)\frac{i_o T_s}{C_2} \tag{7}$$

where δv_{C_1} and δv_{C_2} are the voltage variations over one switching interval, C_1 and C_2 represent the capacitance of the two capacitors and i_o is the load current.

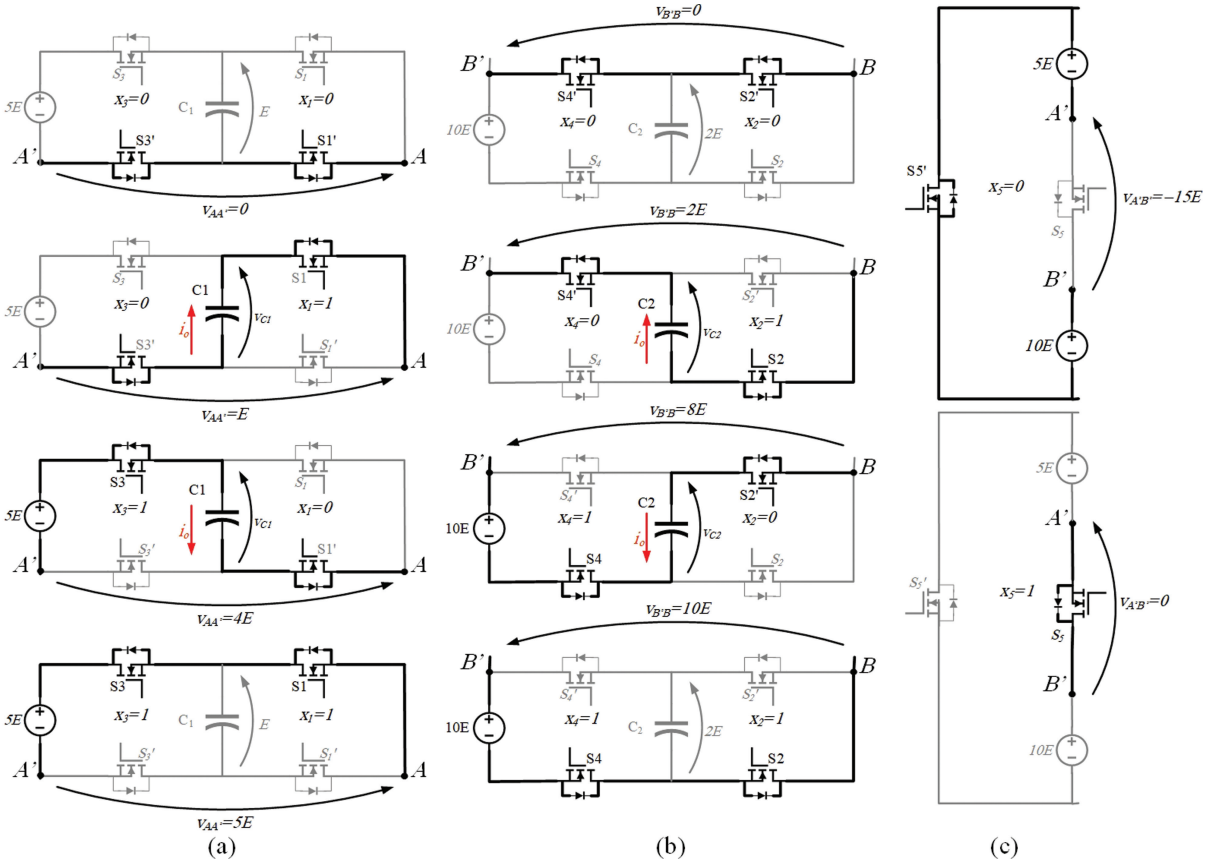


Figure 2. The operation modes of the inverter system illustrate how the switching variables control the voltages: (a) The effect of (x_3, x_1) combinations on $V_{AA'}$; (b) The effect of (x_4, x_2) combinations on $V_{B'B}$; (c) The effect of x_5 on $V_{A'B'}$.

3. Controlling the Inverter by FCS-MPC Algorithm

This section presents the development of the control algorithm to track a reference current, stabilise the FCs voltages and minimise switching losses. The MPC approach has been selected due to its suitability for multi-target control. FCS-MPC has been shown to be one of the effective tools in converter control, particularly optimising inverter performance with multiple performance objectives (Muhaisen and Abdul Kadir, 2021). MPC is a model-based control strategy that uses a discrete-time model of the system to predict future behaviour. The core idea is to select the optimal switching state that minimises a predefined cost function. For inverters, the cost function usually includes factors related to current tracking error, common mode voltage suppression and capacitor voltage balancing (Garcia et al., 2024; Le et al., 2024; Nitheesh et al., 2022).

The cornerstones of an FCS-MPC algorithm are as follows:

1. **Discrete-time model:** The system's future behaviour is predicted using a discrete-time model. In MLIs, the model predicts the current for all possible voltage vectors. The conventional MPC predicts the behaviour for one step ahead, while multiple step prediction horizons enhance the performance at the cost of exponential growth of computational burden.
2. **Cost function:** The cost function is designed to prioritise control objectives. For instance, minimising the current error and common mode voltage (CMV) are common objectives in three-phase inverters.
3. **Voltage vector selection:** The algorithm evaluates all possible voltage vectors and selects the one that minimises the cost function. However, the large number of voltage vectors in MLIs makes this process computationally intensive.

The following three subsections describe the three components of the discrete time model, and the fourth subsection describes the control system and the voltage vector selection.

3.1. Reference current tracking

Considering an RL-load, the next desired output current has been forecasted based on the past values of the reference current and using a cubic spline extrapolation function. In the literature, the most common method to predict the reference output current is the Euler-based linear extrapolation (Sanca et al., 2023). More accurate estimation has been achieved with the higher order Runge-Kutta-based extrapolation, as presented by Adjei-Saforo et al. (2022). In this work, it has been noticed that the cubic spline method leads to more accurate prediction. Figure 3 shows a comparison of the reference current waveform with the prediction by Euler-based linear extrapolation and cubic spline interpolation. At 50 Hz reference frequency and 0.25 ms sampling time, the RMS error obtained using cubic spline interpolation is <5% of the error resultant using linear extrapolation.

The predicted reference current is determined as a function of the current value and the three most recent reference currents:

$$i_{o,ref}^{k+1\prime} = f(i_{o,ref}^{k}, i_{o,ref}^{k-1}, i_{o,ref}^{k-2}, i_{o,ref}^{k-3}) \tag{8}$$

where $i_{o,ref}^{k+1\prime}$ is the predicted next reference current. The past four current values are used to determine the parameters of the third-order extrapolation polynomial that predicts the next current.

To reduce computational complexity, it has been decided to identify the voltage magnitude required to realise the reference current instead of comparing it with the current produced by each inverter's next switching state. This approach reduces computational effort, since comparing voltage levels for all inverter states is more efficient than calculating the resulting current for every possible switching state.

The $(k + 1)^{th}$ reference voltage is determined using the measured k^{th} and estimated $(k + 1)^{th}$ reference current values, as follows:

$$v_{o,ref}{}^{k+1} = L\frac{[i_{o,ref}{}^{k+1} - i_{o}{}^{k}]}{Ts} + i_{o,ref}{}^{k+1}R \tag{9}$$

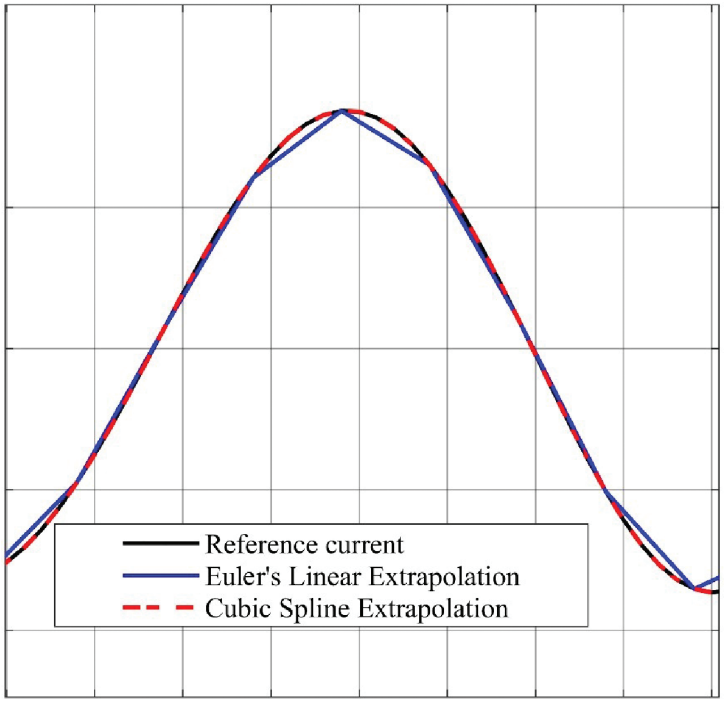


Figure 3. Comparison of the reference current with currents predicted by linear and cubic spline extrapolation.

where L and R are the load inductance and resistance, respectively, and i_o^k is the measured output current at the kth step. For extended prediction horizons beyond one step, the $(k + 2)^{th}$ reference voltage is determined by the following equation:

$$v_{o,ref}^{\ k+2} = L\frac{[i_{o,ref}^{\ k+2} - i_o^{\ k}]}{2Ts} + i_{o,ref}^{\ k+2}R \tag{10}$$

where $v_{o,ref}^{\ k+2}$ and $i_{o,ref}^{\ k+2}$ are the reference voltage and current at the second step ahead, respectively.

The cost function term corresponding to the required voltage to track a given reference current for the next switching state (i) and subsequent state (j) is given in Eq. (11):

$$C_v(i,j) = K_v\left((1-W_{ss})\left(\frac{v_{o,ref}^{\ k+1} - v_o^{\ i}}{E}\right)^2 + W_{ss}\left(\frac{v_{o,ref}^{\ k+2} - v_o^{\ j}}{E}\right)^2\right) \tag{11}$$

where C_v is the cost function term corresponding to the voltage error, K_v is a weighting factor for reference voltage with $0 < K_v < 1$ and W_{SS} is a factor that represents the significance of the step $(k + 2)$ compared with the following $(k + 1)$ step, where $0 \le W_{SS} < 0.5$; $W_{SS} = 0$ for a one-step prediction horizon. i and j are next and subsequent states indices, respectively, $0 \le i, j \le 31$.

It must be emphasised that Eqs (9) and (10) describe an RL load; other types of loads such as machines, non-linear loads and grid-connected inverters have different models, many of which have been reported in the literature.

3.2. Capacitor voltage balancing

According to the effect of the switching state on the capacitor voltages, given in Eqs (6) and (7), the cost function term representing the capacitor for a one-step prediction horizon is given in Eq. (12):

$$C_c(i) = K_c\left[\left(E - V_{C1}^{\ k} + \delta V_{C1}(i)\right)^2 + \left(2E - V_{C2}^{\ k} + \delta V_{C2}(i)\right)^2\right] \tag{12}$$

where C_c is the term of the cost function corresponding to the capacitor voltage, and K_c is the weighting factor for capacitors balancing, with $0 < K_c < (1 - K_v)$.

Eq. (12) can also be extended to two-step prediction horizon as follows:

$$C_c(i,j)=K_c\left[\begin{array}{c}(1-W_{ss})\times\left(\begin{array}{c}\left(E-V_{C1}{}^{k}+\delta V_{C1}(i)\right)^2+\\ \left(2E-V_{C2}{}^{k}+\delta V_{C2}(i)\right)^2\end{array}\right)\\ +W_{ss}\left(\begin{array}{c}\left(E-V_{C1}{}^{k}+\delta V_{C1}(j)\right)^2+\\ \left(2E-V_{C2}{}^{k}+\delta V_{C2}(j)\right)^2\end{array}\right)\end{array}\right] \tag{13}$$

3.3. Switching losses minimisation

As shown in Figure 2, switches S_1 and S_1' are subjected to an off-state voltage of E, while S_2 and S_2' experience $2E$. It can also be seen that S_3 and S_3', S_4 and S_4' and S_5 and S_5' are subjected to $4E$, $8E$ and $15E$, respectively. Since the off-state voltage of a switch influences the switching losses, the weighting factors in the switching-loss cost term are included to account for the different voltage levels of the switches.

The switching losses are determined based on the variation of the switching state and the voltage across each switch, as follows:

$$C_{sw}(i)=K_{sw}\left[\begin{array}{c}\left(x_1^k-x_1^i\right)^2+2\left(x_2^k-x_2^i\right)^2+4\left(x_3^k-x_3^i\right)^2+\\ 8\left(x_4^k-x_4^i\right)^2+15\left(x_5^k-x_5^i\right)^2\end{array}\right] \tag{14}$$

C_{sw} is the cost function term corresponding to the switching losses, and x_y^i is a binary digit that represents the state of switch y in state i. K_{sw} is the weighting factor corresponding to the switching losses given by the following equation:

$$K_{sw}=1-K_v-K_c \tag{15}$$

Each of the five terms in the brackets in Eq. (14) takes a value of 1 if the corresponding switching device changes its state during the transition from the present state (state k) to state i, and 0 if it maintains its current state. When these terms are multiplied by the integers 1, 2, 4, 8, and 15, the result represents the ratios of the off-state voltages across each pair of switches. Since the converter operates in hard-switching mode, the switching losses are directly proportional to the off-state voltages. Therefore, the switching cost term is represented accordingly.

Similar to Eqs (11) and (13), Eq. (16) gives the switching loss cost for two-step prediction horizon:

$$\begin{array}{l}C_{sw}(i)=K_{sw}\left[(1-W_{ss})\left[\left(x_1^k-x_1^i\right)^2+2\left(x_2^k-x_2^i\right)^2+4\left(x_3^k-x_3^i\right)^2+8\left(x_4^k-x_4^i\right)^2+15\left(x_5^k-x_5^i\right)^2\right]+W_{ss}\right]\\ \left[\left(x_1^k-x_1^j\right)^2+2\left(x_2^k-x_2^j\right)^2+4\left(x_3^k-x_3^j\right)^2+8\left(x_4^k-x_4^j\right)^2+15\left(x_5^k-x_5^j\right)^2\right]\end{array} \tag{16}$$

3.4. The FCS-MPC controller

The flowchart of the FCS-MPC one- and two-step prediction horizon function is shown in Figure 4. The function begins by calculating the predicted values of the next reference currents and then the amplitude of the reference voltage. The iteration loops are then started by assigning large minimum cost which will be updated when a smaller cost is found. Then the outer loop (index i) is associated with the next step while, for two-step horizon, the inner loop (index j) is associated with the second next step.

In each iteration, the cost function is calculated, the index is recorded and the minimum cost value is updated when the calculated cost is smaller than the recorded minimum.

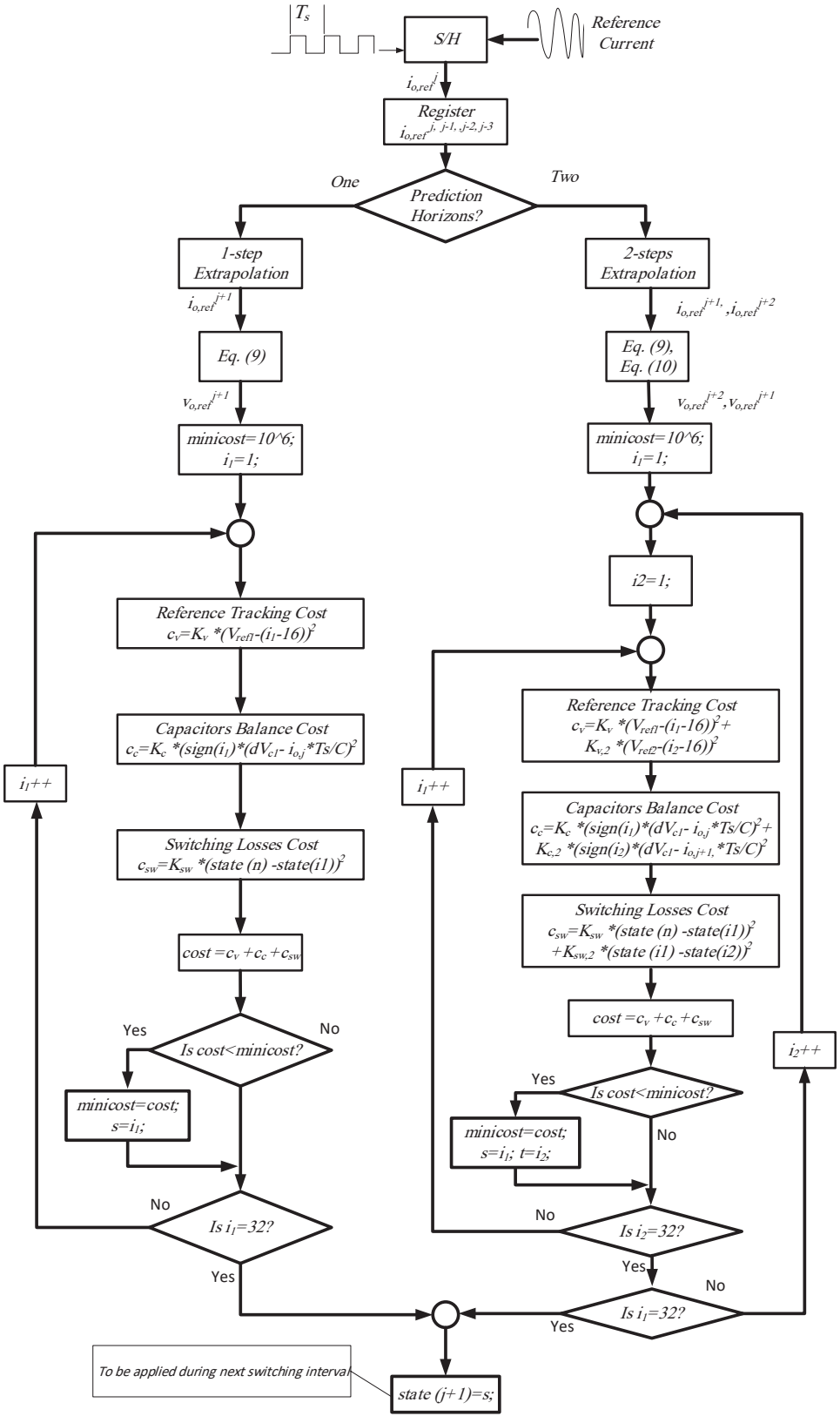


Figure 4. Flow chart of the FCS-MPC control function. FCS-MPC, finite control set-model predictive control.

4. Simulation and Results

The inverter model has been constructed on the Simulink platform, considering the converter parameters given in Table 1. The simulation model layout is shown in Figure 5. The MPC algorithm is implemented using an m-code script within a 'User-Defined Function' block of Simulink at the bottom of the model.

4.1. Model and parameters

An initial investigation has been conducted with a one-step prediction horizon. The effect of changing the weighting factor on various performance indicators is shown in Figure 6. Figures 6(a)–(d) show the average and peak-to-peak ripple voltages of the two capacitors. It can be seen that increasing the capacitor voltage weighting factor (K_c) brings the average capacitors voltage closer to their nominal values. Also, a higher K_c reduced the ripple of both capacitor

Table 1. Circuit and 31-level inverter parameters.

Parameter	Symbol	Value
Voltage step	E	100 V
The load	R, L	100 Ω, L = 0.2 H
Reference current	i_o^*	12 sin (100 πt)
Inverter capacitors	C_1, C_2	100 μF
MOSFET	R_{on}, R_{off}	0.1 Ω, 100 kΩ
Sampling time	T_s	0.5 ms

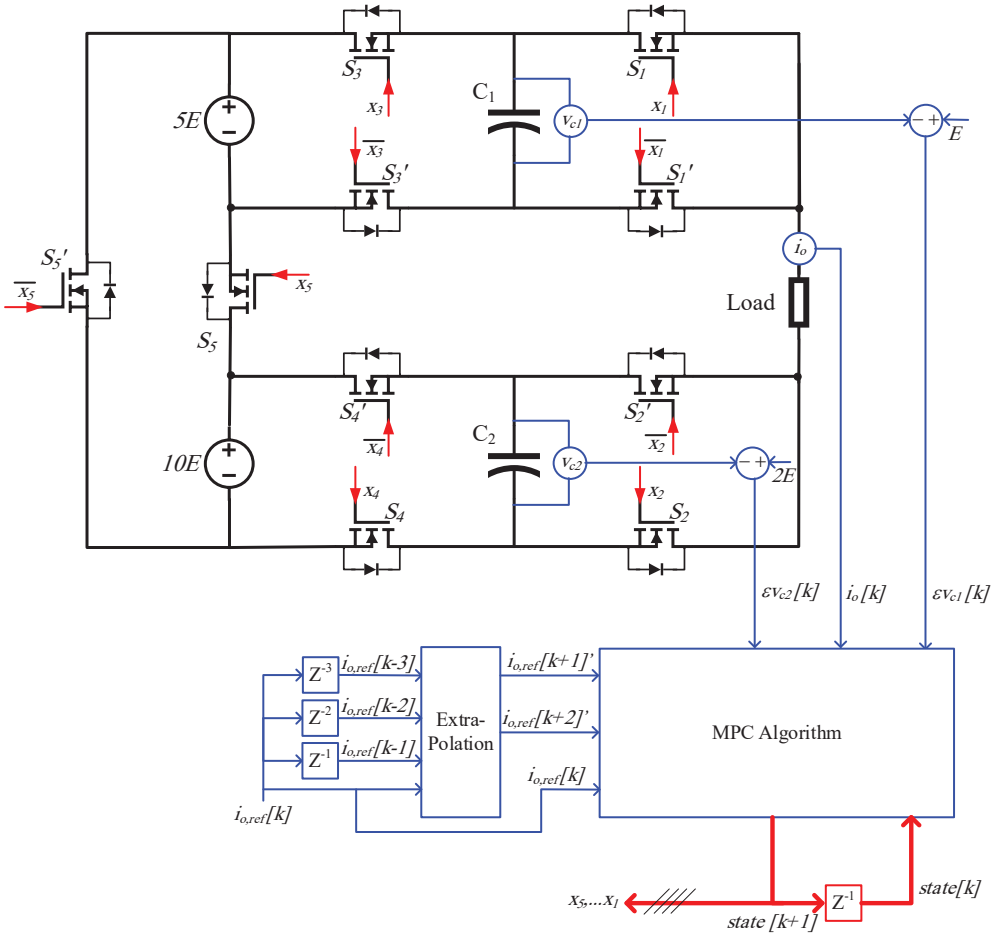
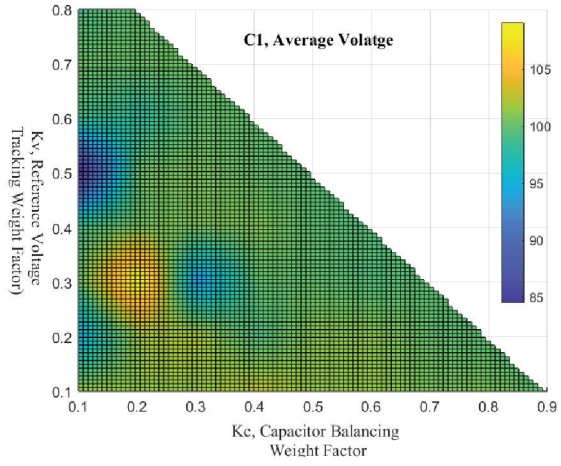
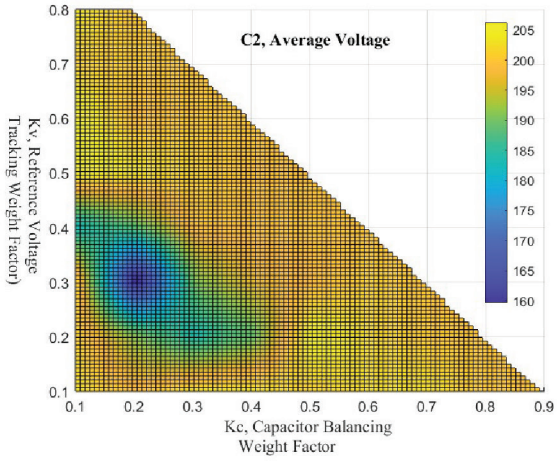


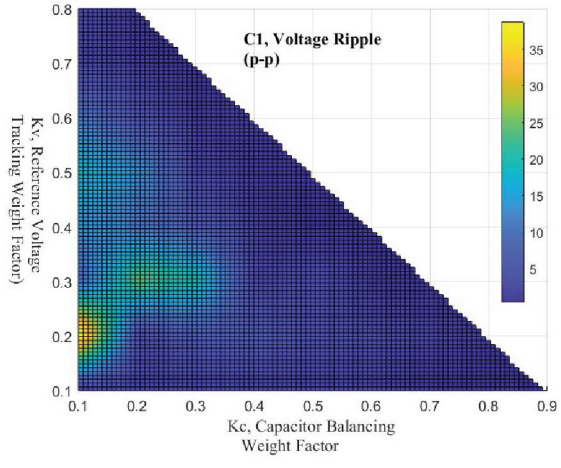
Figure 5. Simulation model of the FCS-MPC controlled 31-level inverter. FCS-MPC, finite control set-model predictive control.



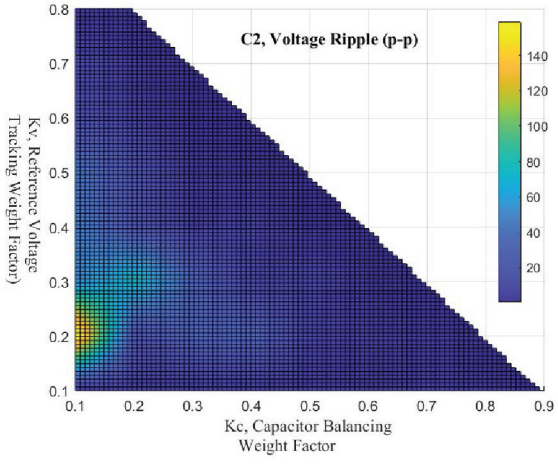
(a) $V_{C1,dc}$



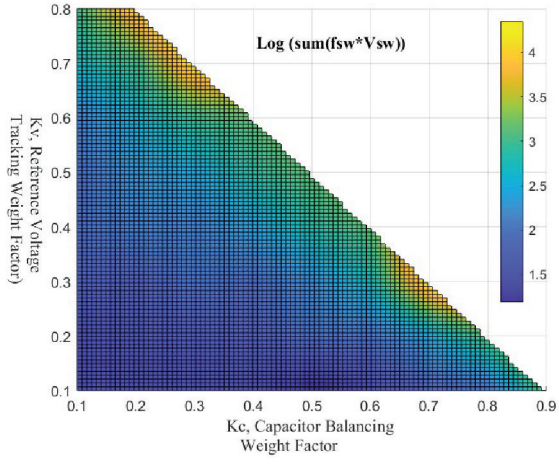
(b) $V_{C2,dc}$



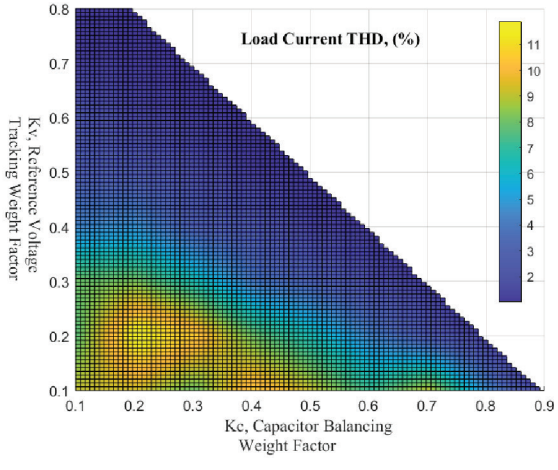
(c) $V_{C1,ripple(p-p)}$



(d) $V_{C2,ripple(p-p)}$



(e) $\log_{10}(\sum V_{sw} f_{sw})$



(f) $THD(i_o)$

Figure 6. Variation of capacitor voltage switching losses and current distortion with the weighting factors with one-step prediction horizon. THD, total harmonic distortion.

voltages. However, increasing K_c leads to higher switching losses as shown in Figure 6(e), which also indicates that increasing the reference tracking weighting factor (K_v) has a similar effect on the switching losses. Lowering both K_v and K_c allows more weight for the switching loss term, since the sum of the three weights is set to 1; in that case lower switching losses can be achieved at the expense of higher current distortion and capacitor voltage ripple.

4.2. One-step prediction horizon

The weighting factors have been tuned to optimise the converter performance considering the following performance indicator (PI):

$$PI = 10 \times THD + \frac{1}{500} \sum V_{sw} f_{sw} + \sqrt{\frac{\int \left(i_{o,ref} - i_o\right)^2 dt}{T}} + 0.1\left|v_{C1} - 100\right| + 0.05\left|v_{C2} - 200\right| \quad (17)$$

where the constants 10, 1/500, 0.1 and 0.05 are used as normalisation factors and the sign Σ denotes the summation for all switching devices, V_{sw} and f_{sw} are the switch voltage and switching frequency and T is the reference current period (20 ms for 50 Hz reference current). The third term on the right-hand side represents the RMS of the current error.

The optimum points of the weighting factors were obtained using the MATLAB function f_{min}, which searches for the values that minimise the cost function defined in Eq. (17). This approach ensures that the selected weighting factors provide the best trade-off between current tracking performance and capacitor voltage regulation. The results from f_{min} directly determine the optimal combination of weighting factors, which are then applied in the predictive control strategy to achieve improved system performance. The optimised operating point was achieved with $K_v = 0.7$ and $K_c = 0.22$. The results are summarised in Table 2.

For the same values of K_v and K_c, the performance of the inverter when starting with zero initial capacitor voltages is depicted in Figure 5. The resultant current is evidently very close to the reference current with RMS deviation from reference value of 0.01643 A as shown in Table 2, the THD of the current is <1%. Figure 7 shows that the capacitor voltages reach the target voltage in about 3 ms, without the need for any dedicated starting protocol. This reflects the stable and fast dynamic response of the FCS-MPC algorithm. The average capacitor voltage deviation is <1% of the average value, and the occasional ripple in the capacitor voltage is <3% of the reference.

Table 2 reveals that the sum of all switching signal pulses multiplied by the normalised switch off-state voltage is 220. This value corresponds either to two switching devices subjected to voltage E and operating at 220 Hz, or to 15 transitions of the switches subjected to the higher voltage (15E). Thanks to the large number of levels, the algorithm tendency to shift the switching towards the switching devices is subjected to lower voltage stress.

4.3. Two-step prediction horizon

The results corresponding to the two-step horizon are presented in Table 3, and the corresponding voltage waveforms are given in Figure 8. No significant improvement has been achieved by extending the prediction horizon to two steps despite the added computational complexity. The two-step prediction requires 31 × 31 evaluations of the cost function at every step compared with 31 calculations for a one-step horizon. On the contrary, the performance indicator defined in Eq. (15) has improved by <5%.

5. Discussion and Comparison to Related Work

To evaluate the advantages of the proposed FCS-MPC-controlled MLI system, a comparison is presented in Table 4 with other published research that introduces innovative MLI topologies of a comparable number of levels. The comparison takes into consideration several factors as discussed in this section.

Table 2. Optimum weighting factors and the corresponding performance indicator with one-step prediction.

Variable	K_v	K_c	THD (i_o)	$\sum V_{sw} f_{sw}$	$\sqrt{\left(\int \left(i_{o,ref} - i_o\right)^2 dt\right)/T}$	$V_{c1,dc}$	$V_{c2,dc}$
Value	0.7	0.22	0.00965	220	0.01643	100.1 V	201.2 V

THD, total harmonic distortion.

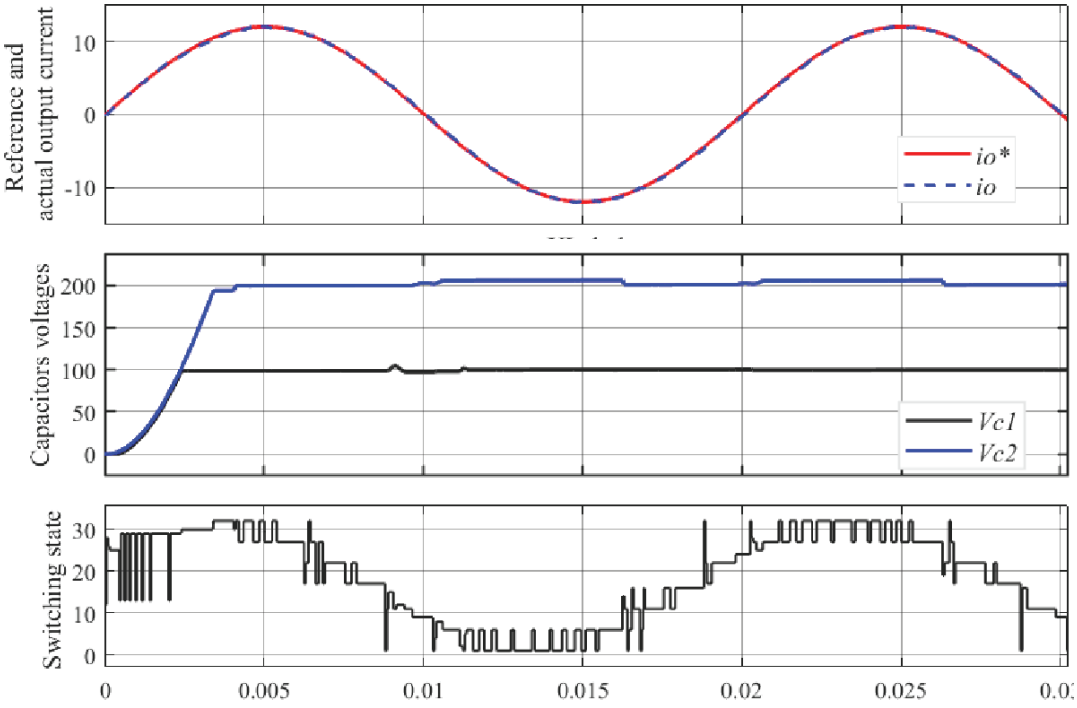


Figure 7. The 31-level inverter operation under the one-step prediction horizon MPC algorithm. The waveforms shown are reference and output current (top), the two capacitor voltages (middle) and the switching state (bottom). MPC, model predictive control.

Table 3. Optimum weighting factors and the corresponding performance with two-step prediction.

Variable	W_{SS}	K_v	K_c	THD (i_o)	$\Sigma V_{sw} f_{sw}$	$\sqrt{\left(\int \left(i_{o,ref} - i_o\right)^2 dt\right)/T}$	$V_{c1,dc}$	$V_{c2,dc}$
Value	0.25	0.7	0.22	0.00973	223	0.0152	100.2 V	201.1 V

THD, total harmonic distortion.

The proposed design achieves the second-lowest number of DC supplies required, N_{dc}, and the ratio of number of supplies to the number of levels (N_{dc}/levels). The lowest ratio is achieved by the converter presented by Arif et al. (2021), which uses a switched capacitors arrangement to generate multiple dc voltage levels. However, the switched capacitor converters require high switching frequency, larger capacitors and deliver lower output power which may restrict their applications.

As shown in Table 4, the proposed design has the lowest number of switching devices, N_{sw}, per level compared with the other six designs. This ratio is approximately 50% lower than that of the second-best design reported by Khasim and Dhanamjayulu (2022).

To obtain a higher number of voltage levels, some MLI designs use capacitors as voltage dividers, FCs or switched capacitors. Capacitor-less MLIs require a larger number of the more expensive, bulky isolated DC supplies. Compared with other designs using capacitors, the proposed design requires the fewest number of capacitors despite its large number of levels.

Total switches voltage (TSV) is calculated as the sum of the voltage stress across all the switches. The proposed MLI considerably reduces the TSV compared with all six other designs. The total capacitors voltage (TCV) is 24% or less than TCV of the three other designs that use capacitors. This factor is important as it affects the converter cost and size.

Finally, the proposed MLI outperforms the other six designs in the number of switching devices in the conduction path per level. This parameter influences the conduction losses of the converter. The proposed design has the second-lowest number of switching devices in the current path after the 17 level inverter presented by Saforo et al. (2020).

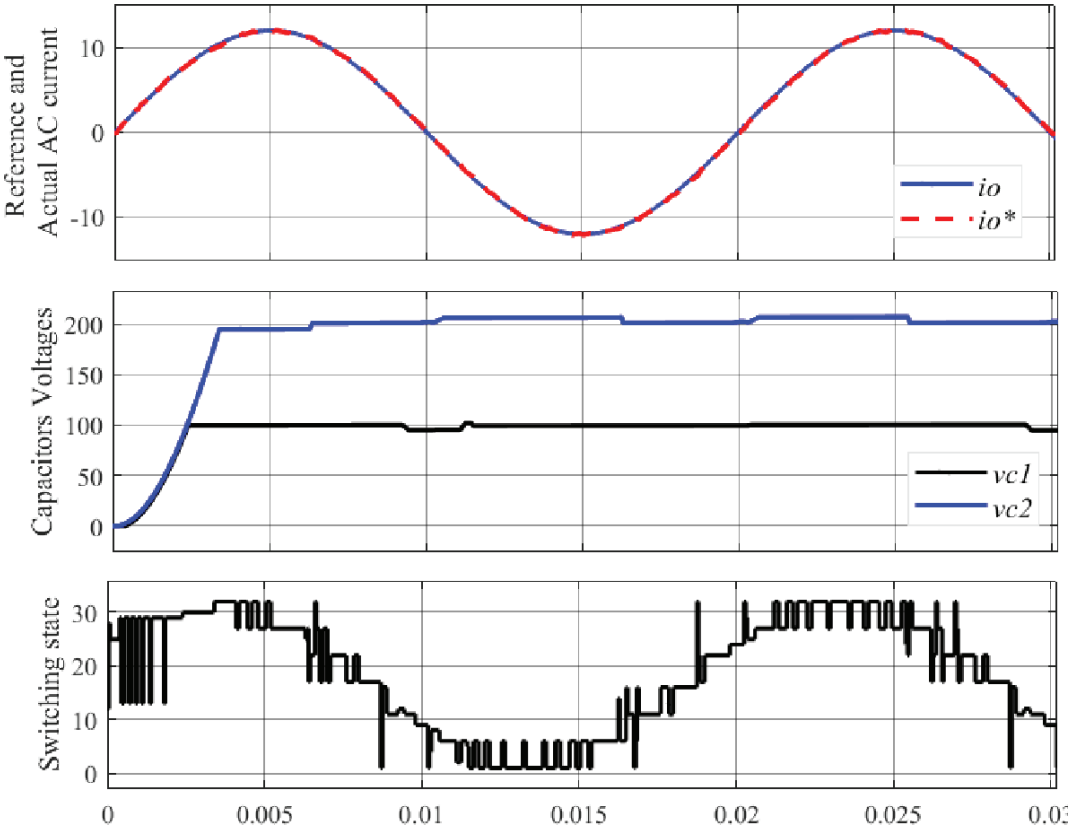


Figure 8. The 31-level inverter operation under the two-step prediction horizon MPC algorithm. The waveforms shown are reference and output current (top), the two capacitor voltages (middle) and the switching state (bottom). MPC, model predictive control.

Table 4. Comparison of the proposed 31 level inverter to other comparable designs.

[Ref]	Saforo et al. (2020)	Arif et al. (2021)	Panda et al. (2021)	Memon et al. (2024)	Khasim and Dhanamjayulu (2022)	Radhakrishnan et al. (2024)	Proposed
N_{Levels}	17	17	17	13	33	25	31
N_{dc}	2	1	4	1	4	4	2
N_{dc}/N_{Levels}	0.118	0.059	0.235	0.077	0.1212	0.16	0.064
N_s	12	12	10	12	16	13	10
$\frac{N_{sw}}{N_{level}}$	0.706	0.706	0.588	0.923	0.485	0.52	0.322
N_{cap}	4	3	0	3	0	0	2
TSV: $\sum V_{off,sw}/V_{o.max,p}$	3.375	4.5	5	4	2.9	-	2.5
TCV: $\sum V_{cap}/V_{o.max,p}$	1	0.875	0	0.833	0	0	0.2
(Max no. of switches in current path)/ levels	4/17 = 0.234	6/17 = 0.353	5/17 = 0.294	5/13 = 0.385	7/33 = 0.212	6/25 = 0.24	5/31 = 0.161

TSV, total switches voltage. TCV, total capacitors voltage.

6. Conclusion

This paper introduces a single-phase 31-level inverter that achieves reduced cost compared with other MLIs offering a similar number of levels. The proposed design uses 2 DC sources, 10 switching devices and 2 low voltage capacitors. It offers low switching losses due to fewer switching events per cycle and the number of switching devices in the current path is the smallest per level among six other recent designs reported in the literature.

This study highlights the significance of closed-loop MPC as an advanced control strategy for MLIs. By applying FCS-MPC to the proposed 31-level inverter, predictive optimisation can improve system performance while overcoming the constraints of traditional control techniques. This demonstrates the potential of MPC to play a central role in next-generation power conversion systems, particularly for renewable energy and high-power industrial applications.

Performance analysis shows that the proposed inverter achieves very low THD and maintains excellent voltage balance of the FCs, even at relatively low switching frequencies. This outstanding performance is enabled by the FCS-MPC algorithm, which not only satisfies multiple control objectives but also provides the flexibility to dynamically prioritise application-specific goals.

The results in this paper are based on modelling and simulation. Experimental validation on a hardware prototype is planned as future work to confirm the practical applicability of the proposed approach.

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