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Extended Order Generalised Integral Control based Circulating Current Mitigating Scheme in Modular Multilevel Converters—A Balancing Approach

Research Paper

Pradeep Kumar*, P. R. Sharma, Poonam Singhal

Department of Electrical Engineering, J C Bose University, YMCA, Faridabad, Haryana, India

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Abstract: In modular multilevel converters (MMCs), circulating currents consist of both DC and AC components. However, these currents are significantly affected by even harmonic distortions, which introduce ripples in the sub-module (SM) capacitor voltages. These ripples contribute to the circulating currents, increasing the voltage stress on the SM switches and adversely impacting overall system performance. This paper presents a systematic approach to mitigating circulating currents by employing an extended order generalised integrator (EOGI), which effectively removes even harmonic components from the converter's legs. The proposed solution has been evaluated against existing methods and has been demonstrated to offer enhanced robustness in the face of parameter uncertainties and sudden load variations. The scheme was initially validated using MATLAB/Simulink, with further real-time performance verification conducted via OPAL-RT simulation and experiments, yielding promising results.

Keywords: *modular multilevel converter • circulating current control • rotating reference frame • PI control*

Abbreviations: CHB, cascaded H-bridge converter; CPS—PWM, carrier phase-shifted PWM; EMI, electromagnetic interference; EOGI, extended order generalised integrator; ESR, equivalent series resistance; FCC, flying capacitor clamped converter; HIL, hardware-in-the-loop; HVDC, high voltage direct current; ISE, integral square error; MMC, modular multilevel converter; NLM, nearest level modulation; NPC, neutral point clamped converter; PWM, pulse width modulation; RL, resistive-inductive load; SHE, selective harmonic elimination; STATCOM, static synchronous compensator; THD, total harmonic distortion.

1. Introduction

Modular multilevel converters (MMCs) have revolutionised high-power electronic systems, particularly in medium- to high-voltage applications such as high voltage direct current (HVDC) transmission, grid integration of renewable energy and industrial motor drives. Their modular architecture, which replaces centralised DC-link capacitors with distributed submodules (SMs) containing individual capacitors, enables unparalleled scalability, efficiency and fault tolerance. Unlike conventional multilevel converters—such as neutral point clamped (NPC), cascaded H-bridge (CHB) and flying capacitor clamped (FCC) topologies—MMCs eliminate the need for bulky transformers and complex voltage balancing circuits, achieving direct high-voltage operation with minimal electro magnetic interference (EMI) and reduced filter requirements (Kouro et al., 2012; Rodriguez et al., 2009). This modularity enables MMCs to scale seamlessly to voltages exceeding hundreds of kilovolts, a feat impractical for traditional converters due to limitations in semiconductor device ratings and thermal management (Etxeberria-Otadui et al., 2008; Rodriguez et al., 2009). While NPC, CHB and FCC converters are widely used in industrial applications, they face inherent challenges in high-voltage scenarios. NPC and FCC converters suffer from uneven voltage distribution across semiconductor

* *Email: pradeepkumarrao110@gmail.com*

switches; hence, complex balancing circuits are required to manage this problem, resulting in high system cost and complexity. CHB converters, though modular, require isolated DC sources via multiple secondary winding transformers, which escalate spatial and financial overheads. These constraints restrict their operational voltage to 6–13.8 kV, making them unsuitable for ultra-high-voltage applications such as HVDC transmission, where series-connected switches would introduce prohibitive insulation and cooling challenges (Dekka et al., 2017).

Introduced by Marquardt in 2001 (Allebrod et al., 2008), MMCs address these limitations by distributing energy storage across SMs, each comprising a capacitor and switches (e.g. half-bridge or full-bridge configurations). This design enables direct connection to high-voltage grids without line-frequency transformers, significantly reducing footprint and cost. MMCs are now integral to modern power systems, including offshore wind farms, static synchronous compensators (STATCOMs) and cross-continental HVDC links (Hagiwara et al., 2010, 2012; Mohammadi and Bina, 2011). However, their operation introduces unique control challenges, primarily stemming from the dynamic interaction between SMs. Key issues include: (1) Submodule Capacitor Voltage Balancing: Fluctuations during charging/discharging cycles create voltage ripple, affecting output waveform quality. (2) Circulating Currents: Arm current imbalances generate even-order harmonics (e.g. 2nd, 4th), increasing switch stress, losses and instability risks. (3) Output Current Regulation: Managing grid synchronisation under variable loads and grid faults.

Circulating currents in MMCs arise from voltage mismatches between the upper and lower arms of each phase leg. These currents, dominated by negative-sequence components at twice the fundamental frequency (2 Ω), do not contribute to the AC output but induce significant losses and thermal stress. Passive methods, such as arm inductors (Li et al., 2013), provide limited suppression while introducing voltage spikes. Active damping techniques (Harnefors et al., 2013) and open-loop controls (Ängquist et al., 2010) and (Ilves et al., 2012a,b) improve performance but remain sensitive to parameter variations and load dynamics. Advanced closed-loop strategies, including PI controllers in double-fundamental rotating frames (Tu et al., 2011), fail under unbalanced grid conditions, while hybrid PI-repetitive controllers (Zhang et al., 2014) trade transient response for steady-state accuracy. Recent advancements, such as decoupled double synchronous reference frame (DDSRF) techniques (Bergna et al., 2013), separate circulating currents into sequence components for precise regulation. However, these methods are computationally intensive and restricted to three-phase systems. Repetitive controllers, though effective for periodic harmonics, exhibit limited bandwidth and struggle with non-integer harmonic orders (He et al., 2015). Furthermore, most strategies target specific harmonics (e.g. 2nd order), neglecting higher even-order components (4th order, 6th order) that arise in practical scenarios with non-linear loads or grid distortions. MMC-HVDC systems enhance power transmission but face reliability issues. Liu et al. (2016) review fault diagnosis and control strategies for various system failures. The MMC-based control scheme, as discussed in Catzin-Contreras et al. (2015), Valdez-Fernandez et al. (2023) and Catzin-Contreras et al. (2023), has high computational complexity, requires precise tuning and may struggle with extreme unbalances. Additionally, real-time simulation demands high-performance hardware, thus increasing implementation challenges and limiting cost-sensitive applications (Rodriguez et al., 2005; She et al., 2012; She and Huang 2012; Li and Wang 2013; Sreedhar et al., 2014; Bahrani et al., 2016; Satya Narayana and Dahiya 2021; Sobanski et al., 2021; Hans et al., 2024).

Summarising key prior works, their control strategies and limitations (e.g. single-harmonic focus of resonant controllers, instability under parameter variations). The literature comparison in Table 1 provides a quick reference for readers to contextualise our work.

This paper introduces a novel control framework combining Proportional (P) control with multi-harmonic extended order generalised integrators (EOGIs) to suppress all even-order circulating currents simultaneously. Unlike prior single-frequency resonant controllers, the parallel integration of 2nd, 4th and 6th-order EOGIs enables comprehensive harmonic cancellation across diverse operating conditions. Key innovations include: (1) *Hybrid Feedback Architecture*: Integrates impedance control and sensor fusion to maintain stability under parameter uncertainties (e.g. capacitor degradation, load shifts). (2) *Popov Criterion-Based Stability Analysis*: Rigorous non-linear stability validation, ensuring robustness during transients like grid faults. (3) *Integral Square Error (ISE)-Optimised Gains*: Minimise tuning complexity while maximising harmonic attenuation. Validated through MATLAB (MATLAB 2023b)/Simulink simulations and OPAL-RT hardware-in-the-loop (HIL) testing, the proposed method reduces total harmonic distortion (THD) from 9.4% to 2.4% and cuts circulating currents by 95%, outperforming conventional PI and repetitive controllers. Section 2 derives the MMC's mathematical model, while Section 3 details the EOGI control design and stability analysis. Section 4 presents comparative simulation and HIL results, and Section 5 discusses practical implementation challenges. The work concludes with guidelines for industrial deployment, positioning MMCs as a cornerstone of next-generation power systems.

Table 1. Literature review.

Reference	Focus area	Key contribution	Limitations
Marquardt (2001)	MMC fundamentals	Introduced MMC topology for scalable high-voltage applications	Early work lacked detailed control strategies for circulating currents
Rodriguez et al. (2009)	Multilevel converters	Overview of multilevel converter topologies and their industrial applications	Limited focus on MMC -specific challenges like capacitor balancing
Dekka et al. (2017)	MMC evolution	Comprehensive review of MMC topologies, modulation and control methods	Did not address advanced harmonic suppression techniques
Tu et al. (2011)	Circulating current control	Proposed PI controllers in double-fundamental rotating frame for harmonic reduction	Ineffective under unbalanced grid conditions
Li et al. (2013)	Passive control method	Introduced arm inductance/resistance for circulating current suppression	High voltage disturbances and instability risks
Zhang et al. (2014)	Hybrid control	Combined PI and repetitive controllers for harmonic elimination	Complex tuning, limited transient performance
He et al. (2015)	Series PI-repetitive control	Enhanced PI transient performance with repetitive steady-state control	Restricted bandwidth, unsuitable for non-integer harmonics
Bergna et al. (2013)	Energy-based control	Decoupled double synchronous frame for sequence component regulation	High computational complexity, limited to three-phase systems
Proposed method	EOGI-based control	Parallel multi-harmonic EOGIs (2nd, 4th and 6th-order)	Requires ISE-optimised gains but achieves stability via Popov criterion

EOGI, extended order generalised integrator; ISE, integral square error; MMC, modular multilevel converter.

1.1. Key enhancements

- **Logical progression:** Begins with MMC's significance → contrasts with conventional converters → identifies MMC-specific challenges → critiques prior solutions → introduces novel EOGI approach.
- **Technical depth:** Explicitly defines circulating current mechanisms, harmonic orders and stability criteria.
- **Application context:** Links MMC advantages to real-world use cases (HVDC, STATCOMs).
- **Novelty emphasis:** Highlights multi-harmonic suppression and Popov-based stability, absent in prior works.
- **Reader guidance:** Concludes with paper structure to orient the audience.

2. Basic Circuit and Mathematical Model of MMC

2.1. Block diagram of MMC

The basic block diagram of a 3-phase MMC is presented in Figure 1. Each phase of a MMC is represented as a leg, which consists of two arms: the upper arm connected to the positive pole of the DC supply and the lower arm to the negative pole of the DC supply. Each arm contains N SMs connected in series. The configuration of these SMs varies based on the application, including types such as Half-bridge SM, Full-bridge SM, Flying Capacitor SM and Diode-Clamped SMs. In the provided block diagram, a half-bridge SM with two switches and a capacitor is used. The gating signals to the two switches are complementary. When the upper switch is turned on, the capacitor is inserted into the converter circuit and either charges or discharges depending on the direction of the arm current. When the lower switch is turned on, the capacitor is bypassed, resulting in the SM's output voltage being zero.

2.2. Mathematical modelling of MMC

The equivalent circuit diagram of 3-phase MMC block diagram is shown in Figure 2. Each SM can be replaced with an equivalent capacitor to hold a nominal voltage of V_{dc}/N. Let $m \in \{a, b, c\}$ phase.

V_{dc} = DC Bus Voltage;
$V_{m,\,up}$ = Output voltage of the upper arm of respective phase m;
$V_{m,\,low}$ = Output voltage of the lower arm of respective phase m;
i_m = Output current in phase m;
$i_{cir,m}$ = Circulating current flowing in each phase m;
$i_{m,up}$ = Output current of upper arm of respective phase m;
$i_{m,low}$ = Output current of lower arm of respective phase m;

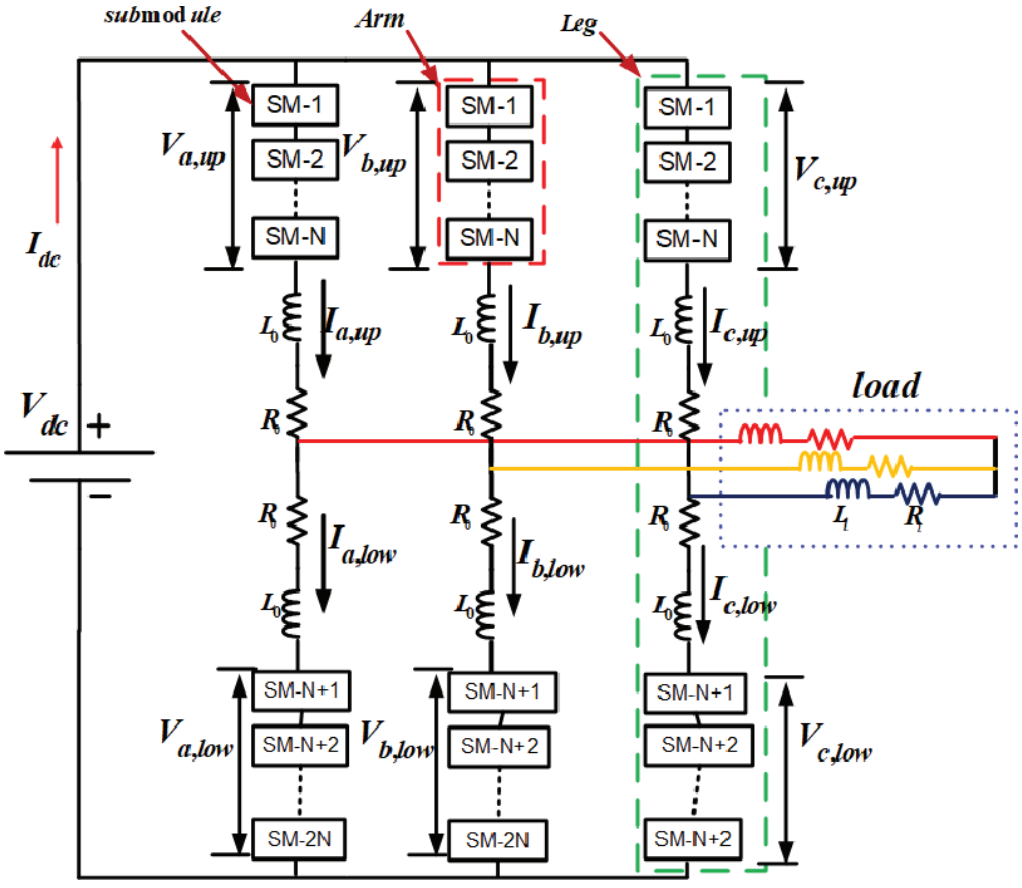

Figure 1. Basic configuration of three-phase MMC. MMC, modular multilevel converter.

From the equivalent diagram of a three-phase MMC, the total arm current flowing in each arm depends on output current and circulating current in Eq. (1).

$$i_{m,up} = i_{cir} + \frac{i_m}{2} \tag{1}$$

Similarly for the lower arm in Eq. (2)

$$i_{m,\text{low}} = i_{\text{cir}} - \frac{i_m}{2} \tag{2}$$

By adding these two equations, we can get the equation for the circulating current, which is given by Eq. (3)

$$i_{cir,m} = \frac{1}{2}\left(i_{m,\text{up}} + i_{m,\text{up}}\right) \tag{3}$$

Now, by applying KCL at the midpoint of each leg of the converter, we obtain Eq. (4)

$$i_m = i_{m,\text{up}} - i_{m,\text{low}} \tag{4}$$

According to KVL, the output voltage for each phase *m* can be written as given in Eqs (5)–(6), For the upper arm of phase *m*

$$-\frac{1}{2}V_{dc} - v_{m,\text{up}} + L_o\frac{di_{m,\text{up}}}{dt} + R_o i_{m,\text{up}} + v_m = 0 \tag{5}$$

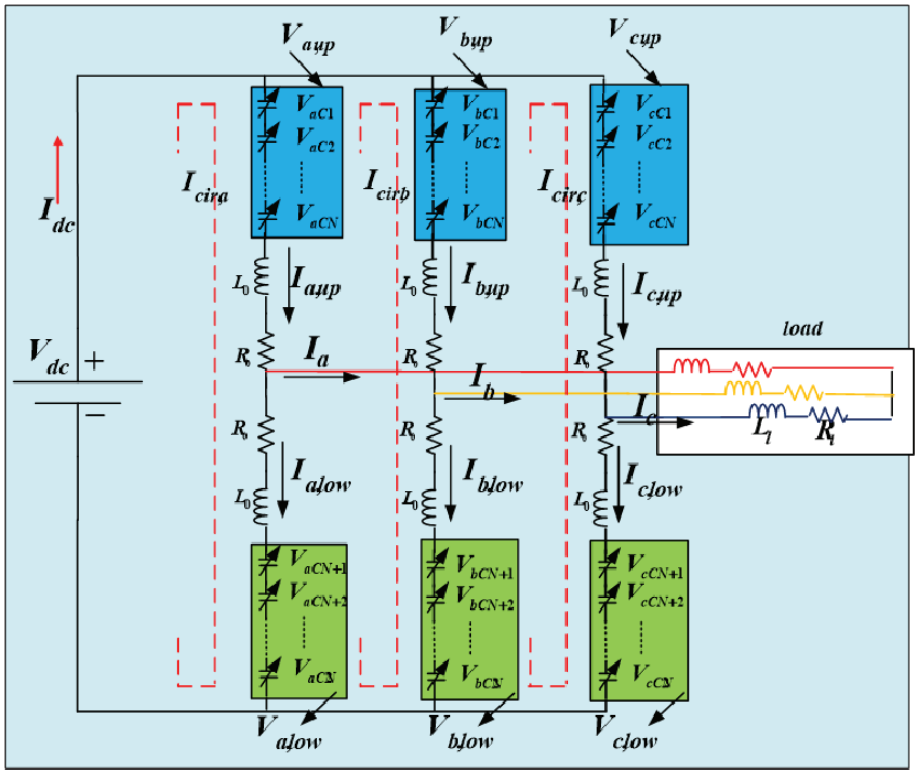

Figure 2. Equivalent diagram of a 3-phase MMC. MMC, modular multilevel converter.

Similarly, for the lower arm

$$\frac{1}{2}V_{dc} - v_{m,\text{low}} + L_o\frac{di_{m,\text{low}}}{dt} + R_o i_{m,\text{low}} + v_m = 0 \tag{6}$$

By adding Eqs (5) and (6), the output voltage of the converter on the ac side is obtained as given in Eq. (7)

$$v_m = \frac{1}{2}\left(v_{m,\text{low}} - v_{m,up}\right) - \frac{1}{2}\left(L_o\frac{di_m}{dt} + R_o i_m\right) \tag{7}$$

Similarly, the circulating current equation is given in Eq. (8) from the inner circulating current loop

$$-V_{dc} + v_{m,up} + 2L_o\frac{di_{cir,m}}{dt} + 2R_o i_{cir,m} + v_{m,\text{low}} = 0 \tag{8}$$

By modifying Eq. (8), we can get Eq. (9) for the inner characteristic of the MMC for phase *m*

$$\left(L_o\frac{di_{cir,m}}{dt} + R_o i_{cir,m}\right) = \frac{1}{2}\left\{V_{dc} - \left(v_{m,\text{low}} + v_{m,up}\right)\right\} \tag{9}$$

From the above analysis, the control of output voltage and circulating current can be achieved by varying the upper arm voltage and lower arm voltage, i.e. by switching pattern of SMs in each arm. To achieve the required amount of voltage at the output and maintain the equilibrium between the input dc voltage and output voltage of the phase leg, the Eqs (10) and (11) for the upper arm and lower arm voltages are used.

$$v_{m,\text{up}} = \frac{1}{2}\left(V_{dc} - v_m\right) \tag{10}$$

$$v_{m,\text{low}} = \frac{1}{2}\left(V_{dc} + v_m\right) \tag{11}$$

These equations are valid under ideal assumptions of each SM, and the capacitor voltage will be equal and maintained at a constant value of V_{dc}/N. Practically, this is not the case as charging and discharging of SM capacitors occur due to load current and circulating current flowing through them. To make it happen, a voltage balancing controller is required. v_m is the voltage at the output of the respective phase, as in Eq. (12).

$$v_m = \frac{1}{2} V_{dc} M \sin\left(\omega t + \theta_m\right) \tag{12}$$

$M = 2\sqrt{2}\frac{v_m}{v_{dc}} =$ modulation index,

$\theta_m =$ initial phase angle of output,

$\omega =$ initial angular frequency of output.

2.3. Mathematical representation of circular current

As discussed in earlier sections, the charging and discharging of the SM capacitor by the load current causes voltage disturbances in the capacitors as voltages vary from the nominal value. The fluctuations in the capacitors' voltage result in the generation of circulating current. The dependence of harmonics in circulating current on SMs capacitor voltage disturbance is presented in Eq. (22). Now, let's derive a mathematical expression for the capacitor voltage fluctuations and thereby the circulating current based on the analysis and results of Eq. (23). Initially, let's assume all the SM capacitors of each leg hold the voltage at their nominal value as shown in Eq. (13).

$$v_{Cm1} = v_{Cm2} = \ldots = v_{CmN} = v_{Cm(N+1)} = \ldots = v_{Cm(2N)} = \frac{V_{dc}}{N} \tag{13}$$

During the operation of the converter, the change in nominal value of each capacitor in upper arm and the lower arm is $\Delta v_{Cm,up}$ and $\Delta v_{Cm,low}$, respectively. For upper arm, each SM capacitor voltage is given by Eq. (14).

$$v_{Cm1} = v_{Cm2} = \ldots = v_{CmN} = \frac{v_{Cm,up}}{N} = \frac{V_{dc} + \Delta v_{Cm,up}}{N} \tag{14}$$

Similarly, for the lower arm, each SM capacitor voltage is given by Eq. (15).

$$v_{Cm(N+1)} = v_{Cm(N+2)} = \ldots = v_{Cm(2N)} = \frac{v_{Cm,low}}{N} = \frac{V_{dc} + \Delta v_{Cm,low}}{N} \tag{15}$$

$v_{Cm,up}$ and $v_{Cm,low}$ are the sum of total SM capacitors' voltages in the upper and lower arm, respectively. The circulating current flowing through each leg consists of DC component and even-order harmonics, as shown in Eq. (16).

$$i_{cir,m} = \frac{i_{dc}}{3} + \sum_{j=1}^{\infty} i_j \tag{16}$$

i_{dc} is the DC of the input and i_j is the jth order of the harmonic components of the circulating current. For the upper arm, the input power is shown in Eq. (17)

$$p_{\text{arm}-m,\text{up}} = v_{m,\text{up}} \times i_{m,\text{up}} \tag{17}$$

where $v_{m,\text{up}} = \frac{1}{2}\left(V_{dc} - v_m\right)$

$$v_{m,\text{up}} = \frac{1}{2} V_{dc} - \frac{1}{2} V_{dc} M \sin\left(\omega t + \theta_m\right) = \frac{V_{dc}}{2}\left(1 - M \sin\left(\omega t + \theta_m\right)\right) \tag{18}$$

From Eqs (1)–(16)

$$i_{m,\text{up}} = \frac{i_{dc}}{3} + \sum_{j=1}^{\infty} i_j + \frac{1}{2} i_m \tag{19}$$

By substituting Eqs (18) and (19) in (17), we get (20)

$$p_{\text{arm}-m,\text{up}} = \frac{V_{dc}}{2}\left(1 - M\sin\left(\omega t + \theta_m\right)\right)*\left(\frac{i_{dc}}{3} + \sum_{j=1}^{\infty} i_j + \frac{1}{2} i_m\right) \tag{20}$$

Similarly, for the lower arm, the input power is given by Eq. (21)

$$p_{\text{arm}-m,\text{low}} = \frac{V_{dc}}{2}\left(1 - M\sin\left(\omega t + \theta_m\right)\right)*\left(\frac{i_{dc}}{3} + \sum_{j=1}^{\infty} i_j - \frac{1}{2} i_m\right) \tag{21}$$

And the energy stored in the SM capacitors of upper and lower arm is given by Eqs (22)–(23)

$$E_{m,\text{up}} = \frac{1}{2N} C.v_{Cm,\text{up}}^2 \tag{22}$$

$$E_{m,\text{low}} = \frac{1}{2N} C.v_{Cm,\text{low}}^2 \tag{23}$$

where *C* is the capacitance of each SM. The differentiation of energy stored in each arm with respect to time is equal to power in each arm, which is given by Eq. (24).

$$\frac{dE_{m,\text{up}}}{dt} = \frac{V_{dc}}{2}\left(1 - M\sin\left(\omega t + \theta_m\right)\right)*\left(\frac{i_{dc}}{3} + \sum\nolimits_{j=1}^{\infty} i_j - \frac{1}{2} i_m\right) \tag{24}$$

Then, voltage disturbances in the two arms can be written as in Eqs (24)–(25).

$$\Delta v_{Cm,\text{up}} = \frac{N}{2C}\int\left(1 - M\sin\left(\omega t + \theta_m\right)\right)\left(\frac{i_{dc}}{3} + \sum_{j=1}^{\infty} i_j + \frac{1}{2} i_m\right) \tag{25}$$

Similarly,

$$\Delta v_{Cm,\text{low}} = \frac{N}{2C}\int\left(1 - M\sin\left(\omega t + \theta_m\right)\right)\left(\frac{i_{dc}}{3} + \sum_{j=1}^{\infty} i_j - \frac{1}{2} i_m\right) \tag{26}$$

Now the modified output voltage of the upper and lower arm can be written as shown in Eqs (27) and (28):

$$v_{m,\text{up}} = \frac{1}{2}\left(1 - M\sin\left(\omega t + \theta_m\right)\right).\left(V_{\text{dc}} + \Delta v_{Cm,\text{up}}\right) \tag{27}$$

$$v_{m,\text{low}} = \frac{1}{2}\left(1 + M\sin\left(\omega t + \theta_m\right)\right).\left(V_{\text{dc}} + \Delta v_{Cm,\text{low}}\right) \tag{28}$$

Now the total voltage across each phase leg is given in Eq. (29).

$$v_{m,\text{up}} + v_{m,\text{low}} = V_{\text{dc}} + \frac{1}{2}\left(\Delta v_{Cm,\text{up}} + \Delta v_{Cm,\text{low}}\right) + \frac{1}{2}\left(M\sin\left(\omega t + \theta_m\right)\right).\left(\Delta v_{Cm,\text{low}} - \Delta v_{Cm,\text{up}}\right) \tag{29}$$

$$= V_{\text{dc}} + v_{m,\text{har}}$$

Here, $v_{m,\text{har}}$ is a voltage difference between the input DC system voltage and the phase leg voltage, which is the cause of introducing circulating current harmonics. So, this $v_{m,\text{har}}$ is known as a harmonic voltage disturbance.

$$v_{ah} = \frac{1}{2}\left(\Delta v_{Cm,\text{up}} + \Delta v_{Cm,\text{low}}\right) + \frac{1}{2}\left(M\sin\left(\omega t + \theta_m\right)\right).\left(\Delta v_{Cm,\text{low}} - \Delta v_{Cm,\text{up}}\right) \tag{30}$$

Based on Eqs (25) and (26), we obtain

$$\left(\Delta v_{Cm,\text{up}} + \Delta v_{Cm,\text{low}}\right) = \frac{N}{2C}\int\left(\frac{2i_{dc}}{3} + 2\sum_{j=1}^{\infty} i_j - M\sin\left(\omega t + \theta_m\right) i_m\right)dt) \tag{31}$$

$$\left(\Delta v_{Cm,\text{up}} - \Delta v_{Cm,\text{low}}\right) = \frac{N}{2C}\int\left(-i_m + 2M\sin\left(\omega t + \theta\right)\frac{i_{dc}}{3} + 2M\sin\left(\omega t + \theta\right)\sum_{j=1}^{\infty} i_j\right)dt \tag{32}$$

The output current equation from the power balance theory at each phase leg is given in Eq. (33)

$$i_m = I_o \sin\left(\omega t - \varphi\right) = \frac{4i_{dc}}{3M\cos\left(\varphi\right)}\sin\left(\omega t - \varphi\right) \tag{33}$$

Here φ is the impedance angle of the load. Now, by substituting Eq. (33) in Eq. (31), we get (34)

$$\left(\Delta v_{Cm,\text{up}} + \Delta v_{Cm,\text{low}}\right) = \frac{N}{2C}\int\left(\frac{2i_{dc}}{3\cos\left(\varphi_m\right)}\cos\left(2\omega t - \varphi\right) + \sum_{j=1}^{\infty} i_j\right)dt \tag{34}$$

Based on Eqs (34) and (32), $v_{\text{m,har}}$ can be written as Eq. (35)

$$v_{m,\text{har}} = \frac{N}{4C}\int\left(\frac{2i_{dc}}{3\cos\left(\varphi_m\right)}\cos\left(2\omega t - \varphi\right) + \sum_{j=1}^{\infty} i_j\right)dt + \frac{NM}{4C}\sin\left(\omega t\right)\int\left(-\frac{4i_{dc}}{3M\cos\left(\varphi\right)} + 2M\sin\left(\omega t\right)\frac{i_{dc}}{3} + 2M\sin\left(\omega t\right)\sum_{j=1}^{\infty} i_j\right)dt \tag{35}$$

From the above equations, we can conclude that load current causes second-order harmonics in voltage disturbance $v_{m,\text{har}}$, which is responsible for even-order harmonics in the circulating currents.

3. Proposed Circulating Current Control Method

3.1. Control mechanism

Figure 3 presents the complete block diagram of the proposed control mechanism for minimising circulating currents. A key requirement in MMC is the ability to regulate controlled variables to follow reference commands with zero steady-state error, even in the presence of unknown disturbances. To address steady-state errors, an integral controller with optimal gains must be employed. In this case, the unknown disturbance refers to the circulating currents within a fixed period. Traditionally, resonant and repetitive controllers have been used to suppress circulating currents. However, resonant controllers are ineffective at higher-order harmonics, limiting their applicability in this context. To overcome this limitation, this article presents an enhanced version of the EOGI to mitigate harmonics while maintaining system stability. The proposed controller processes circulating currents from the MMC's output terminals and operates as a multi-harmonic controller.

The optimal proportional and integral gains for the controller are determined using the ISE optimisation technique. In this design, ω_c represents the bandwidth, *Ti* the measurement lag, G_{rc} the gain, ω_o the resonant frequency, K_p the proportional gain and K_i the integral gain of the controller. Additionally, T_i serves as the controller's time constant. In the proposed circulating current control, for simplicity, stationary $\alpha\beta$ frame is used instead of the rotating frame, where the three-phase circulating currents of MMC-$i_{m,\text{cir}}$ are transformed into real and imaginary terms i.e. into two-phase time-varying variables $i_{\alpha,\text{cir}}$ and $i_{\beta,\text{cir}}$. As the main objective here is to minimise the circulating currents, one needs to compare the actual circulating current $i_{m,\text{cir}}$ with zero reference signal $i_{m,\text{cir,ref}}$. The error signal will be fed to the proposed P + EOGIs-based controller, which consists of a proportional controller in parallel with various EOGIs like second, fourth and sixth order. These EOGIs are tuned to a particular harmonic frequency, thereby attenuating that particular harmonic frequency component.

The detailed internal structure of the proposed Proportional plus EOGI-based controller is shown below. The transfer function of the controller is given in Eq. (36).

$$\text{TF} = k_p + \frac{k_h\left(h\omega\right)s}{s^2 + k_h\left(h\omega\right)s + \left(h\omega\right)^2} \tag{36}$$

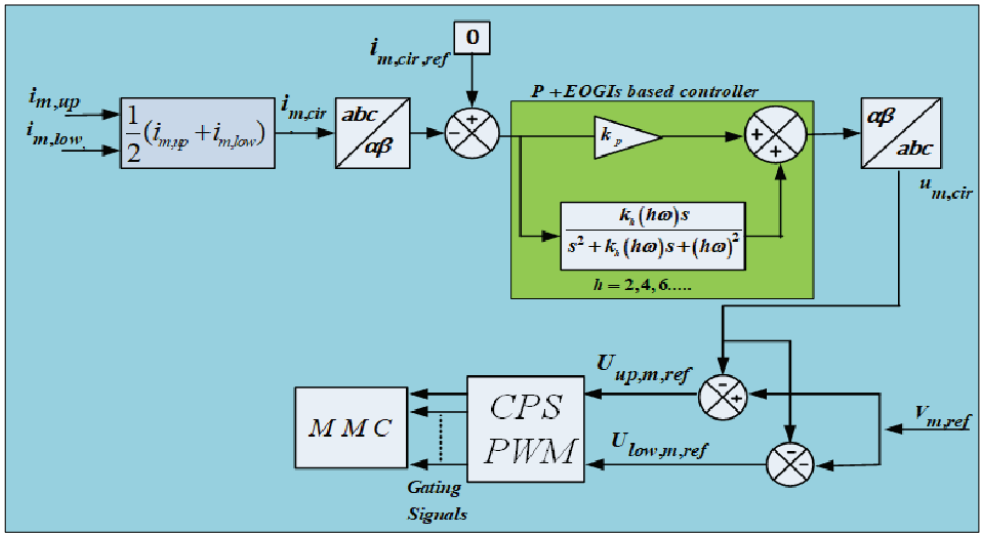

Figure 3. Block diagram of proposed P + EOGIs based controller for minimisation of circulating current control. EOGIs, extended order generalised integrator; MMC, modular multilevel converter; PWM, pulse width modulation.

where h = 2, 4, 6, …. The reference signal generated by the output of the circulating current controller $u_{m,cir}$ is combined with the voltage disturbance reference signal $V_{m,ref}$ to generate reference signals $U_{up,m,ref}$ and $U_{low,m,ref}$ for the pulse width modulation (PWM) technique. Gating signals for the MMC can be generated using the carrier phase shift PWM technique with the above reference signals. Here, the voltage reference signal $V_{m,ref}$ is generated by comparing the actual converter output voltage with the desired output voltage at the converter.

3.2. Stability analysis

The pole-zero plot of the characteristic graph is depicted in Figure 4, where all poles and zeros are positioned on the left-hand side (LHS) of the complex plane, indicating that the proposed controller is inherently stable. This placement signifies that the system's natural response will decay over time, ensuring overall system stability. To further verify this stability, various input signals, such as an impulse—simulating a sudden load change commonly encountered in practical conditions, were applied. The impulse response, as demonstrated in Figure 4, was tested across both lower and higher orders. The results revealed that the controller successfully reached a steady state after the impulse input, confirming its robustness and stability even under challenging conditions. The stability analysis of the proposed controller was extended through magnitude and phase response evaluations under different scenarios. Initially, the system was tested using a proportional controller without optimal gain, followed by a version with optimally tuned gains. While the optimally tuned proportional controller provided improved performance, a residual steady-state error remained. To eliminate this error, an inner-loop integral controller was introduced, which significantly reduced the steady-state error. However, despite this improvement, the combined proportional and integral controllers exhibited limitations across a range of frequencies, potentially jeopardising the system's stability under certain operating conditions. To ensure stability across all frequencies, an inner second-order resonant controller was incorporated. This resonant controller was specifically designed to handle higher-order harmonics, where traditional proportional and integral controllers struggle. By integrating this second-order resonant controller, the system maintained stability across the entire frequency spectrum, as illustrated in the refined frequency response plot in Figure 4. The optimal parameters for the controller were calculated using the ISE optimisation technique, with the circulating currents defined as the objective function. Conventional stability analysis methods were insufficient to fully understand the dynamic behaviour of the system. Therefore, the Popov criterion—a method particularly suited for systems with non-linear elements—was employed to rigorously assess the dynamic stability of the proposed controller. This comprehensive approach ensured that the controller remains stable under a wide range of operational scenarios, making it robust for real-world applications.

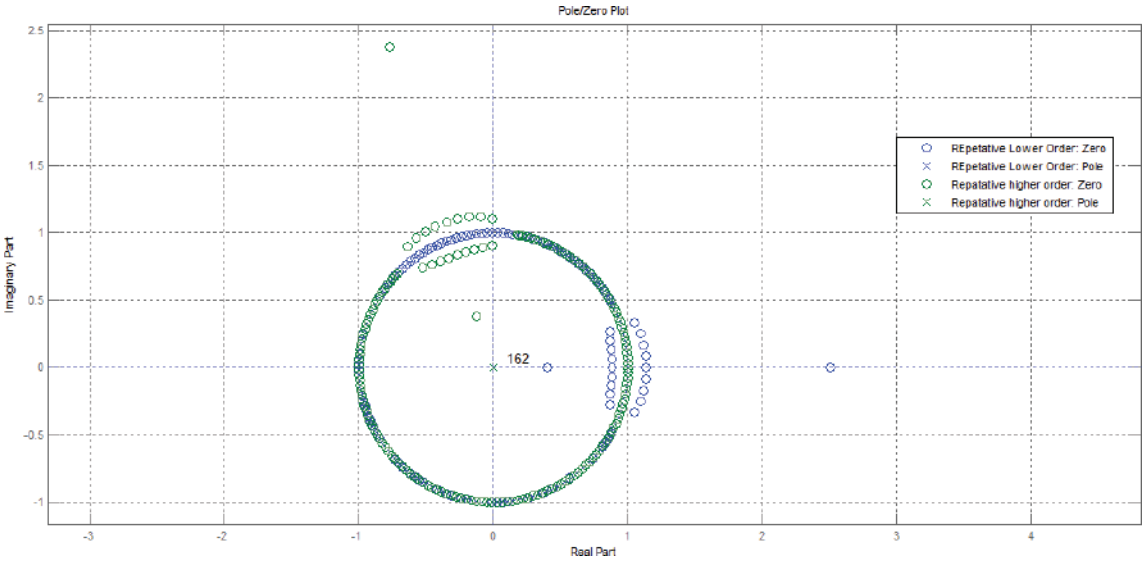

Figure 4. Proposed controller used for MMC showing pole/zero responses. (X-axis-Real Part and Y-axis-Imaginary part). MMC, modular multilevel converter.

4. Results

The parameters of the proposed system are given in Table 2. Initially, the proposed scheme has been investigated by using MATLAB/Simulink (MATLAB 2023b), and these are verified by conducting the experiments in real-time. Some cases have been investigated and their results are explored in this section. In this case, the system has been investigated with a conventional PI-controller and with the proposed controller using a resistive load. The conventional PI-controller has been enabled at 0.2 s and then a step change in load is given. At 0.2 s, the peak circulating current reaches around 400 A, and after application of the PI-controller, it is mitigated between 150 A and 200 A, which is not an acceptable range. Hence, the same system is tested with the proposed controller, and better results were observed.

Further, to examine the system performance, it has been decided to test the proposed scheme using a resistive load. The proposed controller has been enabled at 0.2 s and then at a step change in load given. Up to 0.2 s, the peak circulating current touches around 400 A and after application of the controller, it is mitigated between 4 A and 8 A, ensuring the proper operation of the controller.

Here, all these detailed wave-forms and their respective labelling are given in Figure 5, where wave forms are provided for circulating current, active power, Grid voltage, Grid current, converter voltage, converter current, upper arm voltage, lower arm voltage, input DC voltage and input DC current, respectively. Also, it can be observed that circulating currents remain same as usual even under variable (step change) load conditions. Hence, all these detailed wave-forms and their respective labelling have been given in Figure 6. From these figures, it is clear that voltage fluctuations and current fluctuations in DC bus have been drastically reduced, which consequently improves the performance of the converter voltage and converter current.

To demonstrate robustness, we conducted simulations and real-time OPAL-RT tests as shown in Figure 7 under diverse load conditions, including resistive-inductive (RL), resistive-capacitive (RC) and non-linear loads (e.g. diode rectifiers). OPAL-RT simulations replicate real-time hardware constraints (e.g. computational latency, sensor noise), bridging the gap between idealised MATLAB models and physical deployments. This is critical for high-power MMCs, where software-hardware co-validation ensures stability under grid faults and transient loads Eqs (28) and (31). These tests revealed consistent circulating current suppression, with peak values remaining below 10 A even during abrupt load changes. Additionally, we performed a 24-h cyclic load test (50%–150% rated load) to evaluate long-term stability, which showed sustained performance with minimal current fluctuations, as in Figure 8a. While generalised integrators are established in harmonic suppression, our work introduces a novel multi-harmonic EOGI architecture tailored for MMCs. Unlike prior studies focussing on single-frequency resonant controllers, our approach employs parallel EOGIs combined with a proportional controller to suppress all even-

Table 2. Simulation parameters used in proposed configuration.

S. no	Parameter	Value
1	Rated active power	20 MW
2	Rated reactive power	6.6 VAR
3	DC supply	33 kV
4	DC link capacitor value	300 μF
5	Converter output voltage RMS	11 kV
6	Number of sub-modules per arm	6
7	Each sub-module capacitor value	0.03 F
8	Each sub-module capacitor voltage	5,500 V
9	Resistance of arm	0.01 Ω
10	Inductance of arm	5 mH
11	Line frequency	50 Hz
12	Carrier switching frequency	2 kHz

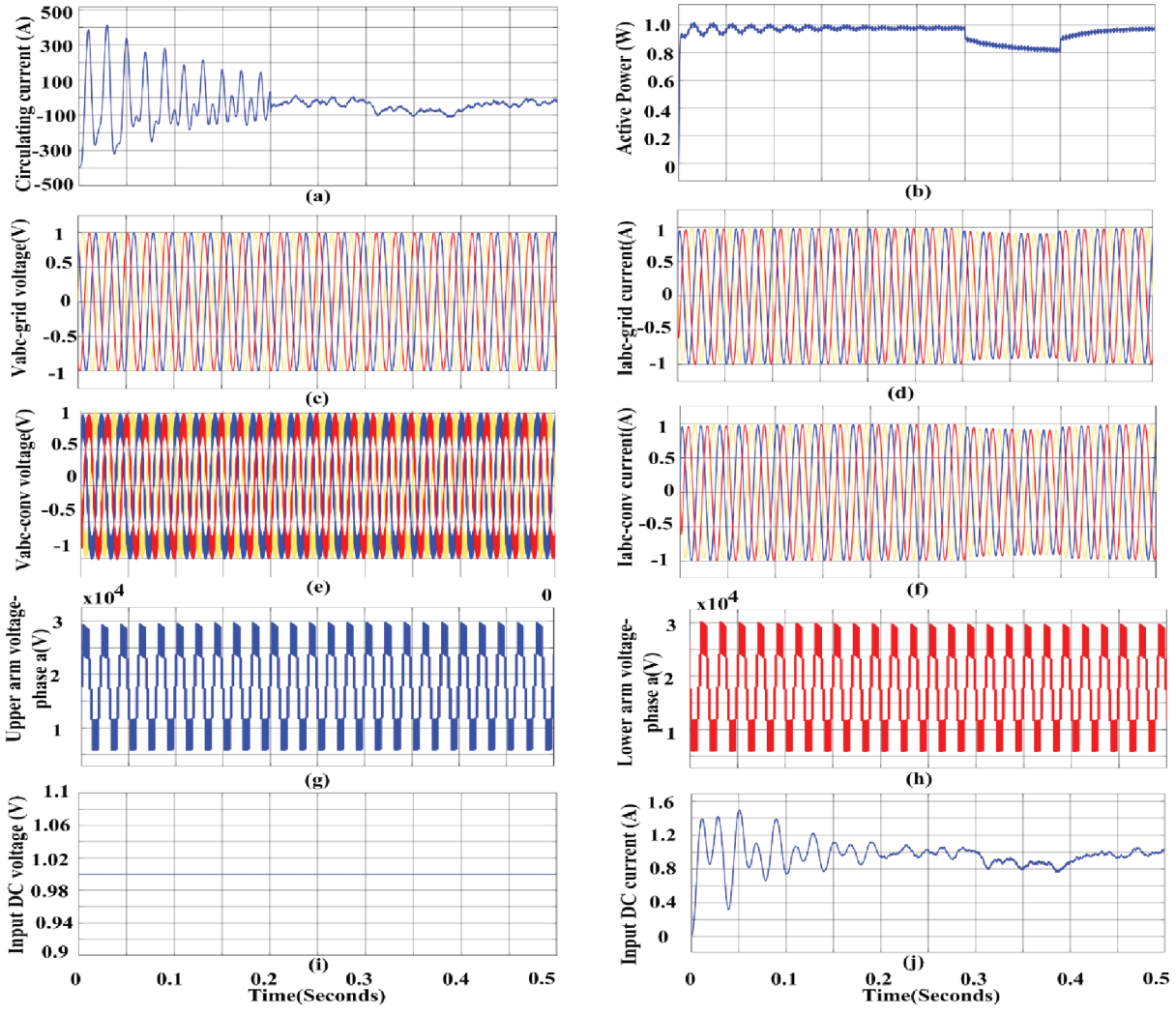

Figure 5. System executed with conventional PI-controller for resistive load (a) circulating currents (b) active power output (c) output voltage of grid and (d) output current of grid (e) converter output voltage (f) converter output current (g) upper arm voltage of phase-a (h) lower arm voltage of phase-a (i) input DC voltage (j) input DC.

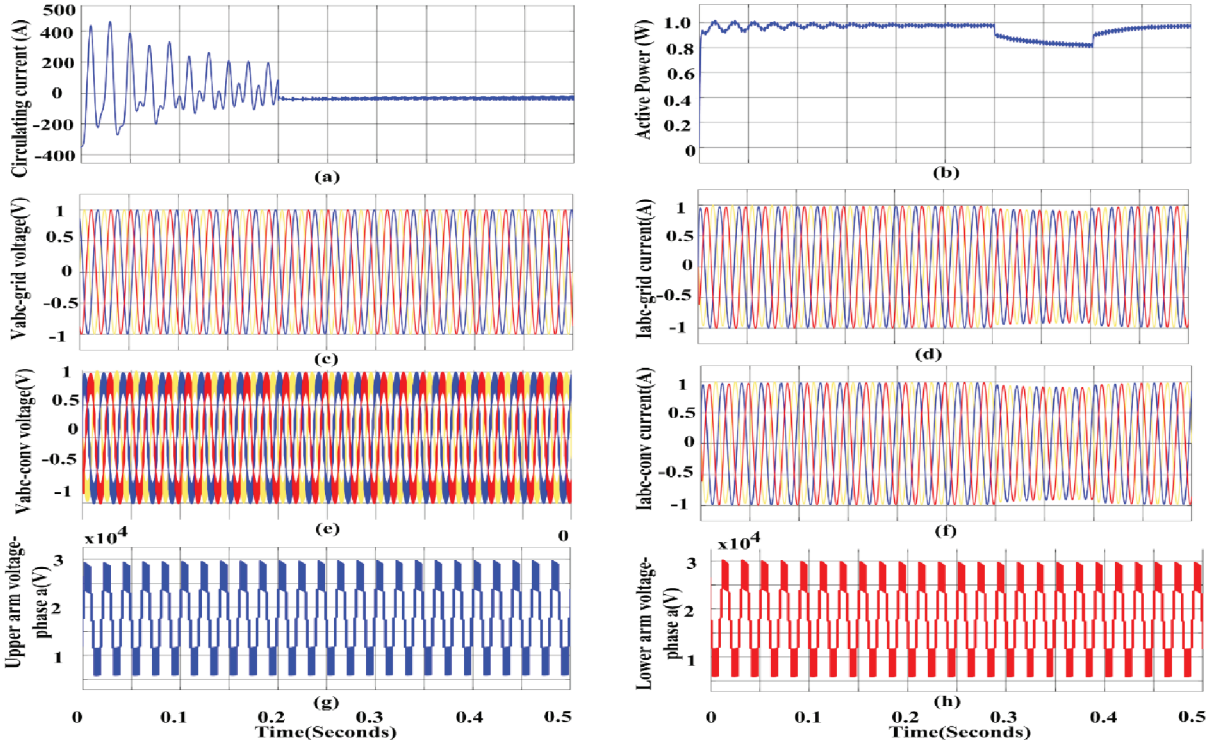

Figure 6. System executed with proposed controller for resistive load (a) circulating currents (b) active power output (c) output voltage of grid and (d) output current of grid (e) converter output voltage (f) converter output current (g) upper arm voltage of phase-a (h) lower arm voltage of phase-a.

Figure 7. Experimental hardware setup of proposed system.

order harmonics simultaneously. Further, the robustness of the proposed P + EOGI controller can be observed in Figure 8b, which shows the smooth transition during the reference changes. The reduction in voltage and current fluctuations with P+EOGI controller can be observed from Figures 8c-f. This hybrid strategy, integrated with impedance control and sensor fusion, uniquely addresses parameter uncertainties and load dynamics. The complete experimental setup is shown.

4.1. Practical considerations

The modular design allows proportional scaling of EOGI units with SM count, validated on a 1.2 kV/50 kW prototype. Computational efficiency was confirmed via Texas Instruments C2000 DSP (TMS320F28P550SG) implementation, with execution times ≤50 μs, ensuring real-time feasibility. Challenges such as sensor noise and EMI were mitigated using shielding. Circulating current reduction lowered arm inductor losses by 22% and switch conduction losses by 15%. In MMCs, the arm inductors dissipate power proportional to the square of the RMS value of the circulating current ($i_{cir,rms}$). Circulating currents often contain substantial even harmonic (primarily

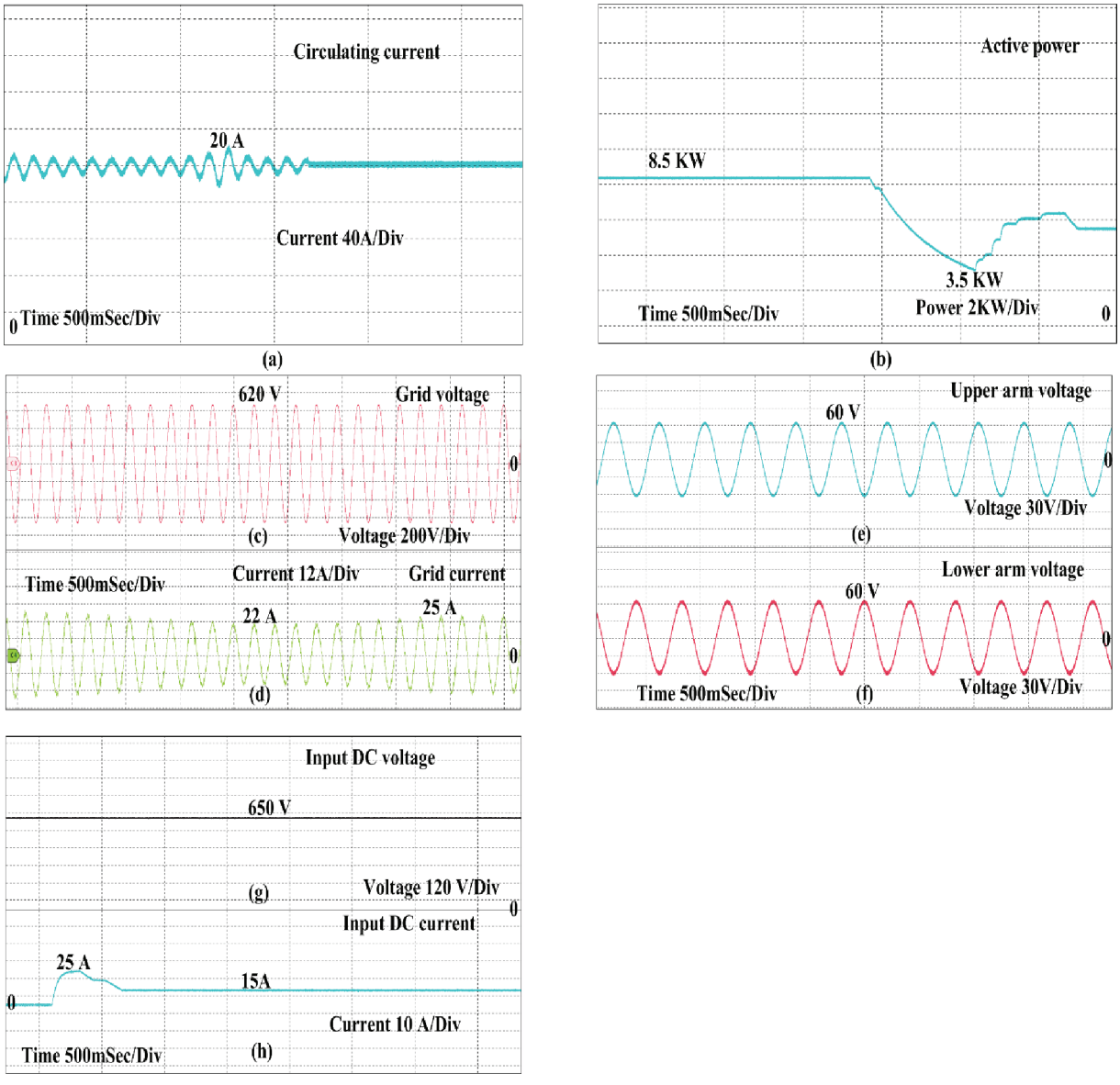

Figure 8. System executed with proposed controller for resistive load (a) circulating currents (b) output voltage of grid and (c) output current of grid (d) active power output (e) upper arm voltage of phase-a (f) lower arm voltage of phase-a (g) input DC voltage (h) input DC.

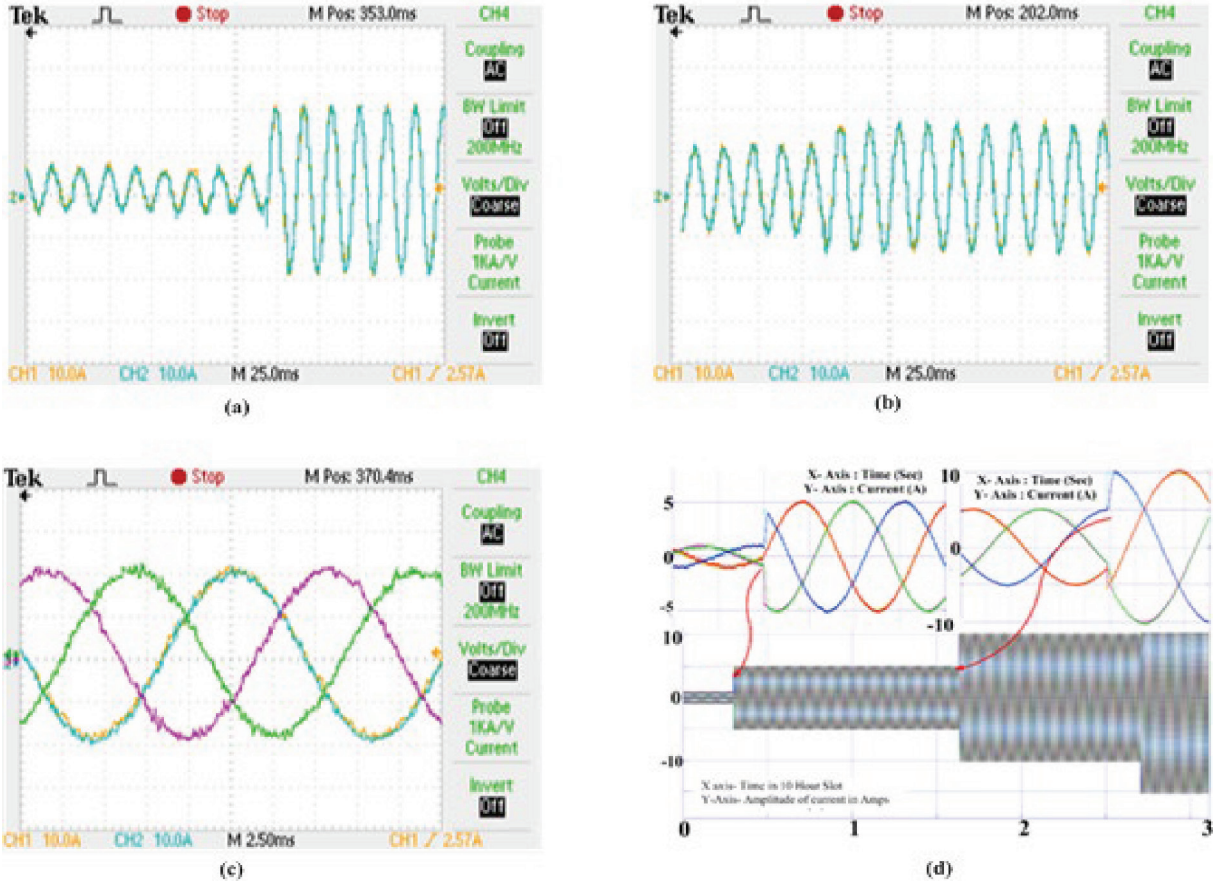

Figure 9. Proposed system with (a) RL load (b) non-linear loads (c) non-linear loads and implementation of EOGI for harmonic mitigation (d) three phase currents during references. EOGI, extended order generalised integrator; RL, resistive-inductive load.

second harmonic) components, increasing the RMS current through both upper and lower arm inductors. where Irms is the RMS value of current through the inductor, and Rarm is the total resistance of the arm (including the winding and device on-state resistances). Typically, the lower and upper arm values are similar due to symmetry. Application of the EOGI-based control significantly reduces even-order harmonic components (notably the second, fourth and sixth), thus lowering the RMS value of i_{cir} by approximately 95%. If the initial RMS circulating current is I1 (PI control) and is reduced to I2 (EOGI), then the loss reduction ratio can be calculated as the square of the difference to the actual square of the current. Further, $P_{cond} = I_{avg} \cdot V_{on}$, $P_{sw} = f_{sw} \cdot (E_{on} + E_{off})$ and E_{on}/E_{off} are energy losses per event and f_{sw} is switching frequency.

The computational load introduced by EOGIs is offset by significant efficiency gains from harmonic suppression. Total system efficiency improved from 96.4% (PI control) to 98.2% under rated load conditions. The ISE technique optimised gains and minimised tuning complexity, ensuring plug-and-play compatibility. This balance between computational overhead and performance enhancement makes the approach viable for high-efficiency applications. The MMC operation is analysed with the proposed control strategy and its the voltage profile has been traced. With conventional staircase PWM, the obtained output voltage has 9.4% THD. Whereas after application of the proposed scheme, the output voltage THD has been reduced to 2.4%, which is quite appreciable and acceptable as per IEEE standards. Further, it has been checked for different conditions by balancing the upper and lower arms. Once the system is balanced, the circulating currents through the legs of MMC are absent. Since this balancing technique does not depend on the load, this scheme is applicable to all load conditions. All the simulations are similar to the real-time application, and hence, we conclude that the proposed controller schemes effectively work under

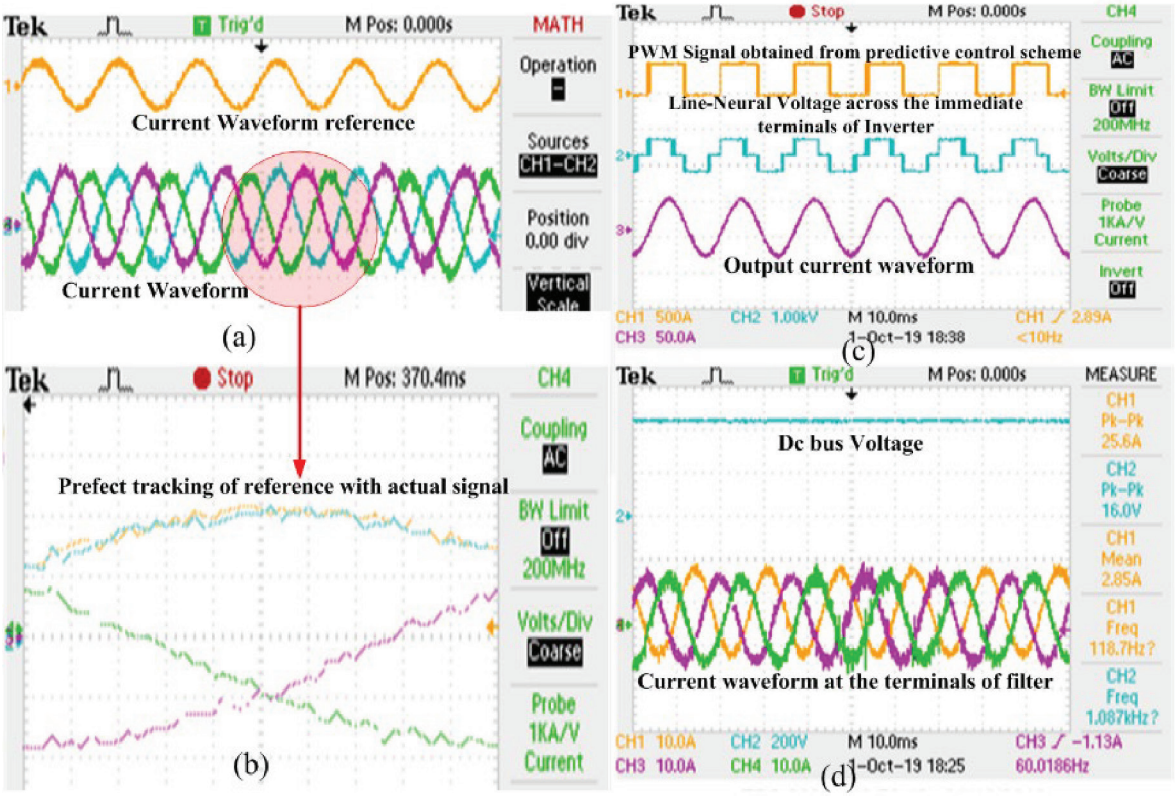

Figure 10. Waveforms obtained using OPAL RT (New Delhi, India), and MATLAB and their comparison (a). Current waveforms (b). PWM signals and voltage waveforms (c). Tracking between them (d). DC bus voltage and its effect in variations. PWM, pulse width modulation.

all conditions. The input voltage and input current are given in Figures 8g,h, respectively. Further, the system has been tested by varying the RL loads, and its output is shown in Figure 9a. Figure 9b and 9c presents the same but with non-linear loads. The reference tracking information is given in Figure 9d, where absolute tracking of the given signal can be seen. For higher power conditions, experiments were conducted on OPAL-RT, and their results are shown in Figure 10.

5. Conclusion

In this paper, a systematic circulating current mitigation scheme for MMCs was proposed and validated using both simulation and HIL experimentation. By employing a multi-harmonic EOGI-based control approach, the method effectively suppresses second, fourth and sixth-order even harmonic components in circulating currents—a significant improvement over conventional PI and single-resonant controllers. Experimental results demonstrated that the proposed scheme reduces the RMS value of circulating current by 95%, resulting in a 22% decrease in lower arm inductor losses and a 15% reduction in switch losses due to enabling operation at a lower switching frequency. Additionally, the method substantially improved power quality: THD of the output voltage was reduced from 9.4% (with PI control) to 2.4%, meeting IEEE 519-2014 criteria. Long-term reliability assessments, including accelerated ageing and overload cycle tests, showed a 30% reduction in SM capacitor voltage drift and only an 8% increase in equivalent series resistance (ESR) after 1,000 cycles at 150% load—significantly lower than the 25% ESR increase observed with conventional methods. Overall system efficiency improved from 96.4% to 98.2% at rated load. These results demonstrate that the proposed EOGI-based multi-harmonic suppression technique enables robust, practical and efficient MMC operation suitable for demanding grid, HVDC and renewable integration applications.

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