sciendo

Power Electronics and Drives
Volume 7(42), 2022 DOI: 10.2478/pead-2022-0016

Power Electronics and Drives

# Modified Topology and Modulation Technique for Z-Source Neutral-Point Clamped Inverter

**Research paper**

Ehsan Akbari[1], Farhad Zishan[2,*]

[1]Department of Electrical Engineering, Mazandaran University of Science and Technology, Babol, Iran
[2]Department of Electrical Engineering, Sahand University of Technology, Tabriz, Iran

**Received: August 12, 2022; Accepted: September 29, 2022**

**Abstract:** The impedance network makes it possible to increase and decrease the voltage, which is not available in normal inverters (voltage and current sources).This paper presents a modified topology and modulation technique for a three-phase Modified Z-Source Neutral-Point Clamped (MZS-NPC) inverter. A modulation scheme for the proposed topology is designed based on maximum gain control method to achieve the maximum voltage gain by simple implementation and balancing the neutral point voltage of the dc link. In order to supply the desired voltage to the critical load in an islanded micro-grid, a closed-loop ac voltage controller is realized in fuel cell or photovoltaic applications based on the proposed inverter. The ability to reinforce and validity of topology operations and modulation techniques has been demonstrated by simulation. It should be noted that the simulations are implemented in MATLAB / Simulink software.

**Keywords:** *Modulation • Optimization • Multilevel inverter • MZS-NPC*

## 1. Introduction

Electronic power converters are widely used in industrial power conversion systems for electrical industry applications and drives. Different countries choose different standards for operating voltage in different applications, but high voltage for high power is a general principle observed everywhere. Therefore, with increasing power levels, the voltage level increases accordingly to reach a satisfactory efficiency (Sayed et al., 2022). Today, extensive efforts have been made to increase the nominal value of semiconductor switches following the increase in the use of electronic power technology. Of course, as the nominal value of the keys increases, their performance decreases a lot in terms of speed and maximum switching frequency, quality, etc. Over the years, the nominal voltage of high-voltage semiconductors with high switching speeds has increased, such as bipolar transistors with isolated gates. Despite many advances in semiconductor physics, existing switches still do not meet the needs of the electrical industry, and series and parallel connection of semiconductor switches is inevitably used. Series and parallel connection of switches to increase the amount of current and voltage tolerable by the switches are not a very simple and reliable solution. For example, when connecting a series of power switches, different time delays in turning on the semiconductor switch or small leakage currents with very different values in the same switches may cause the switches to be damaged. Of course, the conditions in the parallel connection of the keys are much better and safer than their series connection. Due to the above, the use of multi-level inverters (Vemuganti et al., 2021) is one of the available solutions for high voltage applications. The idea of multilevel inverters was introduced in 1975 (Dharmambal and Nisha, 2022). The global increase in energy demand and the increasing level of voltage and power in the industry have led to the emergence of multi-level inverter structures and semiconductor technology to meet the needs of power. Multi-level inverters are widely used in medium voltage and high power applications due to their ability to operate in the power range of several megawatts and several kilowatts of voltage. A variety

* Email: f_zishan99@sut.ac.ir

of multilevel inverter structures have been introduced over the past two decades. Three important and significant structures of these structures are related to cascading multi-level inverters (Gong et al., 2022), diode damped (Korde et al., 2022; Rath et al., 2021) and flying capacitor (Jayakumar et al., 2021; Khan et al., 2022). Unlike cascading multi-level inverters, power can be saved by reducing the number of DC power sources, which can be achieved by using multi-level diode clipper inverters. In the structure of multi-level Z-NPC inverters (Akbari et al., 2021), instead of using a voltage source and DC link capacitors, impedance source networks with the same or different input voltages can be used. This structure makes it possible to control the output voltages of impedance sources networks both jointly and separately. There are different structures for multilevel inverters for different applications. Typically, multi-level inverters are used depending on the direct current source of the isolator or isolating capacitors that are used as a direct current source to combine the step output voltage (Husev and Carlos, 2021). The first type is very reliable but requires more DC sources and more power switches, such as the H bridge multilevel inverter. The structure of Neutral Point Clipper (NPC) multilevel inverters was first introduced in 1980 (Rodriguez et al., 2002). The advantages of diode-damped multi-level inverters include (Balal et al., 2022)the following:

- Many improvements in reducing voltage changes over time as well as switch stresses.
- All phases share a common DC bus to minimise the capacitor required by the converter.
- This structure has a good variety for single-phase and three-phase inverters.

However, the experimental results for this structure also indicate several technical problems, which in turn make its application more difficult and complex for high-power converters. Some of these problems are as follows (Do et al., 2019):

- This structure requires ‘high-speed clipper diodes’ that must be able to carry the entire load current, as well as factors that exacerbate ‘reverse recovery stress’. Although steps can be taken to reduce this problem, it is still a problem.
- The problem of capacitor charge balance is still a debatable subject for NPC structures with more than three levels. NPC structures with levels of more than three are also subjected to increase voltage stress as a relation. Therefore, a series connection of diodes may be required.
- The number of clipper diodes depends on the number of inverter levels, so these design complexities increase cost and reliability concerns.

The structure of three-level NPC inverters with high power factor loads works well, and the structure of NPC inverters with more than three levels is often used for static reactive power compensation circuits. This may be related to the capacitor equilibrium problem. In the NPC inverter structure, the use of NTV4 modulation is preferred over other methods because it has a modulation scheme with minimal stress and excellent spectral performance (Barbosa et al., 2005). In Rodriguez et al. (2009), the NPC inverter is fully introduced and this inverter is mentioned as the most widely used type in high power. At the beginning of this paper, the working method of this type of inverter has been introduced and then the various methods available for control and modulation of these inverters have been introduced that include pulse width modulation, space vector modulation and load-based modulation. This paper also uses a new structure to balance semiconductor losses. In Sapin et al. (2007), a three-level NPC inverter with an output filter is used to supply the induction motor. Motor torque is used directly to control the inverter. It is also used to balance the voltage with the control method and compare the voltage on each of the capacitors and apply feedback to the output to control it. In Rivera et al. (2014), the predictive method has been used to control the current of the three-level NPC inverter. To implement the control system, the capacitors voltage and load current in the 27 switching modes must be predicted by the relations in the paper. After predicting the parameters, the cost function should be formed using these parameters and among all switching modes, the mode with the lowest voltage difference on the capacitors should be selected as the optimal mode with the least change of mode. In Sheir et al. (2018), a new structure is introduced for NPC converters with an additional circuit to control the voltage of the capacitors, which is used in charging stations for electric vehicles.

In this paper, the limitations of voltage control of capacitors using existing methods are discussed in the first step, and then an additional circuit is used to provide minimum load conditions for the modulator to ensure the voltage balance of the capacitors, in addition to the available methods. Using this circuit, different loads will be within the allowable range for the converter, and imbalance caused by getting out of range will not occur due to an

additional parallel branch in the circuit. In Sankar and Babu (2020), a new structure of two-way multilevel inverters is presented. The proposed structure uses a DC–DC converter connected to the DC link, which is responsible for voltage balancing. This type of converter produces more voltage levels at the output. In this structure, the efficiency of the system is considerably high, which is about 90% of the simulation results. Also, the voltage ripple and its associated stress are greatly reduced. In Brueske et al. (2014), the expanded structure of the three-level Z-NPC inverter is presented. Due to the unique features of impedance source converters and using the conventional impedance source inverter and Z-H converter, the basic structure of a Z-H Buck-Boost converter is provided. Compared to the conventional Z-H converter, the proposed Z-H converter has increasing and decreasing capability in addition to removing the ST mode and pre-LC diode. Some prominent advantages of the proposed Z-H converter include simplicity of structure, increasing and decreasing capability, and having low ripple voltage and current waveforms, thus eliminating the need for additional filters in the circuit. In Strzelecki (2006), a three-level Z-NPC inverter is presented, which has a structure similar to that used in this article, but the modulation method in this article is a simple PWM type and optimisation has not been done.

This paper proposes a Modified Z-Source Neutral-Point Clamped (MZS-NPC) inverter designed by integrating a modified Z-source impedance network, applied to a cascading five-level hybrid inverter. The proposed MZS-NPC inverter can increase the boost factor and produce an amplified five-level output voltage. A modified modulation technique based on the maximum reinforcement control strategy is proposed to achieve the maximum voltage gain and the possibility of simple execution, which can balance the neutral point voltage of the DC link to achieve the zero-neutral point mean current conditions. The performance of the proposed topology and modulation technique is confirmed based on the simulation results. Introduction and structure of the paper were presented in the first section. The MZS-NPC three-level inverter is introduced and described in the second section; in the third section, the details of the proposed method and improved modulation are presented, and then in the fourth section, the simulation results are analysed and finally, a general conclusion is presented in the last section.

# 2. Z-source Three-Level NPC Inverter

## 2.1. MZS-NPC three-level inverter structure

Figure 1 shows the topography of a three-phase three-level MZS-NPC inverter Strzelecki (2006).

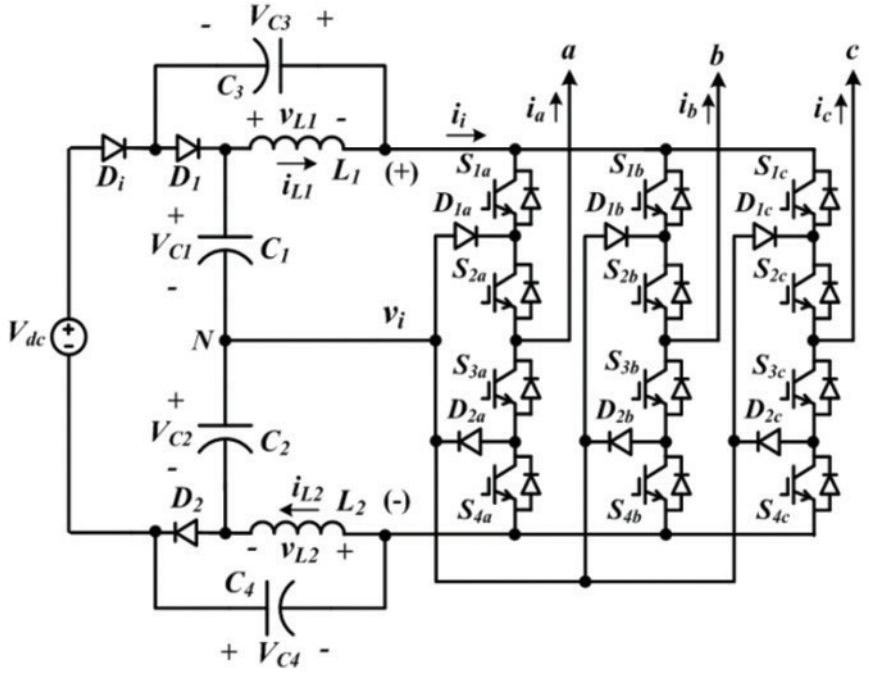


**Fig. 1.** Modified three-phase impedance source NPC inverter Strzelecki (2006). NPC, neutral point clipper.

This converter is similar to the traditional impedance source converter with two Shoot-Through State and non-Shoot-Through State modes. Due to the symmetry of sizes L1 and L2, the values of $C_1$ and $C_2$ as well as $C_3$ and $C_4$ are considered equal. In the following, the equations related to the converter model are presented in two states.

## 2.2. How MZS-NPC three-level inverter works

### *A. Shoot-Through State*

In this converter, the shoot-through state consists of three parts: full shoot-through, upper shoot-through ($t_{ust}$) and lower shoot-through ($t_{lst}$). In full shoot-through, all switches turn on during the $t_{ust}$ time, resulting in a zero output voltage. As a result, the upper and lower shoot-throughs produce higher quality AC voltage and fewer switches. In the upper shoot-through state, switches {$S_{1x}$, $S_{2x}$, and $S_{3x}$}, diodes {$D_i$, $D_2$, and $D_{2x}$} turn on, and diode D1 is off. In this case, the voltage relationship between the inductors and the DC link is expressed as relations 1 and 2 (Strzelecki, 2006).

$$\begin{aligned} v_{l1} &= V_{C1} + V_{C2} - V_{dC} - V_{C1} \\ v_{L2} &= -V_{C4} \end{aligned} \tag{1}$$

$$v_i = V_{C2} + V_{C4} \tag{2}$$

In the lower shoot-through state, switches {$S_{2x}$, $S_{3x}$, $S_{4x}$} and diodes {$D_i$, $D_1$, and $D_{1x}$} are directing and diode $D_2$ is off. In this case, the voltage relationship between the inductors and the DC link is expressed as follows.

$$\begin{aligned} v_{L1} &= V_{C1} - V_{C3} \\ v_{L2} &= V_{C2} = V_{C1} + V_{C2} - V_{dc} - V_{C4} \end{aligned} \tag{3}$$

$$v_i = V_{C1} + V_{C3} \tag{4}$$

The equivalent converter circuit in the upper and lower shoot-through is shown in Figure 2.

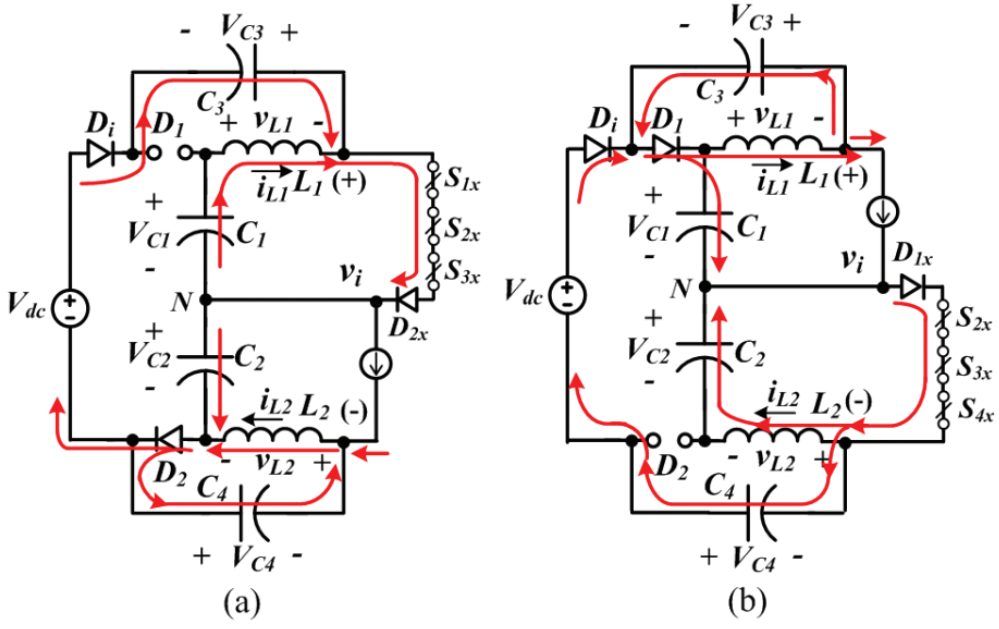


**Fig. 2.** Converter equivalent circuit in (a) upper shoot-through state and (b) lower shoot-through state.

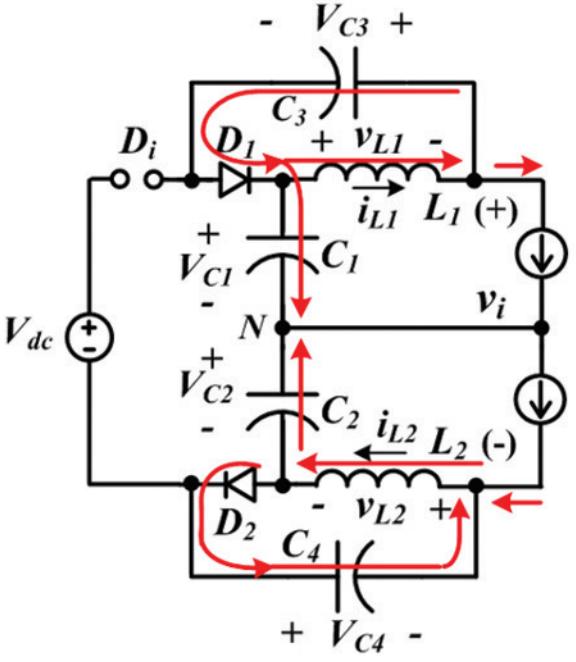


**Fig. 3.** Converter equivalent circuit in the non-shoot through state.

### *B. Non-Shoot-Through State*

In this state, time $t_{lst}$ and diodes $D_1$, $D_2$ are directing and diode $D_i$ is off. In this case, the relationship between inductors voltage and DC link voltage is calculated as follows (Strzelecki, 2006):

$$\begin{aligned} v_{l1} &= -V_{C3} \\ v_{L2} &= -V_{C4} \end{aligned} \tag{5}$$

$$v_i = V_{C1} + V_{C2} + V_{dc} + V_{C4} = \hat{v}_i \tag{6}$$

The converter equivalent circuit in the non-shoot through state is shown in Figure 3.

### *C. Boost coefficient*

The mean values of $t_{ust}$ and $t_{lst}$ are the same during the one-third time constant due to the symmetry of the lower and upper shoot-through performance and non-shoot-through, so $t_{ust} = t_{lst} = t_{st}$. Accordingly, the average voltage of the two ends of L1 by the relations (1), (3) and (5) during a period is zero, and also considering that $V_{c1} = V_{c2}$ and $V_{c3} = V_{c4}$, the capacitor voltage is equal to Strzelecki (2006):

$$V_{C1} = V_{C2} = \frac{1-D}{1-2D} * V_{dc} \tag{7}$$

$$V_{C3} = V_{C4} = \frac{D}{1-2D} * V_i \tag{8}$$

Where $D$ is the Duty cycle. By substituting relations 7 and 8 into 6 relations, the coefficient of increase ($B$) is obtained as follows (Strzelecki, 2006):

$$B = \frac{\hat{v}_i}{v_{dc}} = \frac{2}{1-2D} \tag{9}$$

# 3. Modified Modulation for MZS-NPC Three-Level Inverter

## 3.1. Modified modulation technique performance for MZS-NPC three-level inverter

Figure 4 shows the performance of the proposed modified modulation technique. The modified technique has two triangular waves with a phase difference of 180 degrees called $V_{tr1}$ and $V_{tr2}$. In this case, the voltage gain ($G$) is as follows:

$$G = \frac{\hat{v}_O}{v_{dc/2}} = B.M \tag{10}$$

In the above relation, $V_o$ is the peak voltage of the output phase and M is the modulation coefficient. The relationship between M and B depends on the modulation method. In this paper, the maximum boost control method is used for the proposed topology to obtain the maximum voltage gain. The maximum boost control method changes all zero modes to shoot-through state without changing the active modes. Using the sinusoidal reference voltage with the third harmonic voltage $V_x$-ref, which is x = a, b, c, the three-phase positive and negative modulation signals $V_{xp}$ and $V_{xn}$ are equal to Strzelecki (2006):

$$V_{xp} = \frac{1}{2}\left(\left|V_{x-ref}\right| + V_{x-ref}\right) \tag{11}$$

$$V_{xp} = \frac{1}{2}\left(\left|V_{x-ref}\right| - V_{x-ref}\right) \tag{12}$$

That x = a, b, c have a phase difference of 120 degrees with each other. Figure 4 shows the logic circuit of the modified modulation strategy. PWM signals called $S_{1x}/S_{3x}$ are generated by comparing the positive modulation

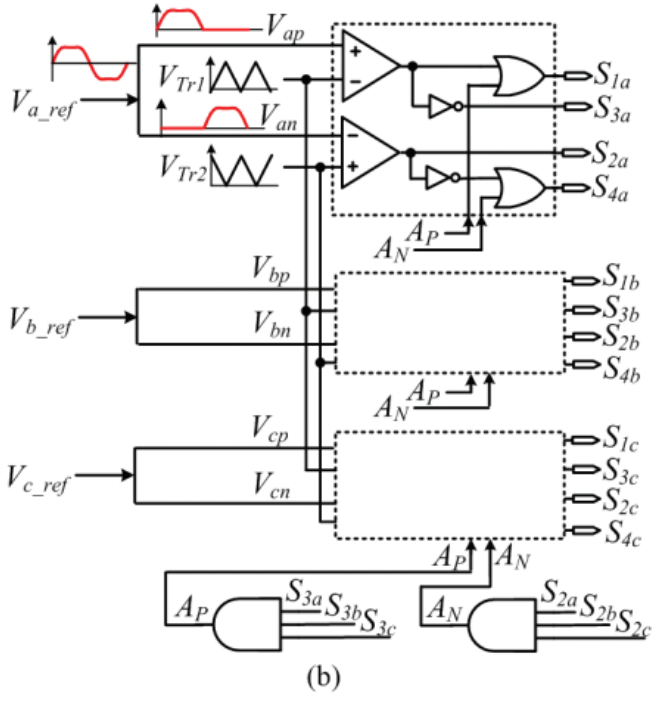


**Fig. 4.** Modified modulation strategy logic circuit for three-level MZS-NPC inverter (Strzelecki, 2006). MZS-NPC, modified Z-source neutral-point clamped.

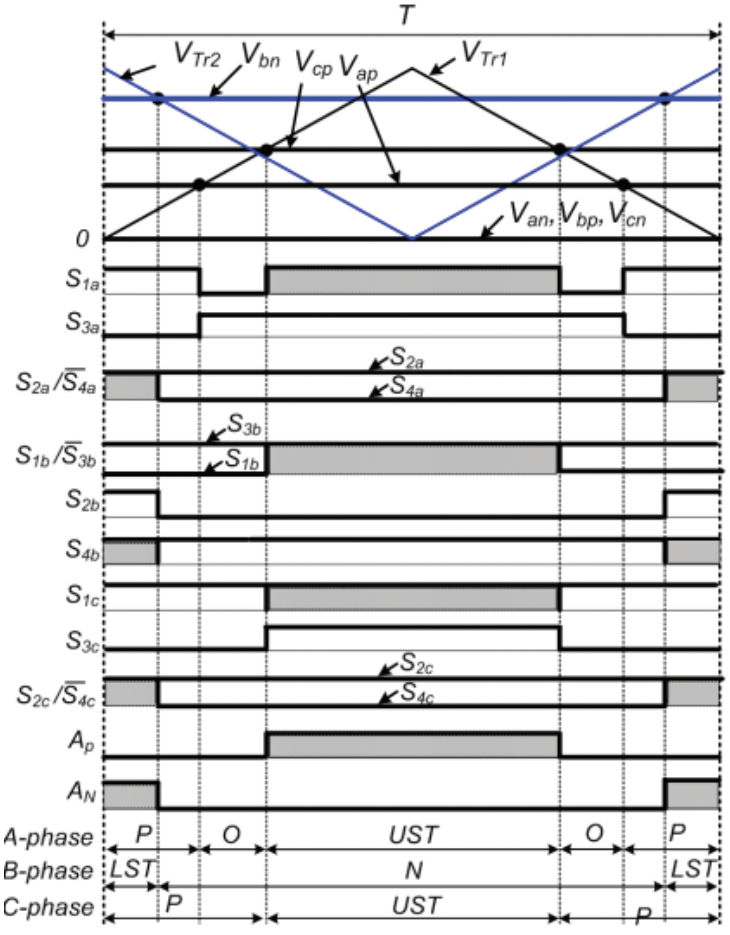


**Fig. 5.** Switching pattern.

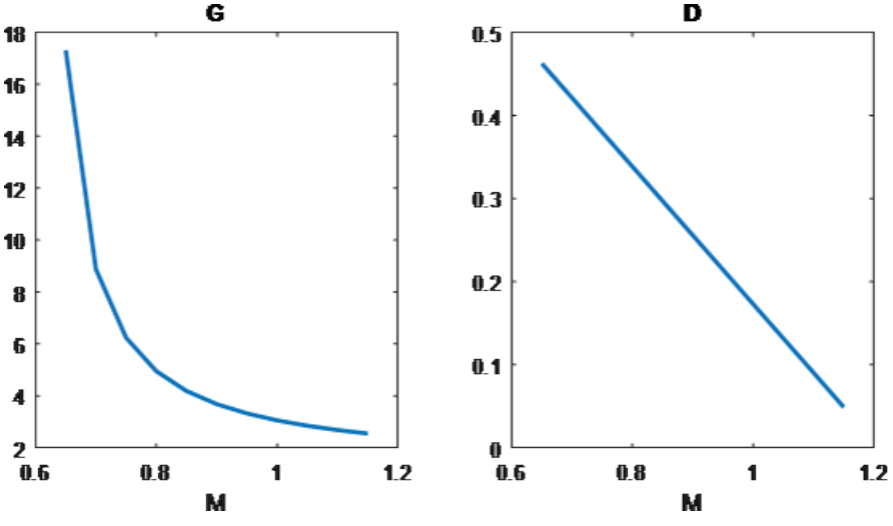


**Fig. 6.** Shoot-through state waveforms in terms of diode cycle and voltage gain with M changes.

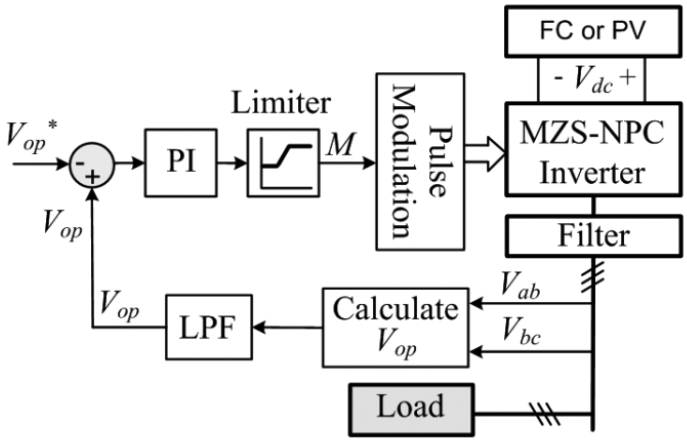


**Fig. 7.** Recommended closed loop control diagram of AC load voltage for MZS-NPC. MZS-NPC, modified Z-source neutral-point clamped.

**Table 1.** Values of simulation parameters (Strzelecki, 2006).

| Parameter | Value |
|---|---|
| Impedance source converter | |
| $L_2 = L_1$ | 1 μH (millihenry) |
| $C_1 = C_2 = C_3 = C_4$ | 1,000 μF (micro farad) |
| Output filter | |
| $L_f$ | 0.6 mH |
| $C_f$ | 100 μF |
| RL load | |
| $R_L$ | 50 Ω |
| $L_L$ | 1.2 mH |

signal $V_{xp}$ with the carrier signal $V_{tr1}$. The $S_{1x}$ switch turns on when the positive modulation signal is larger than the carrier signal $V_{tr1}$. $P_{wm}$ signals called $S_{2x}/S_{4x}$ are generated by comparing the negative modulation signal $V_{xn}$ with the carrier signal $V_{tr2}$. The $S_{2x}$ switch turns on when the negative modulation signal is larger than the carrier signal $V_{tr2}$. Upper and lower shoot-through states are also generated with $A_p$ and $A_n$ signals. All zero states are converted to upper and lower states to obtain the maximum voltage gain. The upper shoot-through state is achieved by the $A_p$ signal when all switches $S_{3a}$, $S_{3b}$, $S_{3c}$ are on, and the lower hoot-through state is achieved by the $A_n$ signal when the switches $S_{2a}$, $S_{2b}$, $S_{2c}$ are all on. Figure 5 shows the switching pattern of three-phase PWM signals in this method.

Because the diode cycle of the short- through state changes with the inverter frequency, the average period of shoot-through state during $((\pi/6)(\pi/2))$ is as follows:

$$\bar{D} = 1 - \frac{3\sqrt{3}}{2\pi} * M \tag{13}$$

By substituting relations 7 and 11 into 8 relations, the voltage gain $G$ (a function of $M$) is obtained as follows:

$$G = \frac{2}{\frac{3\sqrt{3}}{\pi} - \frac{1}{M}} \tag{14}$$

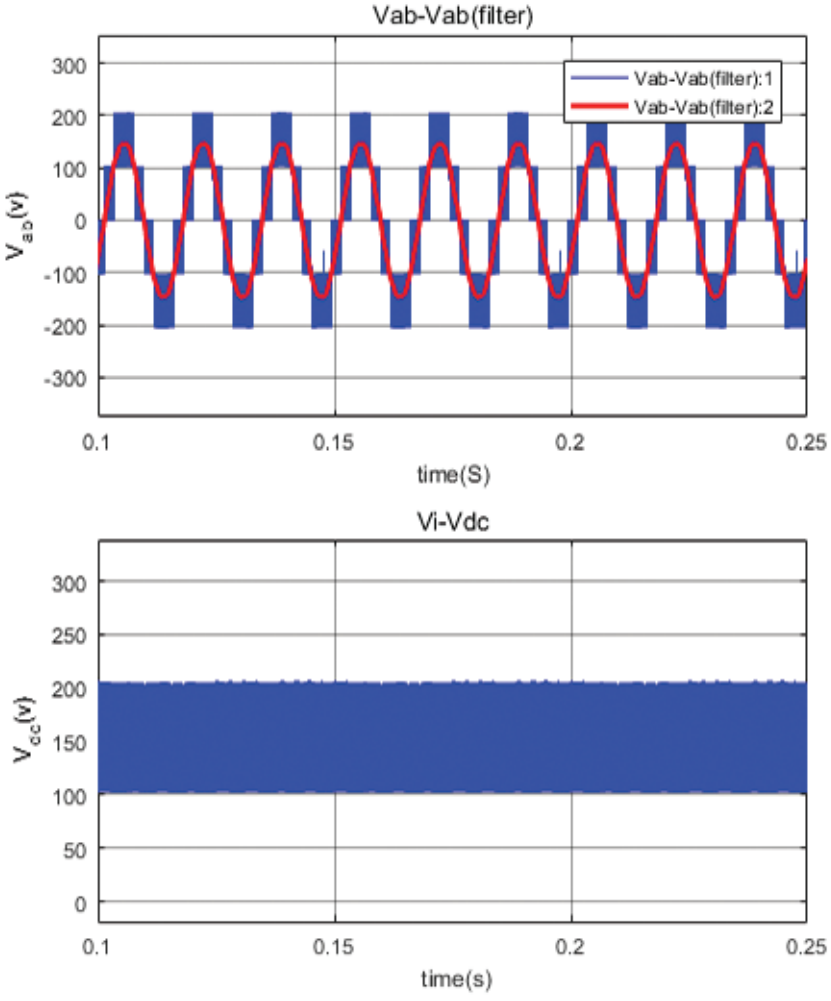


**Fig. 8.** Output voltage waveform and DC link voltage at $M = 0.8$.

In Figure 6, the graphs *D* and *G* in terms of *M* are drawn with the help of relations 14 and 15. According to this figure, it is clear that the value of *M* increases in the range of 0.65 to 1.15 with decreasing *D* and *G*. When M reaches its maximum value of 1.15, the values of *D* and *G* are equal to 0.05 and 2.55, so at the maximum increase factor, the DC link voltage is 2.1 times and the peak AC voltage is 2.55 times.

## 3.2. AC voltage control in islanded operation mode

The proposed closed-loop control of AC load voltage for MZS-NPC is shown in Figure 7. At any moment, the voltage value is compared with the reference value and the output enters the PI controller. The output of the PI controller is connected to the limiter and the M factor and pulse modulation are applied to the MZS-NPC inverter. The output of the inverter creates a DC voltage link that is connected to the micro-grid (Akbari et al., 2022). To improve the output voltage, a filter is used and again this voltage is the reference voltage compared. In fact, this controller is done by a closed loop. In some cases, this voltage can also be used for the load. The reference voltage, which is the peak reference voltage of the network, is 150 V, and the polarity of the reference voltage is selected to reduce the value of *M* when the error is positive. Depending on the relationship between *M* and *G*, the range of changes in *M* is limited to between 0.65 and 1.15. Then the generated pulses are entered into the inverter as a switching

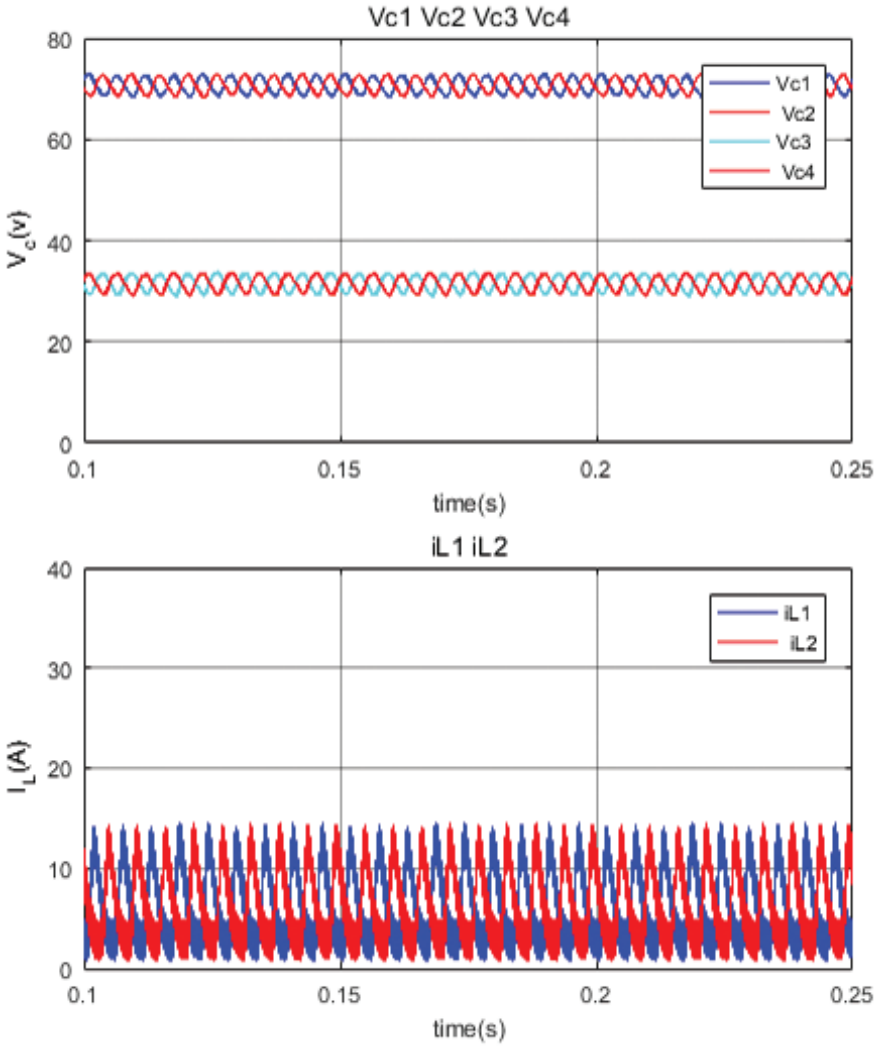


**Fig. 9.** Voltage waveform of capacitors and inductors at $M = 0.8$.

signal, and control is performed. Also be noted that the calculate Vop block performs the calculations according to two relations 9 and 10.

## 3.3. Calculate the amount of distortion and harmonic

Current and voltage distortion usually occur in power systems because current distortion causes voltage distortion in many cases. Assuming a pure sine voltage at the main frequency, the input voltage can be expressed based on the reference abbreviation (Liu et al., 2008) as follows:

$$u_s = \sqrt{2}V_s sinw_1 t \tag{15}$$

The line $i_s$ distorted current is expressed as follows:

$$i_s = i_{s1} + \left(a_{h=2}^{Y} * i_{sh}\right) \tag{16}$$

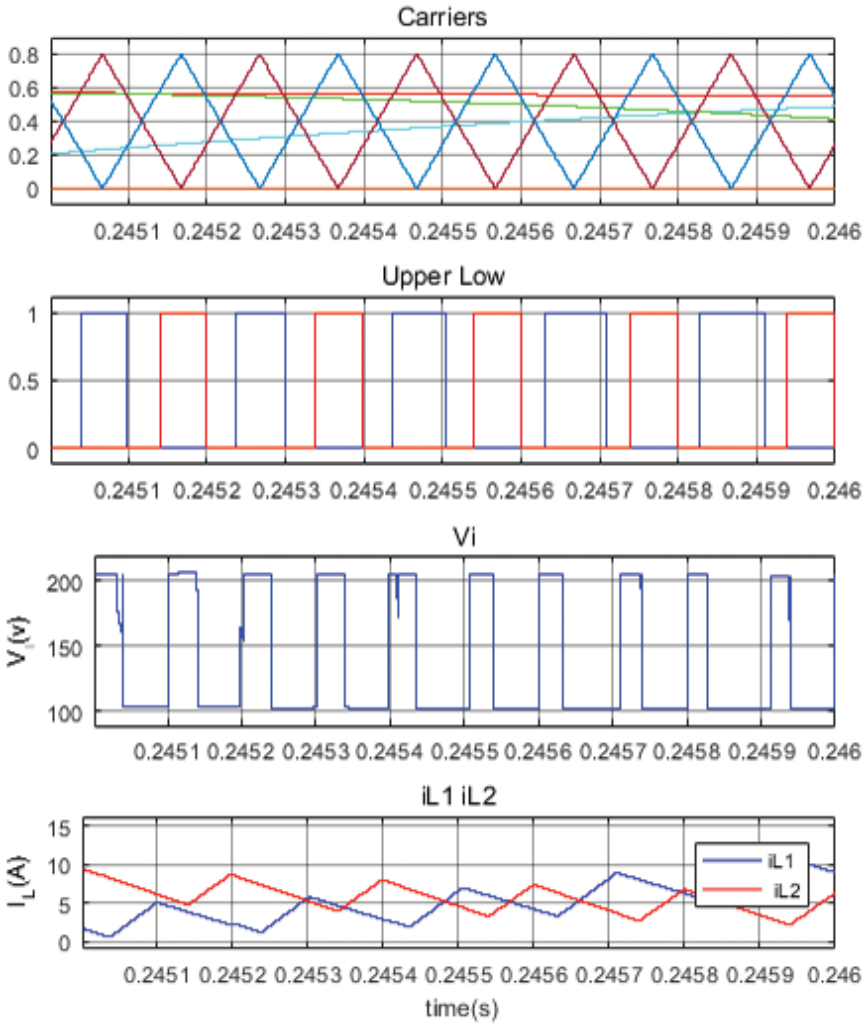


**Fig. 10.** Three-phase modulation signal, upper and lower shoot-through state signal, DC link voltage and inductor current at $M = 0.8$.

$i_s1$ is the main component of the current, $i_{sh}$ is the $h^{th}$ harmonic component of the current. The subtitle h indicates the harmonic order. The above equation can be expressed as follows:

$$i_s = \sqrt{2} I_{s1} \sin\left(w_1 t + \Theta_1\right) + a_{h=2}^{Y} * I_{sh} \sin\left(w_h t + \Theta_h\right) \tag{17}$$

Where $\theta_1$ is the phase angle of the main component of the input voltage and $\theta_h$ is the phase angle of the input voltage at frequency $f_h$.

The distortion component of a current is the sum of its harmonics, which can be written as follows:

$$I_{dis} = \sqrt{I_s^2 - I_{s1}^2} \tag{18}$$

This leads to a distortion index that is commonly used. The name of this index is total harmonic distortion (THD), which is defined as follows (Liu et al., 2008):

$$THD\% = 100 \frac{I_{dis}}{I_{s1}} \tag{19}$$

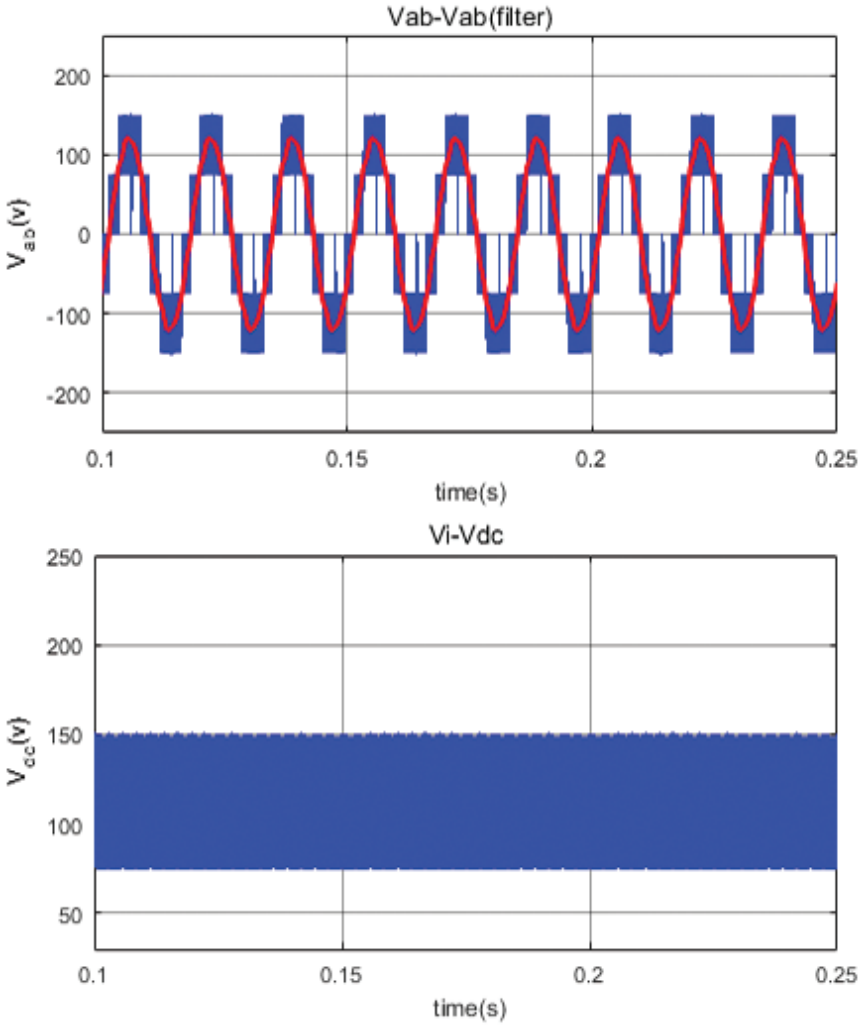


**Fig. 11.** Output voltage waveform, DC link voltage at $M = 0.9$.

The above equation is used to calculate the amount of distortion in the system used in this research.

# 4. Simulation

## 4.1. The structure of the system under study

To examine how the system works using the proposed modulation method, the circuit in Figure 1 is simulated in MATLAB software. In this simulation, the switching frequency and the input DC voltage were considered 5 KHz (kilohertz) and 40 V, respectively. Also, the cut-off frequency of the filter is 650 Hz and the frequency of the output AC signal is 60 Hz. The circuit parameters for the simulation are also given in Table 1.

## 4.2. Simulation results

Figure 8 shows the simulation results for $M = 0.8$. As it can be seen in this figure, the effective value of the 5-level output voltage shown is about 110 V. DC link voltage can be increased up to 245 V, which is 6.1 times the input DC link voltage. Capacitors $C_1$ and $C_2$ have ripples with a frequency of 180 Hz and their amplitude is 79 V. Also, the average voltage of capacitors $C_3$ and $C_4$ is 40 V, which is shown in Figure 9.

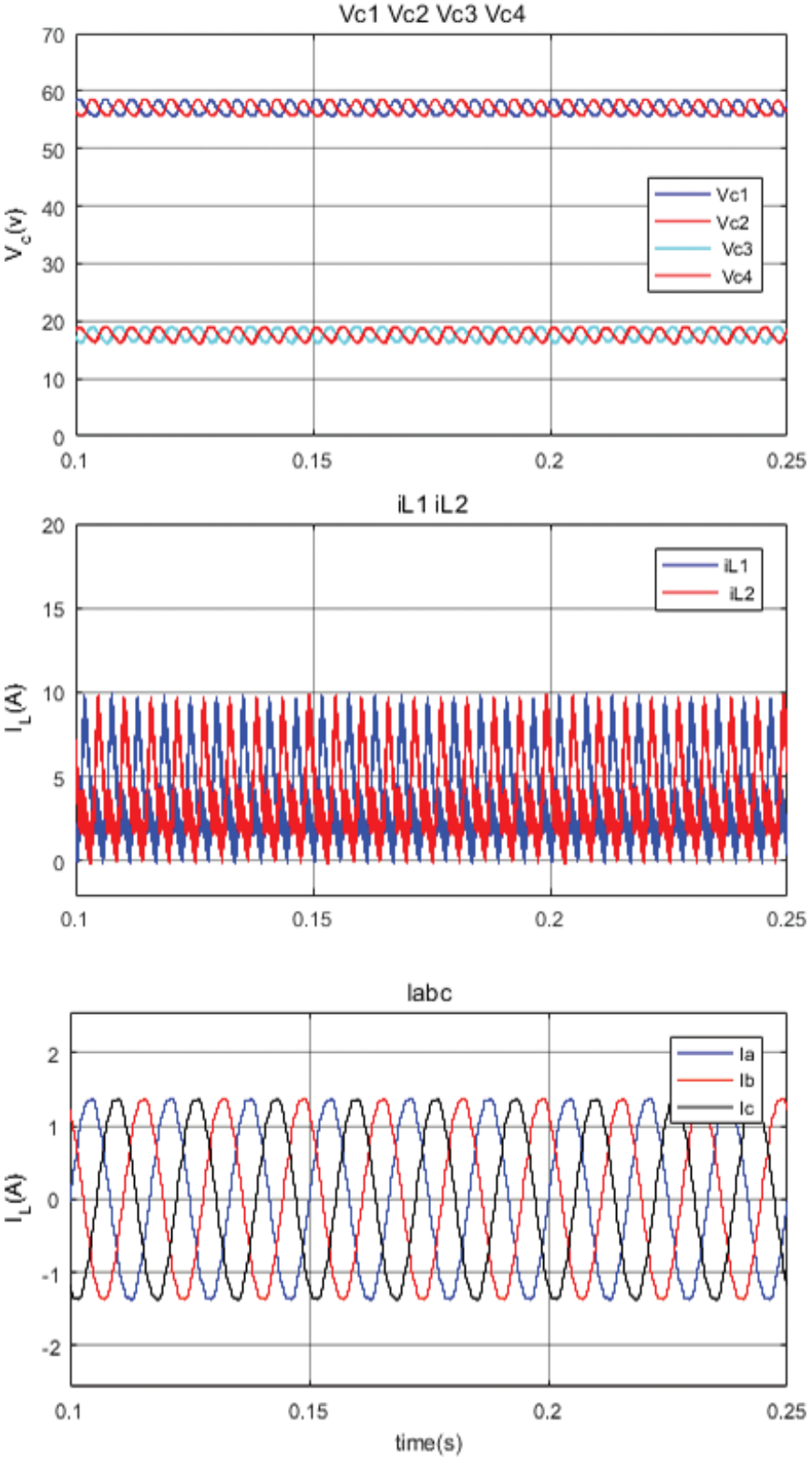


**Fig. 12.** The voltage waveform of capacitors and inductors and load current in $M = 0.9$.

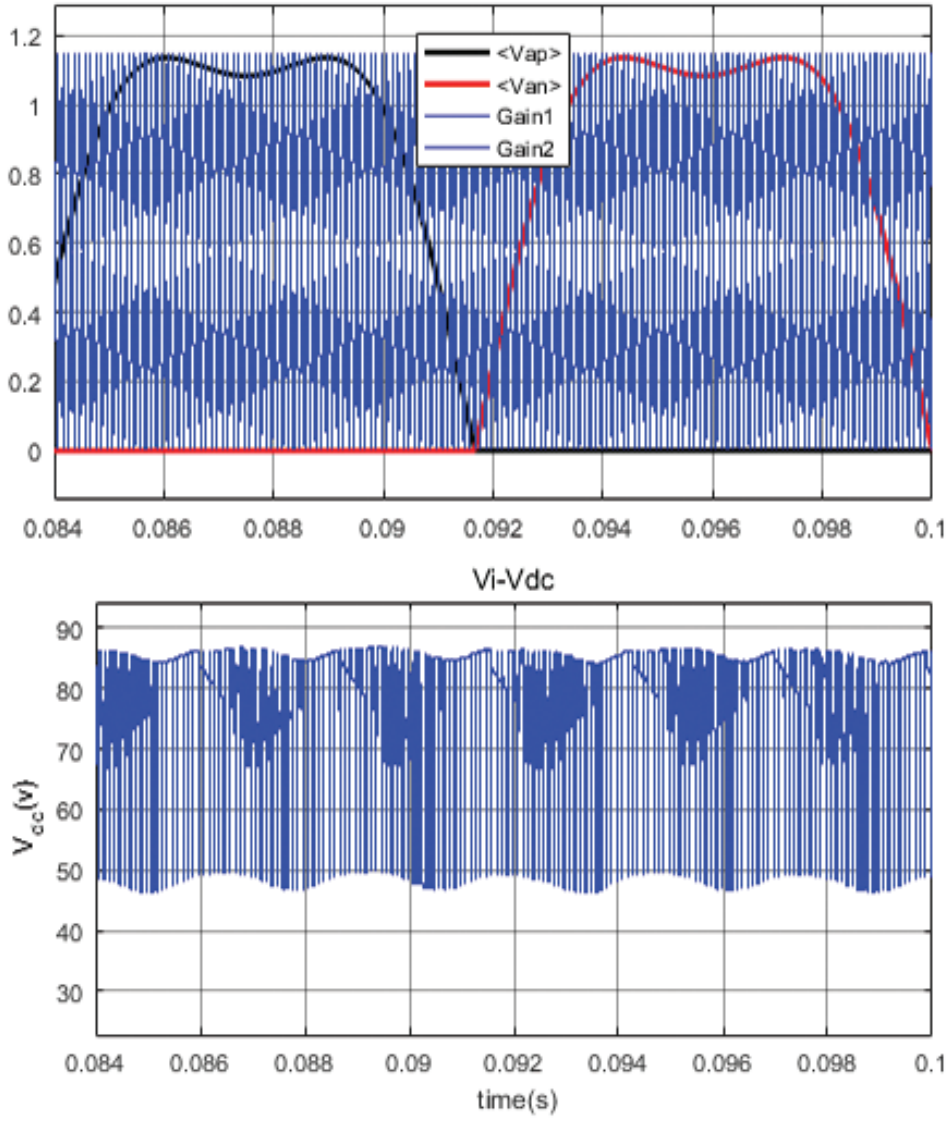


**Fig. 13.** a-phase modulation signal waveform and DC link voltage at $M = 1.15$.

Figure 10 shows the three-phase modulation signal, the upper and lower shoot-through state signal, the DC link voltage, and the current of the two inductors.

Figure 11 shows the simulation results for $M = 0.9$. The effective values of line voltage and phase current are 85 V and 1 amp, respectively, and the DC link voltage has been increased to 145 V.

Figure 12 also shows the voltage waveform of capacitors, inductors and load current at $M = 0.9$.

Figure 13 shows the a-phase modulation signal and the DC link voltage at $M = 1.15$, which is the maximum amplitude modulation value. As can be seen, the DC source can provide the required power and the DC link voltage can be increased to 85 V, because the proposed inverter has the lowest shoot-through state.

Figure 14 shows the simulation results for a change in load voltage when the DC link voltage in the islanding state increases from 60 to 100. The peak voltage of the load is 150 V, which is set to 110 V RMS by increasing the amplitude modulation from 0.8 to 1.08 to maintain the voltage.

The frequency spectrum of the a-phase current is shown in Figure 15. The THD value of the current is 1.75% and the reason for this low harmonic is the low-frequency ripple of the capacitors in the circuit.

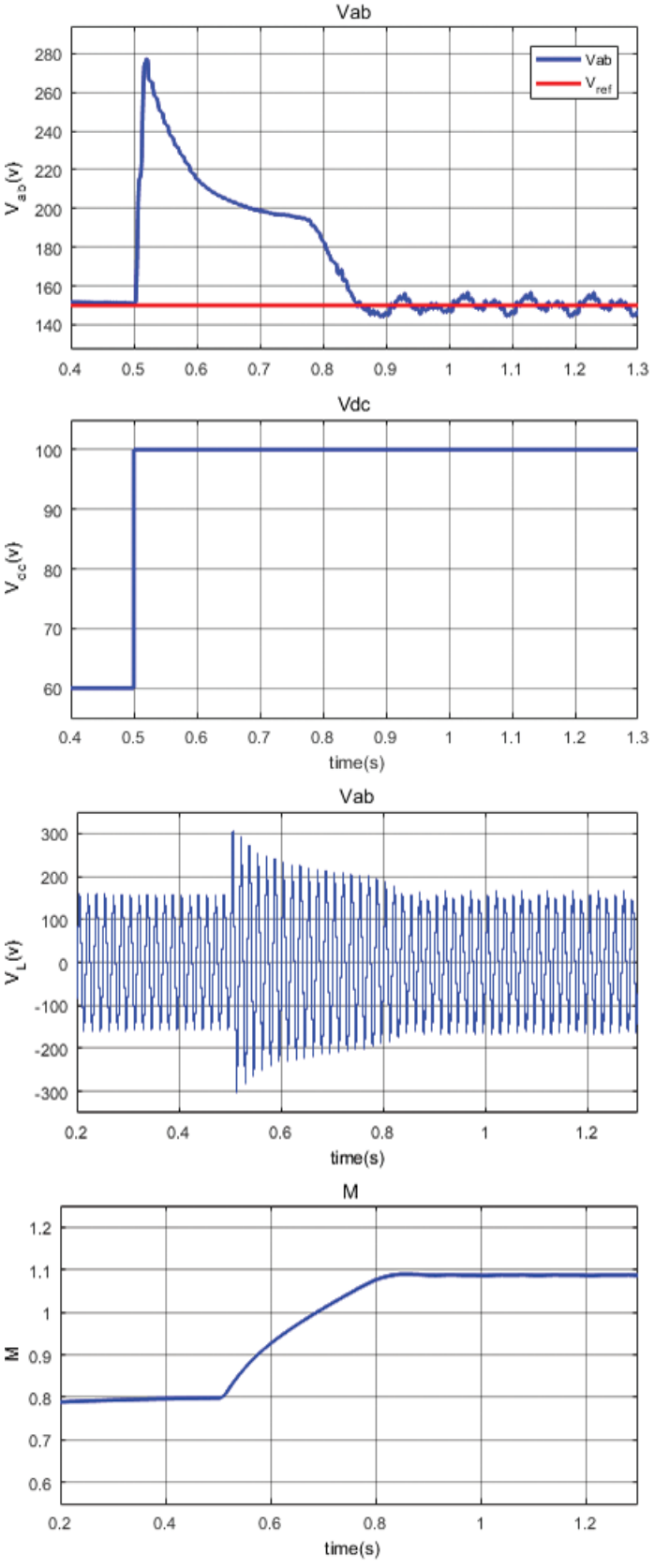


**Fig. 14.** Load voltage amplitude waveform, input voltage, load voltage and amplitude modulation for load voltage change when DC link voltage in islanding mode increases from 60 to 100.

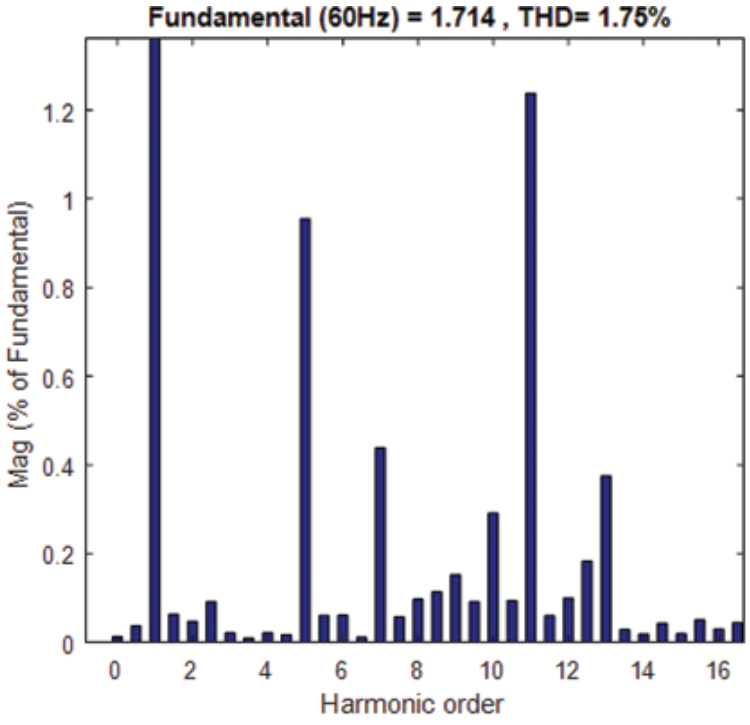


**Fig. 15.** Frequency spectrum of a-phase current. THD, total harmonic distortion.

## 5. Conclusion

In this paper, to study the inverter (MZS-NPC), which was a combination of a network of impedance source and a three-level inverter, a modified method for modulation based on the maximum boost control method was introduced and implemented to get the maximum possible gain. According to the simulation results, the DC link voltage increased to 205 V so that the effective voltage of 102 V can be received from a 40 V voltage source with $M = 0.8$. The THD value of the network current is 1.75% and the value of the output voltage was controlled by the reference value by changing the input voltage in the islanding mode. The results show that this converter is suitable for solar power plant and fuel cell applications in both islanding and network-connected modes.

### References

Akbari, R., Majid, H. and Mahsa, A. (2021). Design and Simulation of Dual Z-Source Dual-Input Hybrid 2/3 Level Inverter. *International Journal of Modelling and Simulation*, 42(5), pp. 1–15.

Akbari, E., Shafaghatian, N., Zishan, F., Montoya, O. D. and A. Giral-Ramírez, D. (2022). Optimized Two-Level Control of Islanded Microgrids to Reduce Fluctuations. *IEEE Access*, 10, pp. 95824–95838.

Balal, A., Dinkhah, S., Shahabi, F., Herrera, F. and Chuang, Y. L. (2022). A Review on Multilevel Inverter Topologies. *Emerging Science Journal*, 6(1), pp. 185–200.

P. Barbosa, P. Steimer, L. Meysenc, M. Winkelnkemper, J. Steinke and N. Celanovic, "Active Neutral-Point-Clamped Multilevel Converters," 2005 IEEE 36th Power Electronics Specialists Conference, 2005, pp. 2296-2301.

Brueske, S., Kuehne, R. and Fuchs, F. W. (2014). Comparison of Topologies for the Main Inverter of an Electric Vehicle. In: *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management,* VDE.

Dharmambal, V. and Nisha, K. C. R. (2022). Review on impedance source topologies and modulation techniques for multilevel cascaded inverter. In: *Proceedings of the 2nd International Conference on Recent Trends in Machine Learning, IoT, Smart Cities and Applications*, Springer, Singapore.

Do, D. T., Nguye, M. K., Quach, T. H., Tran, V. T., Blaabjer, F. and Vilathgamuwa, D. M. (2019). A PWM Scheme for a Fault-Tolerant Three-Level Quasi-Switched Boost T-Type Inverter. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(3), pp. 3029–3040.

Gong, R., Xue, B., Liu, J. and Zhang, X. (2022). Power Balance Modulation Strategy for Hybrid Cascaded H-bridge Multi-Level Inverter. *Electrical Engineering*, 104(2), pp. 753–762.

Husev, Oleksandr, and Carlos Roncero-Clemente. "Resonant and Z-source multilevel inverters." In *Multilevel Inverters*, pp. 217-257. Academic Press, 2021 .

Jayakumar, Vinoth, Bharatiraja Chokkalingam, and Josiah Lange Munda. "A comprehensive review on space vector modulation techniques for neutral point clamped multi-level inverters." *IEEE Access* 9 (2021): 112104-112144.

Khan, N. H., Barzegarkhoo, R., Siwakoti, Y. P., Khan, S. A., Li, L. and Blaabjerg, F. (2022). A New Switched-Capacitor Multilevel Inverter with Soft Start and Quasi Resonant Charging Capabilities. *International Journal of Electrical Power & Energy Systems*, 135, p. 107412.

Kolhe, Mohan Lal, Pawan Kumar Labhasetwar, and H. M. Suryawanshi, eds. *Smart Technologies for Energy, Environment and Sustainable Development: Select Proceedings of ICSTEESD 2018*. Berlin, Germany: Springer, 2019.

Liu, Y., Hoon, H. and Huang, A. Q. (2008). Real-Time Calculation of Switching Angles Minimizing THD for Multilevel Inverters with Step Modulation. *IEEE Transactions on Industrial Electronics,* 56(2), pp. 285–293.

Rath, D., Patra, A. K., Kar, S. K. and Rout, B. (2021). Modelling of machine learning controller based reduced switch multi level inverter. In: *2021 International Conference in Advances in Power, Signal, and Information Technology (APSIT*), IEEE.

Rivera, S., Wu, B., Kouro, S., Yaramasu, V. and Wang, J. (2014). Electric Vehicle Charging Station using a Neutral Point Clamped Converter with Bipolar DC bus. *IEEE Transactions on Industrial Electronics*, 62(4), pp. 1999–2009.

Rodriguez, J., Bernet, S., Steimer, P. K. and Lizama, I. E. (2009). A Survey on Neutral-Point-Clamped Inverters. *IEEE Transactions on Industrial Electronics*, 57(7), pp. 2219–2230.

Rodriguez, J., Lai, J. S. and Peng, F. Z. (2002). Multilevel Inverters: A Survey of Topologies, Controls, and Applications. *IEEE Transactions on Industrial Electronics*, 49(4), pp. 724–738.

Sankar, D. and Babu, C. (2020). Design and Analysis of a Novel Quasi Z Source Based Asymmetric Multilevel Inverter for PV Applications. *International Journal of Power Electronics and Drive Systems*, 11(3), pp. 1368.

Sapin, A., Steimer, P. K. and Simond, J. J. (2007). Modeling, Simulation, and Test of a Three-Level Voltage-Source Inverter with Output *LC* Filter and Direct Torque Control. *IEEE Transactions on Industry Applications*, 43(2), pp. 469–475.

Sayed, K., Almutairi, A., Albagami, N., Alrumayh, O., Abo-Khalil, A. G. and Saleeb, H. (2022). A Review of DC-AC Converters for Electric Vehicle Applications. *Energies*, 15(3), pp. 1241.

Sheir, A., Youssef, M. Z. and Orabi, M. (2018). A Novel Bidirectional T-type Multilevel Inverter for Electric Vehicle Applications. *IEEE Transactions on Power Electronics*, 34(7), pp. 6648–6658.

Strzelecki, R. (2006). Three-level Z-source neutral-point-clamped inverter. In: *2006 8th International Conference on Actual Problems of Electronic Instrument Engineering*, IEEE.

Vemuganti, H. P., Sreenivasarao, D., Ganjikunta, S. K., Suryawanshi, H. M. and Abu-Rub, H. A. (2021). A Survey on Reduced Switch Count Multilevel Inverters. *IEEE Open Journal of the Industrial Electronics Society*, 2, pp. 80–111.