

# A New 13-Level Switched-Capacitor Inverter with Reduced Device Count

Research Article

Kasinath Jena<sup>1,\*</sup>, Chinmoy Kumar Panigrahi<sup>1</sup>, Krishna Kumar Gupta<sup>2</sup>

<sup>1</sup>School of Electrical Engineering, KIIT Deemed to be University, Bhubaneswar, India

<sup>2</sup>THAPAR University, Patiala, India

Received: February 26, 2021; Accepted: June 07, 2021

**Abstract:** This paper proposed a new voltage-boosting 13-level switched-capacitor (SC) cost-effective inverter. The proposed topology comprises fourteen transistors, three capacitors and a single DC source to produce a 13-level staircase waveform. The capacitor voltage balancing problem is inherently solved by the series/parallel technique. Structural description, working principle, calculation of optimum values of capacitance and modulation scheme are briefly described. The comparative analyses with the existing SC multilevel inverter (MLI) in terms of voltage gain, blocking voltage, total standing voltage (TSV), component per level factor and cost function illustrate the merits of the proposed topology. Further, simulation and experimental results at different loading conditions verify the feasibility of the proposed topology.

**Keywords:** multilevel inverter • switched capacitor • voltage gain • component per level factor • cost function

## 1. Introduction

In recent years, multilevel inverter (MLI) has drawn remarkable attention because of the widespread application in non-conventional energy sources such as PV, wind, and fuel cells. This is because MLIs have several advantages over two-level inverters, such as improved waveform, low  $dv/dt$ , lower electromagnetic interference and lower total harmonic distortion (THD). The classical MLIs can be categorised into Diode clamped, Flying capacitor, and Cascaded H-Bridge inverter. However, several limitations, such as voltage balancing problems of DC-link capacitors in case of flying capacitor and diode clamped inverter and for Cascade H-Bridge, require multiple numbers of isolated DC source for the generation higher level of voltage, limited gain, and more number of active and passive components (Leon et al., 2017). Therefore, the novel concepts of 'Reduce device counts' and 'Maximize the voltage level' overcome the disadvantages of classical MLIs (Gupta et al., 2016; Gupta and Jain, 2012). However, the main issue of maximising the voltage level articles is characterised by unity gain.

The issues can be overcome by the switched capacitor (SC) technique, which has the following main advantages: (i) ability to boost the input voltage; (ii) the capacitor voltage is self-balanced; (iii) reduces the uses of multiple DC sources; and (iv) absence of a magnetic circuit. Therefore, switched capacitor multilevel inverters (SCMLIs) are very attractive nowadays to the researchers' community.

Several switched-capacitor topologies using series/parallel techniques to boost the input voltage have been developed. These topologies are mainly categorised as two-stage topology and single-stage topology. Two-stage topology has a back-end H-bridge circuit for the generation of the bipolar output voltage. Alternatively, single-stage topology does not require any back-end H-bridge to synthesised bipolar voltage with reduced voltage stress on the switches.

The two-stage topologies introduced in Hinago and Koizumi (2012), Khounjahan et al. (2019) and Fong et al. (2019) experience high voltage stress (i.e. equal to the load voltage) on the switches of the H-bridge circuit that

\* Email: kasi.jena@gmail.com

limits the high voltage application. Component counts and total standing voltage (TSV) are also significantly high in these topologies.

Single-stage topologies presented in Taghvaie et al. (2018), Bhatnagar et al. (2019) and Lee et al. (2019) experience uniform voltage stress across all the switches, but active and passive component counts are quite high. 13-level SC topology presented in Samadaei et al. (2019), Roy et al. (2020) and Samadaei et al. (2016) has multiple input sources along with high voltage stress on the switches. Single source modular 13-level k-type topologies in Zeng et al. (2020) have the least voltage gain. Additionally, we mention SC topologies (Barzegarkhoo et al., 2016; Saeedian et al., 2019) generating  $2^{n+1}$  output voltage, where  $n$  represents the number of the switched-capacitor unit.

Thirteen-level topologies are presented in Lin et al. (2019); however, when the number of levels is increased, then more individual switches possess high voltage stress. Nine-level topologies that are presented in Siddique et al. (2019) as well as in Sathik and Vijayakumar (2019) have less boosting factor. However, in topology, Siddique et al. (2019) capacitor ( $C_1$  and  $C_2$ ) voltages are not fully utilised. Thirteen-level SC topologies are advocated in Samadaei et al. (2019), Siddique et al. (2020) and Iqbal et al. (2020); herein, each topology is constituted by multiple numbers of the isolated DC source. For this reason, it can be said that the topologies mentioned in Samadaei et al. (2019), Siddique et al. (2020) and Iqbal et al. (2020) become more complex and costly.

The pros and cons elucidated in the preceding paragraph motivated us to design a new cost-effective self-balanced switched-capacitor inverter with reduced switching components in this paper, which has the following significant features:

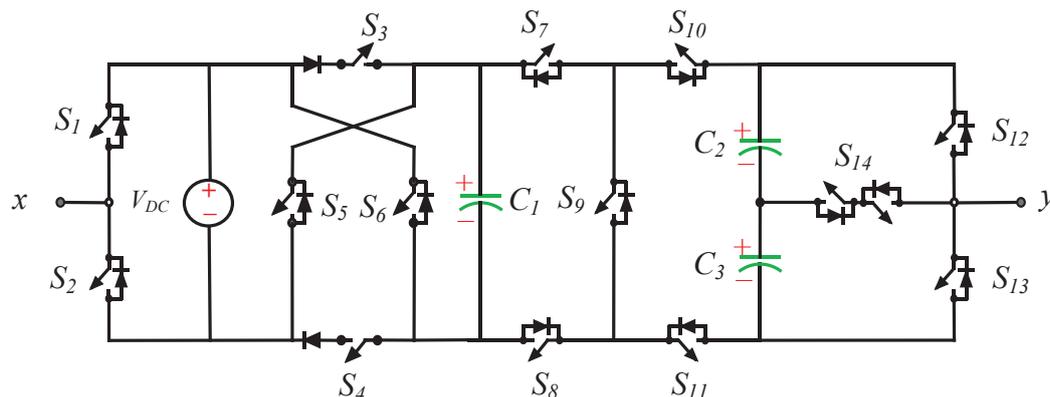
- (1) The capacitors' voltages are inherently self-balanced.
- (2) The ability to boost the input voltage is available.
- (3) Only a single DC source is utilised.
- (4) The number of switching components is reduced.
- (5) The voltage stress on the switches is reduced.

This paper is arranged in the following sequence: Section 2 illustrates the description of the proposed circuit configurations, working principle and determination of optimum values of capacitance. The modulation scheme for the switching operation is presented in Section 3. Analysis of the power losses of the proposed article is described in Section 4. Simulation and experimental results are discussed in Section 5 to prove the practicability of the proposed topology. Comparative analysis with the existing topology is introduced in Section 6 to validate the importance and superiority of the proposed topology. Finally, Section 7 concludes the paper.

## 2. Proposed Topology

### (a) Circuit description

Figure 1 shows the structural design of the proposed topology. It consists of fourteen power switches ( $S_1, S_2 \dots S_{14}$ ), three capacitors ( $C_1, C_2, C_3$ ) and a single DC source. The input DC source may be obtained from a battery, fuel



**Fig. 1.** Structural design of the proposed 13-level topology.

cell or solar cell. Moreover, the switching pairs  $S_1S_2$ ,  $S_5S_6$  and  $S_{12}S_{13}$  are operated in complementary mode during the different modes of operation. The proposed topology can synthesise 13 levels of voltage viz.  $\pm 3V_{DC}$ ,  $\pm 2.5V_{DC}$ ,  $\pm 2V_{DC}$ ,  $\pm 1.5V_{DC}$ ,  $\pm 1V_{DC}$ ,  $\pm 0.5V_{DC}$  and 0. The voltage gain of this topology is three times the supply voltage ( $3V_{DC}$ ). The switching combination for a different mode of operation is enlisted in Table 1. Note that, '0' and '1' depict the OFF and ON states of the switch. The load terminal is depicted as  $x$  and  $y$ ; and  $v_{xy}(t)$  and  $i_{xy}(t)$  represent the terminal load voltage and load current, respectively. The charging path of the capacitors and the direction of the load current are marked by the blue and red dotted lines.

### (b) Working principle

The working principle of the proposed topology is briefly explained with the following modes:

#### Mode 1. $v_{xy}(t) = 0$

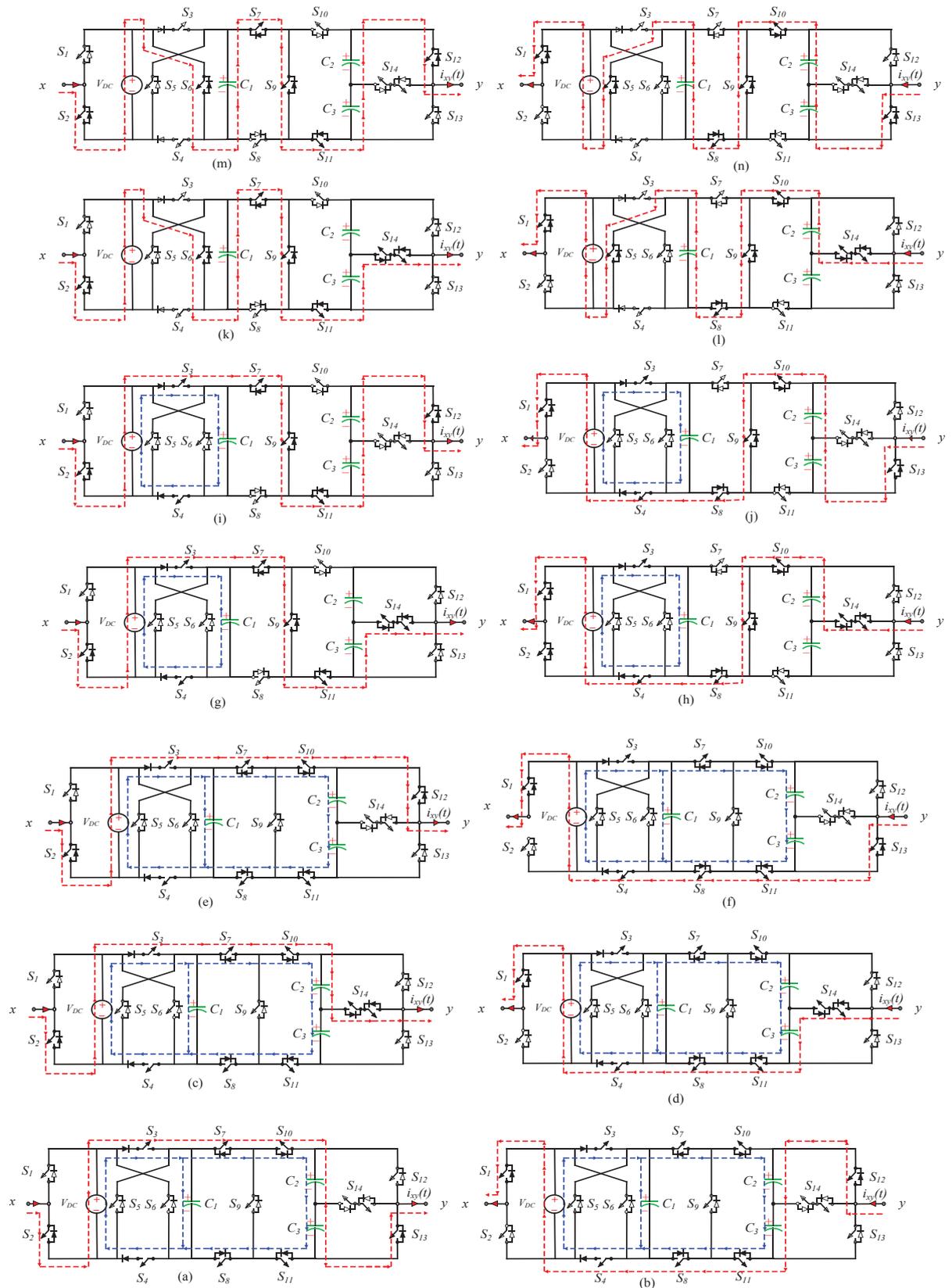
In this mode of operation,  $v_{xy}(t) = 0$ ,  $i_{xy}(t) > 0$  can be achieved by turning on the switches  $S_2, S_3, S_4, S_7, S_8, S_{10}, S_{11}$  and  $S_{13}$  simultaneously. The capacitor  $C_1$  is charged up to a voltage equivalent to the input supply  $V_{DC}$  and  $C_2, C_3$  is charged to  $0.5V_{DC}$  each, since all the capacitors are brought in parallel with the input supply. The direction of the charging path of the capacitor and current is as shown in Figure 2(a). Similarly, for the  $v_{xy}(t) = 0$ ,  $i_{xy}(t) < 0$  can be achieved by switching ON  $S_1, S_3, S_4, S_7, S_8, S_{10}, S_{11}$  and  $S_{12}$  simultaneously. The equivalent circuit diagram is as shown in Figure 2(b).

#### Mode 2. $v_{xy}(t) = \pm 0.5V_{DC}$

In this mode of operation,  $v_{xy}(t) = +0.5V_{DC}$  can be achieved by turning on  $S_2, S_3, S_4, S_7, S_8, S_{10}, S_{11}$  and  $S_{14}$  simultaneously. During this mode, the capacitors  $C_1, C_2, C_3$  are brought in parallel with the input source, and hence  $C_1$  is charged up to  $V_{DC}$ , and  $C_2, C_3$  are charged up to  $0.5V_{DC}$  each. The equivalent circuit is as shown in Figure 2(c). Similarly,  $v_{xy}(t) = -0.5V_{DC}$ , can be achieved by turning on  $S_1, S_3, S_4, S_7, S_8, S_{10}, S_{11}$  and  $S_{14}$  simultaneously. The equivalent circuit is as shown in Figure 2(d).

**Table 1.** Switching combination of the proposed topology

Mode	Active switch														$V_{xy}(t)[V]$
	$S_1$	$S_2$	$S_3$	$S_4$	$S_5$	$S_6$	$S_7$	$S_8$	$S_9$	$S_{10}$	$S_{11}$	$S_{12}$	$S_{13}$	$S_{14}$	
1	0	1	1	1	0	0	1	1	0	1	1	0	1	0	0
	1	0	1	1	0	0	1	1	0	1	1	1	0	0	0
2	0	1	1	1	0	0	1	1	0	1	1	0	0	1	0.5
	1	0	1	1	0	0	1	1	0	1	1	0	0	1	-0.5
3	0	1	1	1	0	0	1	1	0	1	1	1	0	0	1
	1	0	1	1	0	0	1	1	0	1	1	0	1	0	-1
4	0	1	1	1	0	0	1	0	1	0	1	0	0	1	1.5
	1	0	1	1	0	0	0	1	1	1	0	0	0	1	-1.5
5	0	1	0	0	0	1	1	0	0	1	0	1	0	0	2
	1	0	0	0	1	0	0	1	1	1	0	0	1	0	-2
6	0	1	0	0	0	1	1	0	1	0	1	0	0	1	2.5
	1	0	0	0	1	0	0	1	1	1	0	0	0	1	-2.5
7	0	1	0	0	0	1	1	0	1	0	1	1	0	0	3
	1	0	0	0	1	0	0	1	1	1	0	0	1	0	-3



**Fig. 2.** (a-n) Operating states for different voltage levels.

Mode 3.  $v_{xy}(t) = \pm 1V_{DC}$ ,

In this mode,  $v_{xy}(t) = +1V_{DC}$  can be achieved by turning on the switches  $S_2, S_3, S_4, S_7, S_8, S_{10}, S_{11}$  and  $S_{12}$  simultaneously. The capacitors  $C_1, C_2, C_3$  are brought in parallel with the input DC source. The capacitor  $C_1$  is charged up to  $V_{DC}$  and  $C_2, C_3$  is charged up to  $0.5 V_{DC}$ . The equivalent circuit diagram is as shown in Figure 2(e). Similarly,  $v_{xy}(t) = -1V_{DC}$ , be achieved by turning on  $S_1, S_3, S_4, S_7, S_8, S_{10}, S_{11}$  and  $S_{13}$  simultaneously. The equivalent circuit diagram is as shown in Figure 2(f).

Mode 4.  $v_{xy}(t) = \pm 1.5V_{DC}$

In, this mode of operation, the switches  $S_2, S_3, S_4, S_7, S_9, S_{11}$  and  $S_{14}$  are turned on simultaneously to achieve  $v_{xy}(t) = +1.5V_{DC}$ . The capacitor  $C_1$  is charged up to  $V_{DC}$  and  $C_3$  releases its stored energy to the load along with the supply input  $V_{DC}$ . The equivalent circuit diagram is as shown in Figure 2(g). Similarly,  $v_{xy}(t) = -1.5V_{DC}$  can be achieved by turning on  $S_1, S_3, S_4, S_8, S_9, S_{11}$  and  $S_{14}$  simultaneously. The equivalent circuit diagram is as shown in Figure 2(h).

Mode 5.  $v_{xy}(t) = \pm 2V_{DC}$

In this mode,  $v_{xy}(t) = +2V_{DC}$  can be obtained by turning on the switches  $S_2, S_3, S_4, S_7, S_9, S_{11}$  and  $S_{12}$  simultaneously. The capacitor  $C_1$  is brought in series with the source and hence it releases its stored energy to the load along with the supply input source  $V_{DC}$ . The equivalent circuit diagram is as shown in Figure 2(i). Similarly,  $v_{xy}(t) = -2V_{DC}$  can be achieved by turning on  $S_1, S_3, S_4, S_8, S_9, S_{10}$  and  $S_{13}$  simultaneously. The equivalent circuit diagram is as shown in Figure 2(j).

Mode 6.  $v_{xy}(t) = \pm 2.5V_{DC}$

In this mode of operation,  $v_{xy}(t) = +2.5V_{DC}$  can be achieved by switching on  $S_2, S_6, S_7, S_9, S_{11}$  and  $S_{14}$  simultaneously. During this mode, the capacitors  $C_1$  and  $C_3$  are in series with the source and release their stored energy along with the input supply source  $V_{DC}$  to the load. The equivalent circuit configuration is as shown in Figure 2(k). Similarly,  $v_{xy}(t) = -2.5V_{DC}$  can be achieved by switching on  $S_1, S_5, S_7, S_9, S_{11}$  and  $S_{14}$  simultaneously. The equivalent circuit configuration is as shown in Figure 2(l).

Mode 7.  $v_{xy}(t) = \pm 3V_{DC}$

In this mode of operation,  $v_{xy}(t) = 3V_{DC}$  can be achieved by switching on  $S_2, S_6, S_7, S_9, S_{11}$  and  $S_{12}$  simultaneously. During this mode, the capacitors  $C_1, C_2$  and  $C_3$  are connected in series with the supply source, and hence, capacitors release their stored energy to the load along with the DC source. The equivalent circuit diagram is as shown in Figure 2(m). Similarly,  $v_{xy}(t) = 3V_{DC}$  can be achieved by switching on  $S_1, S_5, S_8, S_9, S_{11}$  and  $S_{13}$  simultaneously. The equivalent circuit diagram is as shown in Figure 2(n).

### (c) Self-balancing mechanism

The capacitors are self-balanced due to the series/parallel technique (Babaei and Gowgani, 2014). The details of the charging and discharging of capacitors are explained in Figure 2, which shows that the capacitors are automatically charged to their respective voltage i.e.  $C_1$  is charged to  $V_{DC}$  and  $C_2, C_3$ , are charged to  $0.5 V_{DC}$  in every fundamental cycle of the load voltage. This repeatedly charging and discharging over every fundamental cycle makes the capacitors self-balanced.

### (D) Determination of optimum values of capacitance

The value of capacitance plays a crucial role in the SC inverter design. This is because the values of capacitance will decide the ripple loss, size and cost (Taghvaie et al., 2018).

The discharging amount of capacitor depends upon the following factors viz. longest period of discharging, maximum load current and power factor. Thus, the selection of optimum values of capacitance is vital. The maximum amount of charge released in the capacitor can be expressed as displayed in Figure 2.

$$Q_{Ci} = \int_{\theta_i}^{\pi-\theta_i} I_m \sin(\omega t - \varnothing) dt \quad (1)$$

where  $\theta_i$  and  $\pi - \theta_i$  are the initial and final time value of discharging period,  $\varnothing$  is the load power factor angle and  $I_m$  is the maximum load current.  $f_0$  represents fundamental frequency. Therefore, the values of capacitance should satisfy the following condition:

$$C_i \geq \frac{\Delta Q_{Ci}}{\Delta V_i} \quad (2)$$

For a purely resistive load, the maximum voltage ripple can be expressed as

$$\Delta V_i = \frac{\Delta Q_i}{C_i} \quad (3)$$

$$\Delta V_1 = \frac{1}{\omega C R_1} \int_{\theta_3}^{\pi-\theta_3} 2.5V_{DC} dt + \frac{1}{\omega C R_1} \int_{\theta_4}^{\pi-\theta_4} 3V_{DC} dt \quad (4)$$

$$\Delta V_1 = \frac{V_{DC}}{\omega C R_1} [5.5\pi - 5\theta_3 - 6\theta_4] \quad (5)$$

$$\Delta V_2 = \frac{1}{\omega C R_1} \int_{\theta_1}^{\pi-\theta_1} 1.5V_{DC} dt + \frac{1}{\omega C R_1} \int_{\theta_2}^{\pi-\theta_2} 2V_{DC} dt + \frac{1}{\omega C R_1} \int_{\theta_3}^{\pi-\theta_3} 2.5V_{DC} dt + \frac{1}{\omega C R_1} \int_{\theta_4}^{\pi-\theta_4} 3V_{DC} dt \quad (6)$$

$$\Delta V_2 = \frac{V_{DC}}{\omega C R_1} [9\pi - 3\theta_1 - 4\theta_2 - 5\theta_3 - 6\theta_4] \quad (7)$$

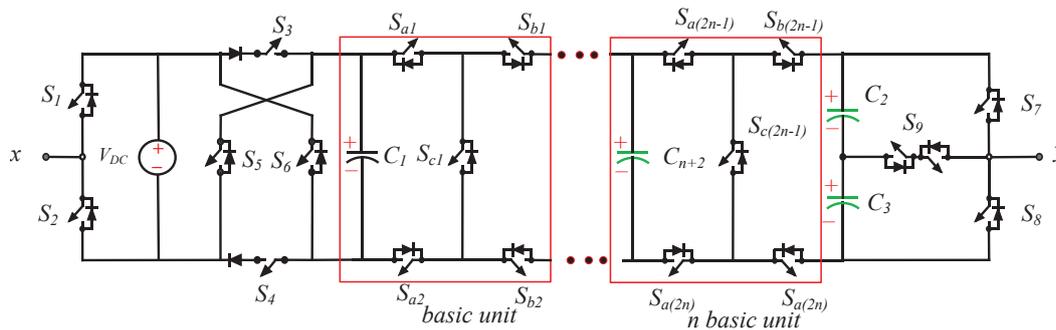
Similarly,  $\Delta V_3$  can be calculated.

The time instance for discharging of the capacitor from Figure 3(b) would be as follows (Taghvaie et al., 2018).

$$\theta_4 = \frac{\sin^{-1}\left(\frac{2.5}{3}\right)}{2\pi f_0} \quad (8)$$

$$\theta_3 = \frac{\sin^{-1}\left(\frac{2}{3}\right)}{2\pi f_0} \quad (9)$$

Similarly, others can be calculated.



**Fig. 3.** Generalised SC topology. SC, switched capacitor.

## (E) Generalised structure of the proposed topology

The generalised structure to reach higher voltage level, based on the primary circuit (displayed in Figure 1), is shown in Figure 3. According to the generalised structure, high gain and higher voltage levels can be achieved by connecting  $m$  basic unit in series. The basic unit consists of one capacitor and five power switches. If  $n$  be the number of the basic unit, then the number of capacitors, number of power switches, number of voltage level and maximum output voltage are as follows:

$$N_l = 2n + 11 \quad (10)$$

$$N_{sw} = 5n + 10 \quad (11)$$

$$V_{max} = (n + 2)V_{DC} \quad (12)$$

$$TSV = 2n + 12 \quad (13)$$

### 3. Control Scheme

Several switching schemes are used for generating the switching pulse of the inverters. In this proposed topology, a high switching frequency simple level-shift pulse width modulation strategy is employed, and the same is displayed in Figure 4. In this technique, 12 triangular carrier waves ( $e_1 \sim e_{12}$ ) of high frequencies (expressed in KHz) each of magnitude  $1/6$  are continuously compared with a reference frequency ( $f_{ref}$ ) of 50 Hz. Out of 12 carrier signals, 6 ( $e_1 \sim e_6$ ) are taken as positive signals and ( $e_7 \sim e_{12}$ ) the remaining as negative carrier signals, as shown in Figure 3(b). The switching pulses for the positive half cycle with a few switches are shown in Figure 4(a). Similarly, negative half-cycle can be represented as shown in Figure 4(a).

The switching functions are expressed by the simple logical OR operation, which is expressed by Eqs (10)–(23)

$$S_1 = y_{11} + x_{11} + x_{22} + y_{22} + x_{22} + y_{33} + x_{33} + y_{44} + x_{44} + y_{55} + x_{55} + y_{66} + x_{66} \quad (14)$$

$$S_2 = y_1 + x_1 + x_2 + y_2 + x_2 + y_3 + x_3 + y_4 + x_4 + y_5 + x_5 + y_6 + x_6 \quad (15)$$

$$S_3 = y_{11} + y_1 + x_1 + y_2 + x_{11} + y_{22} + x_2 + y_3 + x_{22} + y_{33} + x_3 + y_4 + x_{33} + y_{44} \quad (16)$$

$$S_4 = y_{11} + y_1 + x_1 + y_2 + x_{11} + y_{22} + x_2 + y_3 + x_{22} + y_{33} + x_3 + y_4 + x_{33} + y_{44} \quad (17)$$

$$S_5 = x_{44} + y_{55} + x_{55} + y_{66} + x_{66} \quad (18)$$

$$S_6 = y_4 + x_4 + y_5 + x_5 + y_6 + x_6 \quad (19)$$

$$S_7 = y_{11} + y_1 + x_1 + y_2 + x_{11} + y_{22} + x_2 + y_3 + x_{22} + y_{33} + x_3 + y_4 + x_4 + y_5 + x_5 + y_6 + x_6 \quad (20)$$

$$S_8 = y_{11} + y_1 + x_1 + y_2 + x_{11} + y_{22} + x_2 + y_3 + x_{22} + y_{33} + x_{33} + y_{44} + x_{44} + y_{55} + x_{55} + y_{66} + x_{66} \quad (21)$$

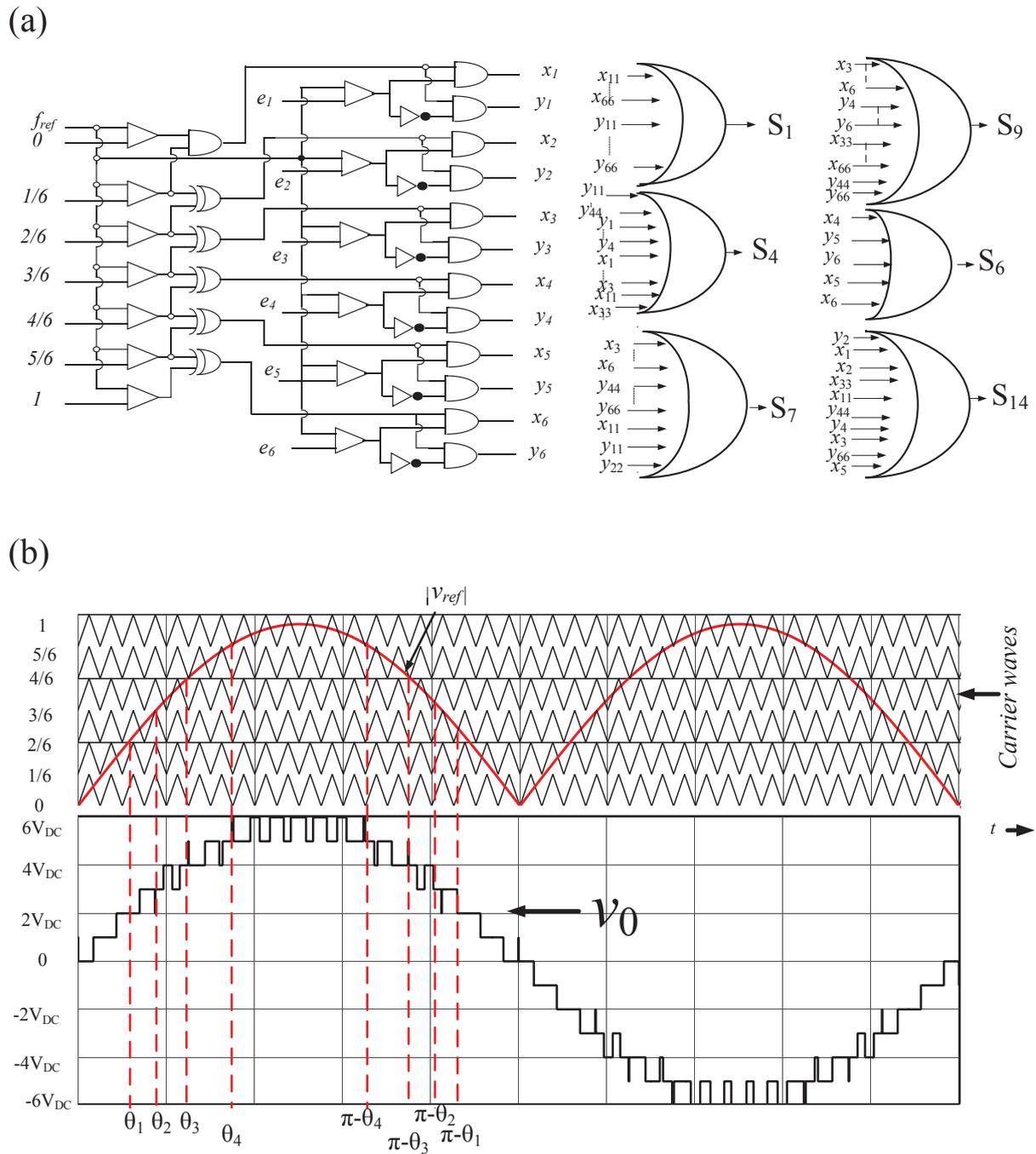
$$S_9 = x_3 + y_3 + x_{33} + y_{44} + x_{44} + y_{55} + x_5 + y_6 + x_{55} + y_{66} + x_6 + x_{66} \quad (22)$$

$$S_{10} = y_{11} + y_1 + x_1 + y_2 + x_{11} + y_{22} + x_2 + y_3 + x_{22} + y_{33} + x_{33} + y_{44} + x_4 + y_5 + x_{44} + y_{55} + x_{55} + y_{66} + x_{66} \quad (23)$$

$$S_{11} = y_{11} + y_1 + x_1 + y_2 + x_{11} + y_{22} + x_2 + y_3 + x_{22} + y_{33} + x_3 + y_4 + x_5 + y_6 + x_6 \quad (24)$$

$$S_{12} = y_{11} + x_2 + y_3 + x_4 + y_5 + x_6 \quad (25)$$

$$S_{13} = y_1 + x_{22} + y_{33} + x_{44} + y_{55} + x_{66} \quad (26)$$



**Fig. 4.** (a) Modulation scheme and (b) Output voltage.

$$S_{14} = x_1 + y_2 + x_{11} + y_{22} + x_3 + y_4 + x_{33} + y_{44} + x_5 + y_6 + x_{55} + y_{66} \quad (27)$$

## 4. Analysis of Power Losses

The power losses of the proposed inverter are broadly categorised as (i) switching losses, (ii) conduction losses and (iii) capacitor ripple losses.

## (i) Switching losses

This loss occurs due to the transition of switching states. The transition of the state refers to the turn-on, followed by the turn-off, of the switches, or vice versa. The power losses for a practical switch during turn-on and turn-off can be explained as follows (Bhatnagar et al., 2019).

Power losses due to turn-on:

$$P_{on,sw} = \frac{1}{6} f_0 (V_{on} I_{on} T_{on}) \quad (28)$$

Power losses due to turn-off:

$$P_{off,sw} = \frac{1}{6} f_0 (V_{off} I_{off} T_{off}) \quad (29)$$

where  $V_{on}, V_{off}$  are the voltage across the switches before the turn-on and after the turn-off, respectively.

$I_{on}, I_{off}$  are the current flowing through the switches after turn-on and before the turn-off, respectively.  $T_{on}$  and  $T_{off}$  are the turn-on and turn-off time of the switch. Thus, overall switching power losses ( $P_{sw}$ ) of the proposed topology are expressed in Eq. (26).

$$P_{sw} = \sum_{n=1}^{13} \sum_{m=1}^{14} (P_{on,sw,m} + P_{off,sw,m}) \quad (30)$$

where  $n$  and  $m$  represent the number of levels and the number of switches, respectively.

## (ii) Conduction losses

Conduction losses are caused due to power dissipation in the internal resistance of power semiconductor switches and diodes when the current is flowing through it (Hinago and Koizumi, 2012).

## (a) Conduction losses for the power switch

$$P_{c,sw} = V_{on,sw} I_{sw,avg} + I_{sw,rms}^2 R_{on,sw} \quad (31)$$

## (b) Conduction losses for diode

$$P_{c,d} = V_{on,d} I_{d,avg} + I_{d,rms}^2 R_{on,d} \quad (32)$$

where  $V_{on,sw}, V_{on,d}$  are the on-state voltage of switch and diode, respectively.

$I_{sw,avg}, I_{d,avg}$  and  $I_{sw,rms}, I_{d,rms}$  are the average and root mean square (RMS) current of switch and diode, respectively.

Hence, overall conduction losses ( $P_c$ ) of switches and diodes are given by:

$$P_c = \sum_{i=1}^k \left( \sum_{j=1}^n (P_{c,sw} + P_{c,d}) \right) \quad (33)$$

where  $n$  = Number of switches and  $k$  = Number of the conduction path.

(c) Capacitor ripple losses ( $P_{cap}$ )

This loss is caused due to the charging of capacitors when the current is flowing through the capacitor. So the capacitor ripple voltage can be written according to Babaei and Gowgani (2014).

$$\Delta V_{Ci} = \frac{1}{C_i} \int_{\theta_i}^{\pi-\theta_i} I_m(t) dt \quad (34)$$

where  $\Delta V_{Ci}$ ,  $I_m(t)$  is the ripple voltage and discharging current (i.e. load current), respectively. Therefore, the capacitor ripple loss can be expressed as: capacitor's ripple loss ( $P_{cap}$ ).

$$P_{Cap} = \frac{f}{2} \sum_{i=1}^3 (C_i \Delta V_{Ci}^2) \quad (35)$$

Therefore, the overall losses ( $P_{overall}$ ) are the sum of switching losses, conduction losses and capacitor ripple losses.

$$P_{overall} = P_{sw} + P_c + P_{cap} \quad (36)$$

At last, the efficiency ( $\eta$ ) can be calculated as:

$$\% \eta = \left( \frac{P_{out}}{P_{in}} \right) \times 100 \quad (37)$$

$$\% \eta = \left( \frac{P_{out}}{P_{out} + P_{overall}} \right) \times 100 \quad (38)$$

## 5. Performance Verification

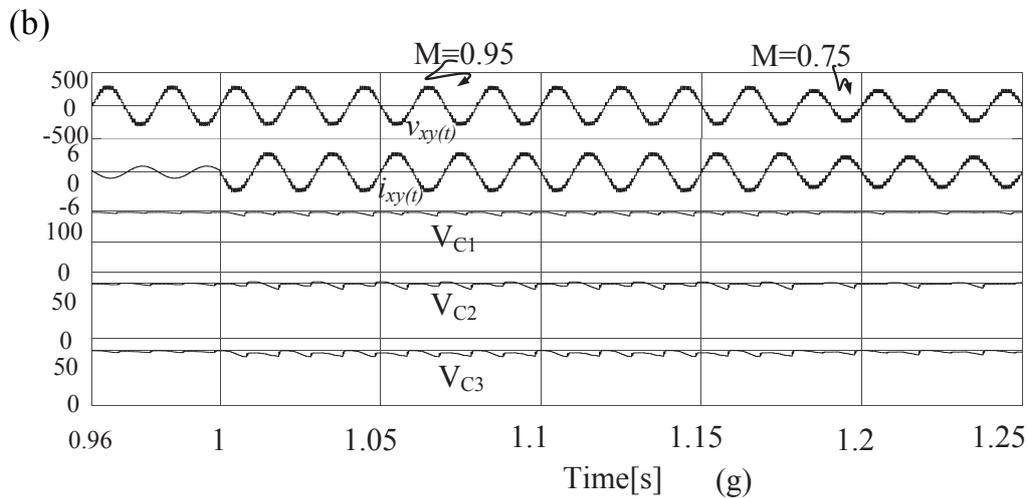
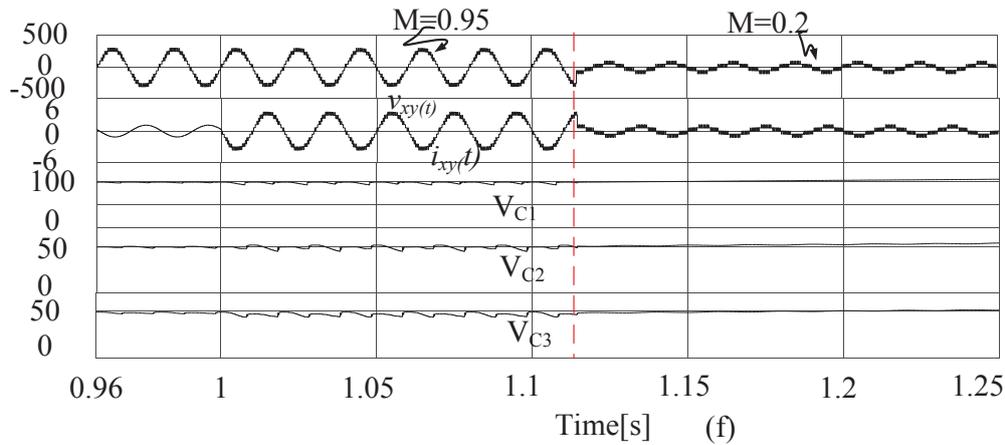
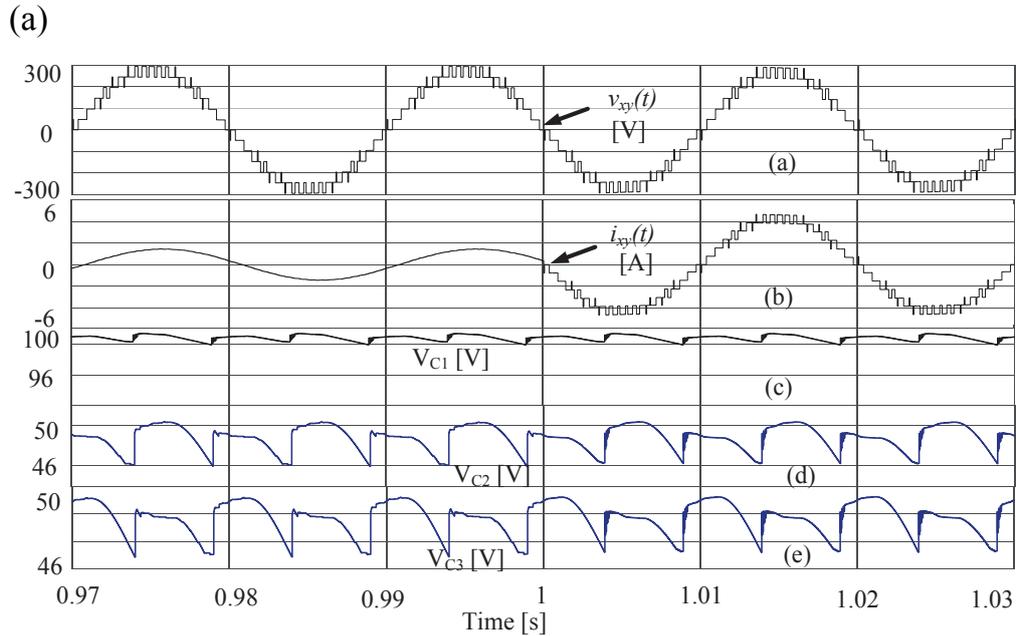
To investigate the performance and operation, the proposed topology is simulated in MATLAB/Simulink environment and experimentally in the hardware set-up. The parameters for the experimental set-up (i.e. laboratory prototype) and simulation are listed in Table 2.

### (a) Simulation results

The proposed novel work is simulated in the MATLAB/Simulink platform to verify the theoretical concept. The simulation results are displayed in Figure 5 under steady-state and step change in loading condition. The output voltages, load current, and the voltage across capacitors for RL-load are as shown in Figure 5(a–g). It is evident from the waveform that the voltage level remains intact under steady and step change in load. The proposed topology generates 13 levels of voltage with a maximum peak value of  $3 V_{DC}$ . Also, the capacitor's voltages, under any sudden change in load condition, maintained their self-voltage balancing properties of

**Table 2.** Parameters for the simulation and experimental model

Parameter	Specification
Input DC source ( $V_{DC}$ )	100 V
Fundamental frequency (f)	50 Hz
Carrier frequency ( $c_i(t)$ )	2 kHz
RL-Load	R = 100 $\Omega$ , L = 80 mH
R-Load	100 $\Omega$
Capacitor ( $C_1 = C_2 = C_3$ )	4,700 $\mu F$
Power switches (IGBTs)	GW30NC120HD
dSPACE DS 1104	
Modulation index (M)	0.95, 0.2 and 0.75



**Fig. 5.** Simulation results (a) load voltage, (b) load current, (c–e) capacitors voltage, (f, g) output voltage, current, voltage across capacitors for the modulation index of  $M = 0.95$ ,  $M = 0.2$  and  $M = 0.75$

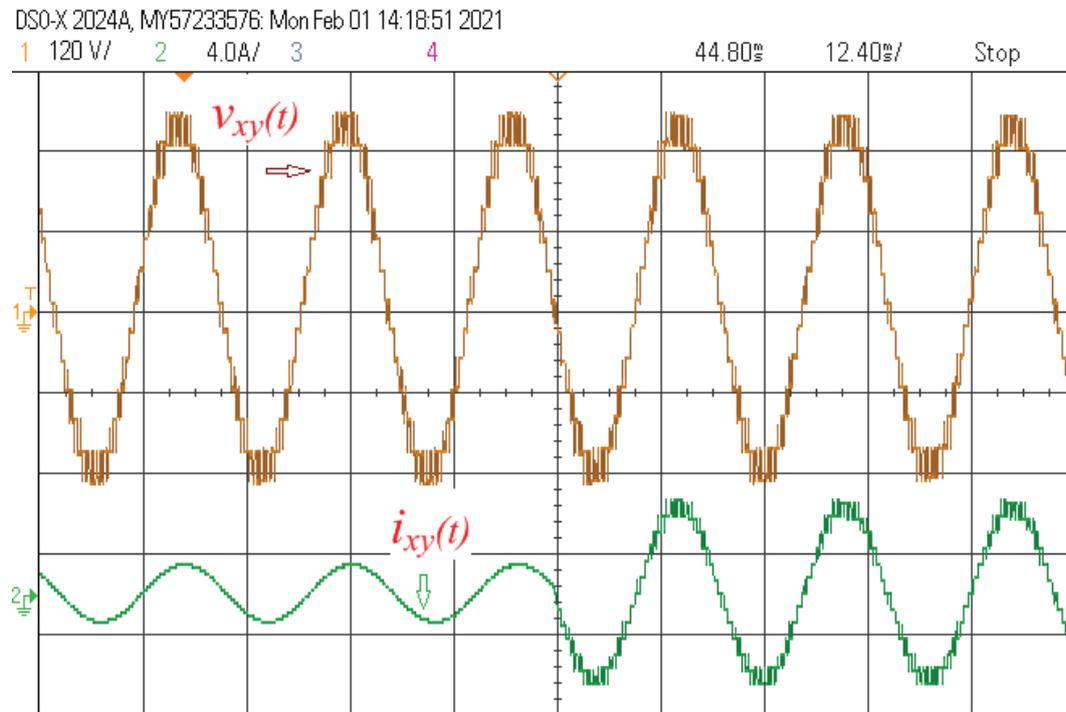
capacitors, which are shown in Figure 5(c–e). Simulation results for different modulation indexes are shown in Figure 5(f, g).

Figure 5(f, g) shows the simulation results for the modulation index  $M = 0.95$ ,  $M = 0.2$  and  $M = 0.75$ , respectively.

**(b) Experimental results**

The experimental work has been carried out with the help of a laboratory prototype to prove the performance and feasibility of the proposed topology. The experimental results under steady-state and step change in loading conditions are shown in Figure 6(a–d). It is observed that the output voltage levels, as well as the voltage across the capacitors, remain intact during the sudden load change and validate the self-balancing mechanism of capacitors’

(a)



(b)

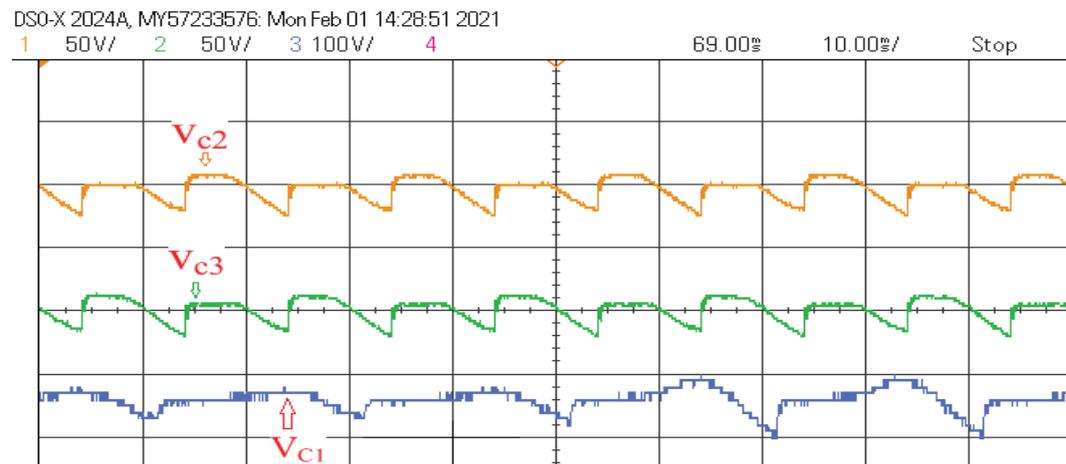
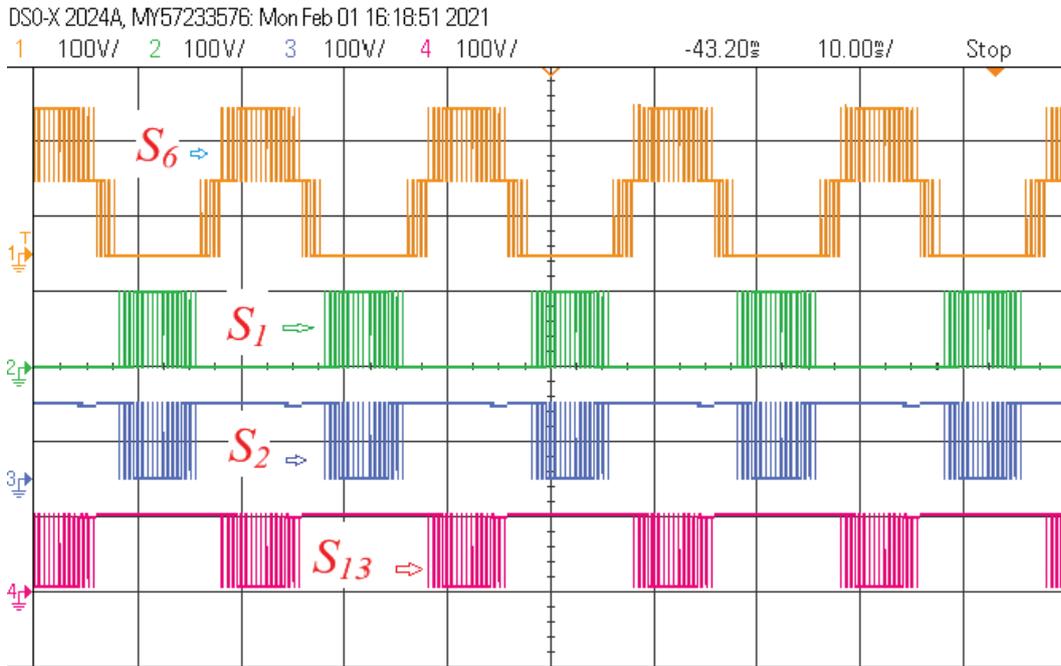
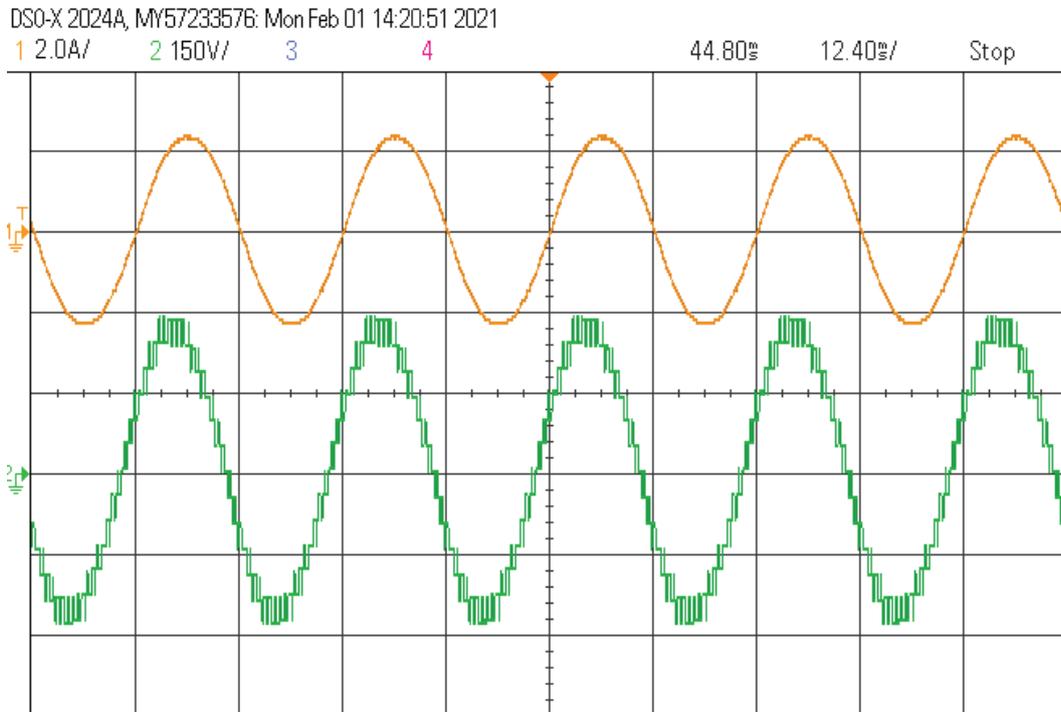


Fig. 6. (Continued).

(c)



(d)



**Fig. 6.** Experimental outcomes (a) load voltage, load current (b) capacitors voltage (c) voltage stresses on few switches and (d) steady-state voltage and current.

voltage. Note that the voltage developed at the output voltage level has an equal step of voltage i.e., 50 V. The voltage boosting ability is three times the supply voltage. The voltage across few switches is shown in Figure 6(c). Finally,

experimental results are well matched with the simulation results; therefore, it proves the superior performance and feasibility of the proposed topology.

## 6. Comparative Analysis

To evaluate the advantages of the proposed 13-level SC topology, a brief comparative analysis has been accomplished with the existing well-known topologies, in terms of TSV, components count per level factor ( $F_{CL}$ ), gain, maximum blocking voltage, and cost function. The comparative studies are summarised in Tables 3, 4 and 5. The component per level factor can be expressed as available in Eq. (39).

$$F_{C/L} = \frac{N_S + N_{SW} + N_C + N_D + N_{DRI}}{N_L} \quad (39)$$

And cost function may be defined as:

$$CF = \frac{N_S(N_{SW} + N_C + N_D + N_{DRI} + \delta * TSV)}{N_L} \quad (40)$$

where,  $N_L, N_{SW}, N_S, N_C, N_D, N_{DRI}, N_L, \delta$  are the number of levels, number of switches, number of sources, number of capacitors, number of diodes, number of levels, number of the driver unit and weight factor, respectively. The weight factor can be considered as either less than, greater than or equal to one according to the importance of switching components or TSV (Zeng et al., 2020). For the proposed topology, weight factor has been taken as one ( $\delta=1$ ) because both the switching components and TSV are given equal importance.

(a) Based on TSV value: TSV is defined by the sum of voltage stress on the individual switches. According to the TSV comparisons with the different 13-level topologies (Hinago and Koizumi, 2012; Ye et al., 2014; Samadaei et al., 2019; Roy et al., 2020; Samadaei et al., 2016; Zeng et al., 2020; Lin et al., 2019; Siddique et al., 2020; Iqbal et al., 2020) the proposed one has the least TSV value. However, topologies mentioned in Hinago and Koizumi (2012) and Ye et al. (2014) have back-end H-bridge, the voltage stresses on the switches of the H-bridge are

**Table 3.** Comparative analysis with the recent SC topologies

Ref.	$N_L$	$N_S$	$N_{SW}$	$N_C$	$N_D$	$N_{DRI}$	Gain	BV	TSV( $\times V_{dc}$ )	$F_{CL}$	CF
Siddique et al. (2020)	7	1	12	2	–	11	3	2	16	3.57	5.87
Bhatnagar et al. (2019)	9	1	11	2	–	10	2	1	11	2.55	3.77
Peng et al. (2019)	7	1	8	2	2	8	3	3	18	2.85	5.42
Ye et al. (2014)	13	1	10	5	10	10	6	6	59	2.69	7.23
Hinago and Koizumi (2012)	13	1	19	5	–	19	6	6	39	3.07	6.30
Samadaei et al. (2016)	13	4	10	–	–	8	1.5	6	32	1.38	15.38
Samadaei et al. (2019)	13	2	14	2	–	11	3	6	39	2.23	20.30
Roy et al. (2020)	13	2	16	3	2	16	3	6	34	3	10.92
Zeng et al. (2020)	13	1	14	4	–	14	1.5	2	40	2.46	5.53
Lin et al. (2019)	13	1	14	4	–	13	3	2	18	2.46	3.76
Samadaei et al. (2019)	13	2	11	2	–	10	3	6	32	1.92	8.46
Siddique et al. (2020)	13	2	11	2	–	10	3	6	34	1.85	8.61
Iqbal et al. (2020)	13	2	13	2	–	12	1.5	3	42	2.23	10.61
[P]	13	1	15	3	–	14	3	2	17	2.53	3.76

BV, blocking voltage; CF, cost function; SC, switched capacitor; TSV, total standing voltage.

**Table 4.** Comparison of the proposed topology with SCs-based topologies presented in Siddique et al. (2019), Sathik et al. (2019)

Ref.	$N_L$	$N_S$	$N_{SW}$	$N_C$	$N_D$	$N_{DRI}$	Gain	BV	TSV( $\times V_{dc}$ )	$F_{CL}/\text{gain}$	CF/gain
Siddique et al. (2019)	9	1	10	2	–	9	2	2	11	1.22	1.77
Sathik et al. (2019)	9	1	11	2	–	10	2	1	11	1.22	1.77
[P]	13	1	15	3	–	14	3	2	17	0.84	1.25

BV, maximum blocking voltage; CF, cost function; SCs, switched capacitors; TSV, total standing voltage.

**Table 5.** Comparison of the proposed topology with conventional topologies (NPC, FC and CHB)

	$N_L$	$N_S$	$N_{SW}$	$N_C$	$N_D$	TSV( $\times V_{dc}$ )	Gain	$F_{CL}$	CF
NPC	13	12	24	–	–	24	1	6.3	8.15
FC	13	12	24	12	12	24	1	5.53	7.38
CHB	13	6	24	–	–	24	1	4.15	5.92
[P]	13	1	15	3	–	16	3	2.54	5.31

TSV, total standing voltage; CF, cost function; NPC, neutral point clamped inverter; FC, flying capacitor inverter; CHB, cascaded H-bridge inverter.

equal to the peak value of the output voltage, and hence total voltage stresses increase. Additionally, these topologies withstand high voltage stresses. Moreover, the single-stage topologies advocated in Samadaei et al. (2019), Roy et al. (2020), Samadaei et al. (2016), Siddique et al. (2020) and Iqbal et al. (2020) have high voltage stresses on the switches. These characteristics limit its application for high and medium power. Moreover, from Table 5 it can be judged that the conventional topologies have more TSVs that will lead to the degradation of efficiency.

- (b) Component count per level factor: This factor plays a significant role because of all the switching components associated with the heat sink, driver unit, protection unit etc. The proposed topology has the least switching components per level as listed in Table 3 except for the topology (Samadaei et al., 2019, 2016). This indicates the proposed topology has less volume. Although topologies mentioned in Samadaei et al. (2019, 2016); Siddique et al. (2020) and Iqbal et al. (2020) have the least component count, the number of source units is more, which makes it more complex and completed. Moreover, topologies mentioned in Zeng et al. (2020) and Lin et al. (2019) have less number of component counts but use more number of capacitors that increase the inrush current and stress, which is a major issue in the SC topologies. From Table 4, it can be observed that the component count per level per gain for the topologies mentioned in Siddique et al. (2019) as well as in Sathik and Vijayakumar (2019) are high as compared to the proposed topology. Conventional topologies have a larger switching component count per level, as shown in Table 5, when compared with the suggested paper.
- (c) Cost function: This section includes the overall cost per level generation to assess the design effectiveness. It can be seen from the comparative Tables 3 and 4 that the proposed novel topology has the least cost function among all the 13-level topologies, excluding Lin et al. (2019). Additionally, when the levels of voltage are increased in Lin et al. (2019) as compared to the suggested novel topology, the cost function is increased. Nine-level topologies presented in Siddique et al. (2019) as well as in Sathik and Vijayakumar (2019) have the least voltage gain, and hence they require additional boosting circuit to increase the gain. It has been seen from Table 5 that the cost functions of the NPC, FC and CHB are quite high as compared to the proposed topology. These features prove the structural design is more advanced and cost-effective.

## 7. Conclusion

This paper presents a novel self-balanced 13-level SC inverter. The special features of the suggested topology are boosting ability, reduced device count, and the advantage of the maximum blocking voltage of all the switching components being restricted below the peak load voltage. A brief comparative analysis with the recent SC topologies and conventional topologies in terms of the cost function, gain, and component count per level has been presented to prove the merits of the proposed topology. Finally, the simulation and experimental results under steady-state and dynamic conditions prove the performance and usefulness of the proposed topology.

## References

- Leon et al. (2017) "Multilevel Converters: Control and Modulation Techniques for Their Operation and Industrial Applications" *Proceedings of the IEEE*, 105(11).
- Gupta, et al. (2016) "Multilevel inverter topologies with reduced device count: A review," *IEEE Trans. Power Electron.*, 31(1), pp. 135–151.
- Gupta et al. (2012) "Topology for multilevel inverters to attain the maximum number of levels from given DC sources," *IET Power Electron.*, 5(4), pp. 435–446.
- Hinago, et al (2012), "A switched-capacitor inverter using series/parallel conversion with an inductive load," *IEEE Trans. Ind. Electron.*, 59(2), pp. 878–887.
- Babaei, et al. (Sept. 2014.) "Hybrid Multilevel Inverter Using Switched Capacitor Units," *IEEE Trans. Ind. Electron.*, 61(9), pp. 4614–4621.
- Ye et al. (2014), "A Step-Up Switched-Capacitor Multilevel Inverter With Self-Voltage Balancing," *IEEE Trans. Ind. Electron.*, 61(12), pp. 6672–6680.
- Taghvaie, et al. (2018), "A Self-Balanced Step-Up Multilevel Inverter Based on Switched-Capacitor Structure," *IEEE Trans. Ind. Electron.*, 33(1), pp. 199–209.
- Bhatnagar, et al. (2019), "Switched capacitors 9-level module (SC9LM) with reduced device count for multilevel DC to AC power conversion" *IET Electric Power Applications*, 13(10), pp. 1544–1552.
- Lee, et al (2019), "New Family of Boost Switched-Capacitor Seven-Level Inverters (BSC7LI)" *IEEE Trans. on Power Electronics*, 34(11), pp. 10471–10479.
- Samadaei, et al. (2019), "A 13-Levels Module (K-Type) With Two DC Sources for Multilevel Inverters," *IEEE Trans. Ind. Electron.*, 66(7), pp. 5186–5196.
- Roy, et al. "Cross-Switched Multilevel Inverter Using Novel Switched Capacitor Converters, (2020)," *IEEE Transactions on Industrial Electronics*, 66(11), pp. 8521–8532.
- Samadaei, et al. (2016) "An Envelope Type (E-Type) Module: Asymmetric Multilevel Inverters With Reduced Components". *IEEE Trans. Ind. Electron.*, 63(11), pp. 7148–7156.
- Zeng, et al. (2020), "Novel k-type multilevel inverter with reduced components and self-balance," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(4), pp. 4343–4354.
- Khounjahan, et al. (2019) "Switched-Capacitor based Single source Cascaded H-bridge multilevel inverter featuring boosting ability," *IEEE Trans. Power Electron.*, 34(2), pp. 1113–1124.
- Barzegarkhoo, et al. (2016) "Generalized structure for a single-phase switched-capacitor multilevel inverter using new multiple DC-link producers with the reduced number of switches," *IEEE Trans. Power Electron.*, 31(8), pp.5604–5617.
- Saeedian, et al. (2019) "A Novel Step-Up Single Source Multilevel Inverter: Topology, Operating Principle, and Modulation," *IEEE Trans. Power Electron.*, 34(4), pp. 3269–3282.
- Fong, et al. (2019) "Generalized topology of a hybrid switched-capacitor multilevel inverter for high-frequency AC power distribution," *IEEE J. Emerg. Sel. Top. Power Electron*, DOI: 10.1109/JESTPE.2905421.
- Peng, et al., (2019) "Seven-level inverter with self-balanced switched-capacitor and its cascaded extension," *IEEE Transactions on Power Electronics*, 34(12), pp. 11 889–11 896,
- Siddique, et al., (2020) "A new switched capacitor 7l inverter with triple voltage gain and low voltage stress," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 67(7), pp. 1294–1298.
- Lin, et al., (2019) "New Cross-Switch Multilevel Inverter with Self-Voltage Balance and Boost Ability for Microgrid" *4th IEEE Workshop on the Electronic Grid (eGRID)* DOI: 10.1109/eGRID48402.2019.9092633,
- Siddique et.al, (2020) "A Single DC Source Nine-Level Switched-Capacitor Boost Inverter Topology with Reduced Switch Count" *IEEE Access*, 8 pp. 5840–5851.
- Sathik, et al., (2019) "Compact Switched Capacitor Multilevel Inverter (CSCMLI) With Self Voltage Balancing and Boosting Ability" *IEEE Transactions on Power Electronics* 34(5), pp. 4009–4013.
- Siddique, et al., (2020) "Dual asymmetrical dc voltage source base switched capacitor boost multilevel inverter topology" *IET Power Electronics*, 13(7), pp. 1481–1486.
- Iqbal, et al., (2020) "A New Family of Step-Up Hybrid Switched-Capacitor Integrated Multilevel Inverter Topologies With Dual Input Voltage Sources" *IEEE Access* 9(1), pp. 4398–4410.