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# Single-source three-phase switched-capacitor-based MLI

**Research paper**

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**Abstract:** This article proposes a novel three-phase inverter based on the concept of switched capacitors (SCs), which uses a single DC source. A three-phase, seven-level line-to-line output voltage waveform is synthesised by the proposed topology, which includes eight switches, two capacitors, and one diode per phase leg. The proposed topology offers advantages in terms of inherent voltage gain, lower voltage stresses on power switches, and a reduced number of switching components. Additionally, the switched capacitors are self-balanced, thereby eliminating the need for a separate balancing circuit. The proposed structure and its operating principle, the self-balancing mechanism of the capacitors, and the control strategy are all thoroughly explained in the article. The proposed topology has also been compared with some recent SC topologies. Lastly, the proposed topology has been shown to be feasible through simulation and experimentation.

**Keywords:** *multilevel inverter • switched capacitors • multicarrier pulse width modulation • cost function • ANPC inverter*

## 1. Introduction

Multilevel inverters (MLIs) have been extensively researched for low, medium, and highvoltage applications (Abu-Rub et al., 2010; Rodriguez et al., 2002). The special features of MLIs are low levels of voltage stress on the switches, low total harmonic distortion (THD), low d*v*/d*t* stress on the load, low filtering requirements, and high modularity (Gupta et al., 2016). Traditional MLIs comprise three basic topologies, viz. cascaded H-bridge (CHB), flying capacitor (FC), and neutral-point-clamped (NPC) inverters. Each of these has its own pros and cons. For example, the conventional CHB is highly modular but requires electrically isolated DC sources. Similarly, the respective need for clamping diodes and capacitors in NPC and FC topologies, apart from the corresponding voltage balancing issues, pose an important challenge. These undesirable features of traditional inverters limit their applications. In addition, these structures do not offer any inherent voltage gain and, therefore, applications that involve low-voltage DC input (such as photovoltaic [PV] systems and electric vehicle [EV] drives) require a front-end DC–DC boost converter or a back-end transformer, thus causing additional losses and costs (Kerekes et al., 2015; Kjaer et al., 2005). In addition to traditional MLIs, hybrid multilevel topologies, e.g. active NPC (ANPC) inverters, have been continuously researched. An example is a five-level active NPC inverter (5L-ANPC) (Barbosa et al., 2005) that combines the features of a 3L-NPC and a 3L-FC to generate a five-level output voltage waveform. Its advantage is a good trade-off between the reduced number of components and single DC-link operation, but it has no voltage-boosting capability.

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In this context, recent research has been focused on the so-called switched-capacitor-based MLIs (SCMLIs), which can overcome the drawbacks of traditional MLIs. The switched-capacitor principle involves a parallel connection of the capacitors to the DC source for charging and a series connection for discharging. Thus, the SCs add a number of levels to the output waveform and simultaneously offer an inherent voltage gain (Abhilash et al., 2019; Barzegarkhoo et al., 2022; Belkamel et al., 2013; Hinago and Koizumi, 2012; Lee et al., 2019; Raman et al., 2018; Raushan et al., 2016; Roy et al., 2019; Salem et al., 2015; Sathic et al., 2020; Siwakoti et al., 2019; Ye et al., 2014; Zeng et al., 2019). The topologies presented in previous papers (Hinago and Koizumi, 2012; Ye et al., 2014) are based on the SC concept and possess modularity characteristics. However, these topologies are limited by the high voltage stress on the semiconductor switches, making them unsuitable for high-voltage applications. In another paper (Raman et al., 2018), the authors demonstrate how a single unit of the basic cell may generate a seven-level output voltage waveform. While the design includes a symmetrical voltage source, the requirement for numerous sources and polarity generation via an H-bridge make the architecture more expensive and less desirable. The topologies described in similar papers (Lee et al., 2019; Sathic et al., 2020; Zeng et al., 2019) use a larger number of switching components while achieving a low gain. Additionally, another seven-level structure (Abhilash et al., 2019) achieves a gain of less than unity and uses additional switching components. The SCMLI in the work of Roy et al. (2019) synthesises seven levels with a voltage-boosting capability that is three times the input voltage, but it has the disadvantage of causing excessive voltage stress on the switches. The topologies described in other works (Belkamel et al., 2013; Raushan et al., 2016; Salem et al., 2015; Siwakoti et al., 2019) offer a limited voltage gain. Further examples of inverters, suitable for three-phase high-power systems, accomplished on the basis of NPC or ANPC MLIs, are demonstrated elsewhere (Lee and Lee, 2019; Pineda and Rech, 2019; Siwakoti, 2018; Ye et al., 2021; Zeng et al., 2019 Liu et al. 2017).

The above discussion indicates that most SCMLIs have one or more limitations in terms of the requirement for a large number of switching components per level, increased voltage stress on the switches, and low voltage gain. In this work, a novel SCMLI has been proposed with the following distinct characteristics:

(a) It uses a single DC source to synthesise a multilevel three-phase stepped-up output.
(b) The fundamental unit of the proposed structure can generate a four-level waveform as the pole voltage. Thus, the topology synthesises seven levels in the line voltages.
(c) It offers an inherent voltage gain equal to '3'.
(d) The capacitors are self-balanced.
(e) A reduced number of switching components per level is required.

# 2. Proposed Topology

## 2.1. Circuit description

Figure 1 shows the power circuit of the proposed three-phase topology. Each phase leg is composed of eight power switches $S_{Xi}$ ($i$ = 1, 2, ..., 8), one power diode ($D_X$), and two capacitors ($C_{X1}$ and $C_{X2}$), where X ∈ phases (*R, Y, B*). It requires a single DC input, shown with a voltage source $V_{DC}$. When considering the pole voltage $V_{Xo}(t)$, the proposed topology can generate four levels, viz. 0, $+V_{DC}$, $+2V_{DC}$, and $+3V_{DC}$. However, when considering the line-to-line voltage, the proposed topology can synthesise a seven-level waveform across the load terminals, viz. 0, $\pm V_{DC}$, $\pm 2V_{DC}$, and $\pm 3V_{DC}$. All of the power switches have voltage stress equal to the input voltage, with the exception of switch $S_{X5}$ (that has $2V_{DC}$). Thus, the voltage ratings of the power switches are less than the peak value of the output waveform, which is one of the essential advantages for medium- and high-voltage applications. For a better understanding of the analysis, consider leg *R*, for which Table 1 summarises the valid switching states.

## 2.2. Modes of operation for pole voltage

The operating concept of pole voltage ($\boldsymbol{V_{RO}}$) for the phase *R* is explained in this section, and a similar analysis can be performed for the other two phases. The following modes can be used to describe the whole operating range of the suggested topology.

$$Mode\ I\colon V_{RO}(t) = 0$$

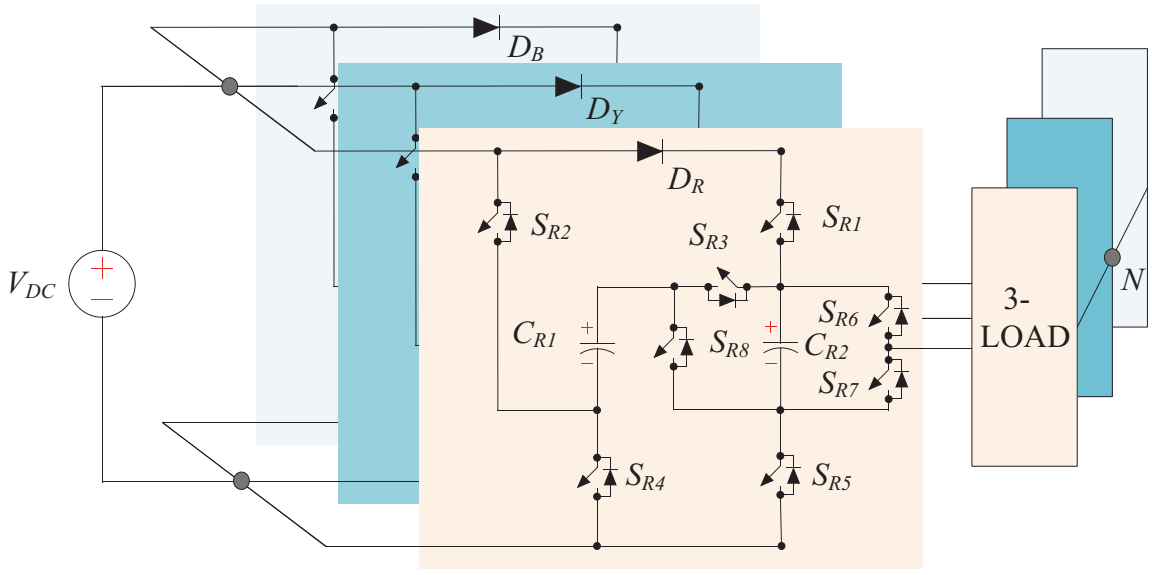


**Fig. 1.** Schematic diagram of the proposed three-phase switched-capacitor-based inverter topology.

| Mode | Active switch | | | | | | | | $V_{Ro}(t)$ |
|---|---|---|---|---|---|---|---|---|---|
| | $S_{R1}$ | $S_{R2}$ | $S_{R3}$ | $S_{R4}$ | $S_{R5}$ | $S_{R6}$ | $S_{R7}$ | $S_{R8}$ | |
| I | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| II | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | $V_{DC}$ |
| III | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | $2V_{DC}$ |
| V | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | $3V_{DC}$ |

**Table 1.** Valid switching states for leg *R* ('1' = on, '0' = off).

Under this mode, the switching combination generates zero output voltage levels across the terminals '*R*' and '0', which is depicted in Figure 2(a). Here, due to the conduction of the switch $S_{R1}$, the capacitor $C_{R2}$ gets charged to a voltage approximately equal to that of the input voltage source, $V_{DC}$. Similarly, the switch $S_{R4}$ conducts to charge the capacitor $C_{R1}$ to $V_{DC}$. As shown in Figure 2(a), the entire process of generating zero voltage levels and the charging of capacitors $C_{R1}$ and $C_{R2}$ can be observed. The red lines show the current that flows via the load terminals, while the green lines represent the current flowing to the charging of the capacitors. Figure 2(b) depicts the load current in the negative direction.

$$Mode\ II: V_{RO}(t) = +V_{DC}$$

Under this mode of operation, the switches $S_{R1,}$ $S_{R3}$, $S_{R4,}$ $S_{R5}$, and $S_{R6}$ conduct simultaneously to achieve $+V_{DC}$ at the load terminals, while the capacitors $C_{R1}$ and $C_{R2}$ get charged to $V_{DC}$. The corresponding conduction paths for this mode are illustrated in Figures 2(c) and 2(d).

$$Mode\ III: V_{RO}(t) = +2V_{DC}$$

In this mode of operation, the proposed topology generates a voltage level that is twice the magnitude of the input voltage source. In this case, the switches $S_{R2}$, $S_{R3}$, and $S_{R6}$ are turned on simultaneously, and

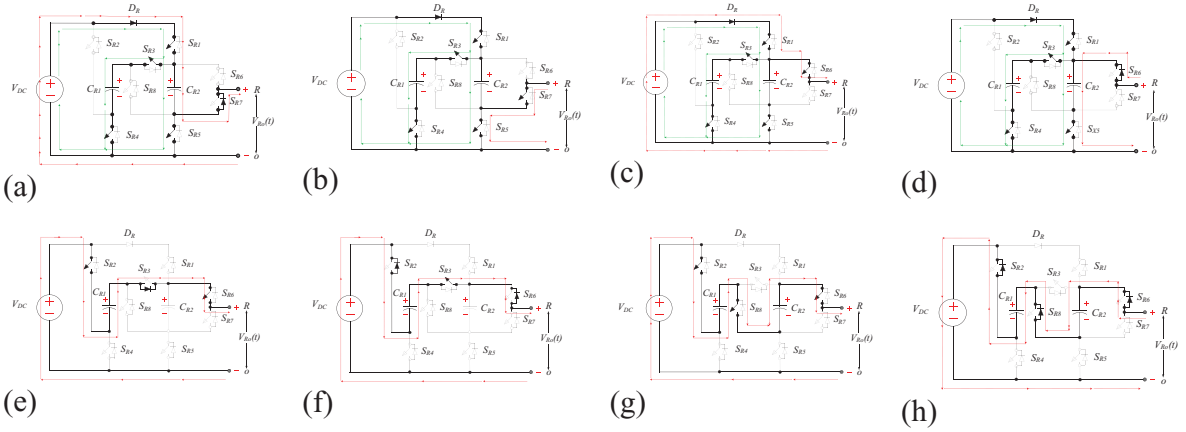


**Fig. 2.** Conduction paths under different operating modes for leg *R* (for positive and negative load currents) (a) $V_{RO}(t) = 0, i(t) > 0$ (b) $V_{RO}(t) = 0, i(t) < 0$. (c) $V_{RO}(t) = +V_{DC}, i(t) > 0$ (d) $V_{RO}(t) = +V_{DC}, i(t) < 0$ (e) $V_{RO}(t) = +V_{DC}, i(t) > 0$, (f) $V_{RO}(t) = +2V_{DC}, i(t) < 0$ (g) $V_{RO}(t) = +3V_{DC}, i(t) > 0$ (h) $V_{RO}(t) = +3V_{DC}, i(t) < 0$.

capacitor $C_{R1}$ gets discharged to the load, while being in series with the input DC source. Hence, the output level becomes $2V_{DC}$. Figures 2(e) and 2(f) show this mode of operation under positive and negative load currents, respectively.

$$Mode\ IV: V_{RO}(t) = +3V_{DC}$$

Under this mode of operation, both capacitors $C_{R1}$ and $C_{R2}$ get discharged to the load along with the input voltage, all being in series, thereby synthesising a voltage of $3V_{DC}$ at the load terminals. Figures 2(g) and 2(h) clearly show this mode of operation for positive and negative load currents, respectively.

## 2.3. Selection criteria for the optimum value of capacitance

For phase *R* of the proposed topology, the capacitors $C_{R1}$ and $C_{R2}$ get charged up to $V_{DC}$. This is accomplished by activating such paths that result in the capacitors being connected in parallel to the input voltage source. In contrast, when the capacitors are connected in series with the source, they get discharged. An exactly similar phenomenon takes place in the other two legs, too. Among the most important factors affecting the discharging characteristics of the capacitors are the following: (i) load type; (ii) longest discharging time; and (iii) power factor angle of the load. As a result, the following is a general description of the maximum amount of discharge in the capacitor:

$$\Delta Q_{C,i} = \int_{\theta_i}^{\pi-\theta_i} I_l(\theta)\mathrm{d}\omega t. \tag{1}$$

With reference to Figures 3 and 4, which respectively show the switching scheme with reference and carrier waveforms, the following can be defined:

$$M = \frac{A_{ref}}{3A_C} \tag{2}$$

$$\theta = \arcsin\left(\frac{1}{3M}\right) \tag{3}$$

where $A_{ref}$ is the amplitude of the sinusoidal waveform, $A_C$ is the peak-to-peak value of the carriers, and *M* is the modulation index.

When the capacitors are charged and discharged, a voltage ripple appears. Generally, this ripple should not exceed 10% of a given capacitor's voltage. For a purely restive load, which is the worst-case scenario as there is

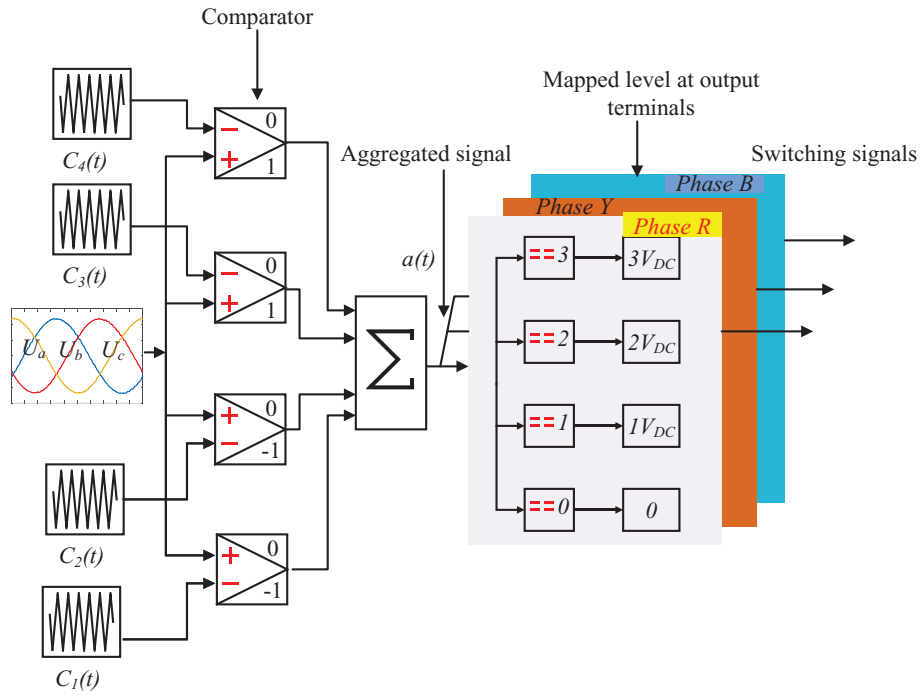


**Fig. 3.** LS-PWM scheme for the proposed topology. LS, level shifted; PWM, pulse width modulation.

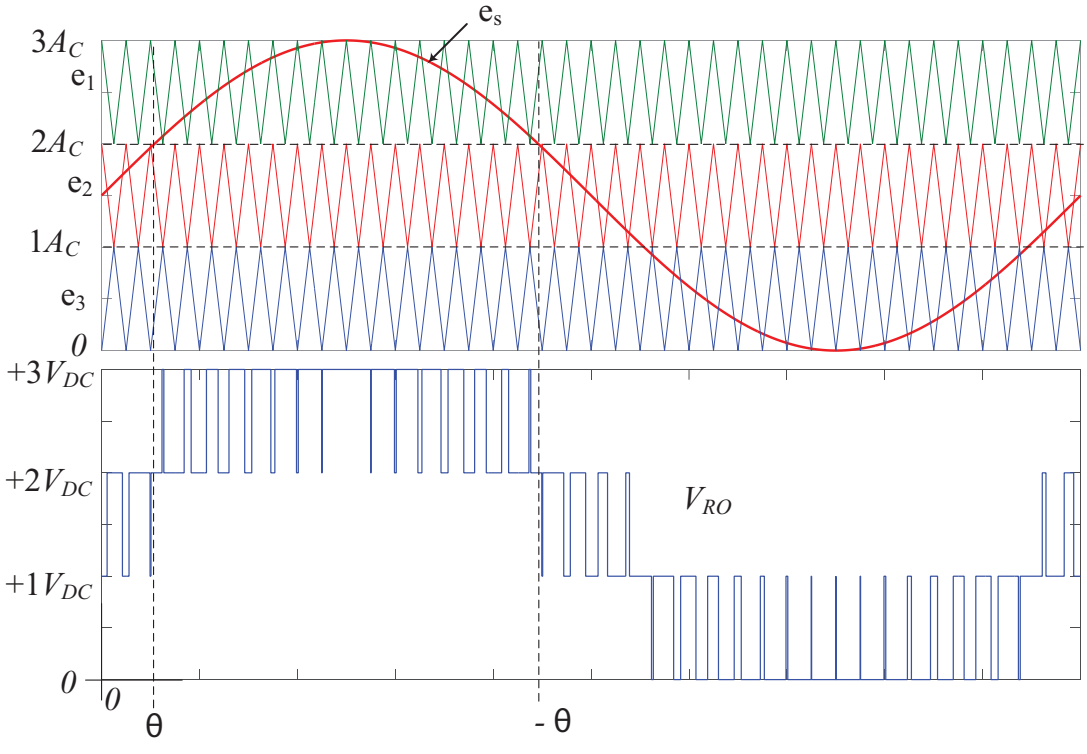


**Fig. 4.** Representation of discharging instant for the evaluation of capacitance value.

no load current flowing back to the capacitors, the voltage ripple can be calculated as follows (Hinago and Koizumi, 2012):

$$\Delta V_{C1} = \frac{1}{\omega C_1}\int_0^{\pi} \frac{2V_{DC}}{R}\mathrm{d}\omega t \tag{4}$$

$$\Delta V_{C1} = \frac{V_{DC}}{fRC_1} \tag{5}$$

$$\Delta V_{C2} = \frac{1}{\omega C_2}\int_{\theta}^{\pi-\theta} \frac{3V_{DC}}{R}\mathrm{d}\omega t \tag{6}$$

$$\Delta V_{C2} = \frac{3V_{DC}}{2\pi fRC_2}\left[\pi - 2\arcsin\left(\frac{1}{3M}\right)\right] \tag{7}$$

Therefore, the capacitance should satisfy the following condition:

$$C_i = \frac{\Delta Q_{C,i}}{\Delta V_{C,i}}. \tag{8}$$

# 3. Modulation Scheme

In the past few decades, several modulation strategies have been implemented to generate gating pulses for MLIs. Among them, the most popular strategies are multi-carrier pulse width modulation (PWM), space vector PWM, space vector control, selective harmonic elimination method, etc. (Blasko, 2007; Chiasson et al., 2003; Taghvaie et al., 2018; Yao et al., 2008). In this work, the level-shifted multi-carrier-based pulse width modulation (LS-PWM) approach has been used. Figure 3 depicts the modulation strategy for the proposed topology. Three triangular carrier signals, viz. $e_1$, $e_2$, and $e_3$, with constant magnitude and frequency, are compared with the modulating signal $e_s$. The latter is a reference sinusoidal signal with a frequency equal to 50 Hz. If the reference signal is greater than the carrier signal above the zero reference, during the comparison, the comparator will output '1'; otherwise, it will output '0'. And if the reference signal is greater than the carrier signal below the zero reference, during the comparison, the comparator will output '0'; otherwise, it will output '–1'.

The comparator output signals are added to produce the aggregated signal '$a(t)$'. By comparing the aggregated signals to their corresponding constant levels, the switching pulses are obtained. The output of the desired signal is then sent to the switches using the mappings illustrated in Figure 3. To obtain a three-phase voltage, each leg is modulated with similar reference signals with a phase difference of 120° between each other. So, the line voltages $V_{RY}$, $V_{YB}$, and $V_{BR}$ are obtained from the pole voltages $V_{Ro}$, $V_{Yo}$, and $V_{Bo}$, as follows:

$$V_{RY} = V_{Ro} - V_{Yo} \tag{9}$$

$$V_{YB} = V_{Yo} - V_{Bo} \tag{10}$$

$$V_{BR} = V_{Bo} - V_{Ro}. \tag{11}$$

# 4. Comparative Analysis

The merits and demerits of the proposed three-phase topology are described in this section with reference to prior art topologies. In an attempt to quantify the above characteristic, two factors are utilised, defined as the

component-to-level factor ($F_{C/L}$) and the cost function (CF) (Panda et al., 2020). These factors are defined as follows:

$$F_{C/L} = \frac{\boldsymbol{N_{SW} + N_C + N_D + N_{Dri} + N_S}}{\boldsymbol{N_L}} \tag{12}$$

$$\mathrm{CF} = \frac{(N_{SW} + N_C + N_D + N_{Dri} + \alpha TSV) \times N_S}{N_L} \tag{13}$$

where the notations represent the following: $N_{SW}$ = the number of switches; $N_C$ = number of capacitors; $N_D$ = number of auxiliary diodes; $N_S$ = number of supply sources $N_L$ = number of pole voltage levels; $N_{Dri}$ = number of driver units; TSV = total standing voltage. Here, '$\alpha$' is the weight factor. The value of $\alpha$ is deemed to be '1, 0' (Panda et al., 2020) when both the switching components and the overall standing voltage are given equal weights.

The maximum blocking voltage (MBV) is the voltage stress across a non-conducting power switch that it must withstand during that state, and it must not exceed the rated value of the power switch; otherwise, the device would undergo breakdown. Table 2 illustrates the brief comparative analysis of the proposed topology with the existing three-phase topologies in terms of component count, cost function, total standing voltage, and voltage gain for a specific number of pole voltage levels. The topologies presented in earlier reports (Raushan et al., 2016; Salem et al., 2014, 2015; and Sander and Yaragatti, 2017) require multiple isolated DC sources. The topology described by Grigoletto (2021) has boosting capability but the voltage level is less as compared to the proposed one. Though the topologies in other similar papers (Lee et al., 2019; Sathic et al., 2020; Ye et al., 2021; Zeng et al., 2019) have voltage-boosting capability, the boosting factor is limited to '1.5', unlike in the proposed topology, which offers a gain of '3.0'. Additionally, the CF of the proposed topology is lower than that of recent topologies. Although the topology in previous works (Abhilash et al., 2019; Siwakoti et al., 2019; Ye et al., 2022; Zhu et al., 2021) has the lowest cost function, it requires a boosting circuit, which adds to the costs and complexity.

| References | $N_L$ | $N_{SW}$ | $N_S$ | $N_D$ | $N_C$ | $N_{Dri}$ | TSV | $F_{C/L}$ | MBV | Gain | Boosting ability | CF |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Salem et al. (2015) | 3 | 4 | 2 | - | - | 4 | 5 | 3.3 | 2 | 1 | No | 8.66 |
| Raushan et al. (2016) | 4 | 6 | 4 | 8 | - | 6 | 22 | 6 | 3 | 0.6 | No | 46 |
| Lee et al. (2019) | 4 | 10 | 1 | - | 4 | 8 | 10 | 5.75 | 1 | 1.5 | Yes | 8 |
| Zeng et al. (2019) | 4 | 9 | 1 | - | 4 | 8 | 16 | 5.5 | 1 | 1.5 | Yes | 9.25 |
| Sathik et al. (2020) | 4 | 10 | 1 | - | 3 | 9 | 10 | 5.75 | 1 | 1.5 | Yes | 8.25 |
| Siwakoti et al. (2019) | 4 | 8 | 1 | - | 4 | 8 | 4.25 | 5.25 | 0.5 | 0.5 | No | 5.32 |
| Abhilash et al. (2019) | 4 | 8 | 1 | - | 3 | 8 | 14 | 5 | 1 | 0.75 | No | 11 |
| Sandeep and Yaragatti (2017) | 5 | 6 | 2 | - | 3 | 3 | 3 | 2.8 | 1 | 1 | No | 6 |
| Salem et al. (2014) | 3 | 4 | 2 | – | – | 4 | 5 | 3.3 | 2 | 1 | No | 8.66 |
| Ye et al. (2022) | 3 | 5 | 1 | 2 | 4 | 5 | 3.25 | 5.66 | 0.5 | 0.5 | No | 6.41 |
| Ye et al. (2021) | 4 | 4 | 1 | 2 | 4 | 4 | 8 | 3.76 | 2 | 1.5 | Yes | 5.35 |
| Zhu et al. (2021) | 2 | 6 | 1 | - | 2 | 6 | 4 | 7.5 | 1 | 0.5 | No | 9 |
| Grigoletto (2021) | 3 | 5 | 1 | - | 1 | 5 | 6 | 4 | 2 | 2 | Yes | 5.66 |
| Proposed topology | 4 | 8 | 1 | 1 | 2 | 8 | 8 | 5 | 3 | 3 | Yes | 6.75 |

CF, cost function; $F_{C/L}$, component-to-level factor; MBV, maximum blocking voltage; $N_c$, number of capacitors; $N_D$, number of auxiliary diodes; $N_{Dri}$, number of driver units; $N_L$, number of pole voltage levels; $N_s$, number of supply sources; $N_{sw}$, the number of switches; TSV, total standing voltage.

**Table 2.** Quantitative comparison of the proposed per-phase topology with recent topologies.

# 5. Results and Discussion

Using the modulation scheme as described previously, the proposed topology is simulated in the MATLAB/Simulink environment. Furthermore, the viability of the proposed topology has been verified by carrying out experimental studies on a laboratory-based prototype. Table 3 represents the circuit parameters used for the simulation and experimental studies.

## 5.1. Simulation results

The simulation results with an *R–L* load are shown in Figure 5. The three-phase line voltages are shown in Figure 5(a), while the pole voltage waveforms are shown in Figure 5(b). It has been observed from the waveforms that line voltages have seven levels (0, ±100 V, ±200 V, ±300 V) and are not affected by a sudden change in load, shown in Figure 5(c). Moreover, the pole voltages have four equal step-sized levels (0, +100 V, +200 V, +300 V). The load current is shown in Figure 5(c) under dynamic conditions. For better analysis, the effect of the load change on line voltage, line current, and capacitor voltage for phase *R* are shown in Figure 5(d). It indicates that the capacitor maintains natural balancing under load changes, and the magnitude of the line voltage is unaffected. The voltage stresses are within the supply voltage, i.e. 100 V each on ($S_{R1}$–$S_{R4}$) and ($S_{R6}$–$S_{R8}$), except for the switch $S_{R5}$ shown in Figures 5(e) and 5(f). Figure 5(g) shows the current stress capacitance of capacitors $V_{CR1}$ and $V_{CR2}$. Figures 5(h) and 5(i) illustrate the current stress of all eight switches (per phase leg R) with a load parameter of 80 mH and 50 Ω. In the charging loop of both capacitors, four switches are present, i.e. $S_{R1}$, $S_{R3}$, $S_{R4,}$ and $S_{R5}$, which need to meet the current rating, which is equal to the sum of the changing and load currents. Considering the R–L load of R=50 Ω and L=80 mH, fast Fourier transform (FFT) analysis of the line voltage $V_{RY}$ and the phase voltage $V_{RN}$ provides the maximum magnitude of the fundamental voltage of 140.6 V and 242.6 **V** with 32.11% and 31.96% of THD, respectively as shown in Figures 5(j) and 5(k).

## 5.2. Experimental results

An experimental verification of a laboratory prototype has been conducted to determine the viability of the proposed three-phase, seven-level topology. Figure 6 shows the experimental waveforms. Figures 6(a)–6(c) illustrate the waveforms of pole voltages, line voltages, and load currents, respectively. A pole voltage is shown in Figure 6(a). The pole voltage has four levels. The levels are +300 V, +200 V, +100 V, and 0 **V**. The observed output voltage (Figure 6(b)) undeniably generated seven voltage levels, with the voltage magnitude of each level being 100 V. It can be seen that the maximum voltage level of 300 V also conformed to a boosting gain of '3'. These observations are in good agreement with the theoretical analysis presented in Figure 2. The line voltage obtained by the experimental arrangement is found to be quite close to the simulation results. Additionally, it can be shown that the magnitude of the line voltage remains unchanged during a sudden change in load. Figure 6(c) shows the line current under sudden change in load. Figure 6(d) depicts the phase R's line voltage, load current, and capacitor voltage more clearly, providing for a better comprehension of line voltage and capacitor voltage under dynamic settings. The voltage across the floating capacitors remains intact under different loading conditions. It clearly indicates that the voltages across the floating capacitors are balanced

| Parameter | Value/Part no. |
|---|---|
| Input DC voltage | 100 V |
| Output voltage frequency | 50 Hz |
| Carrier frequency | 2 kHz |
| Load (*R–L*) | 50 Ω, 80 mH |
| Load (*R*) | 100 Ω |
| Capacitors (*CXi*) | *CR*1 = 2,200 μF, *CR*2 = 1,800 μF (LGX2D222MELC50) |
| Power switches (IGBTs) | GW30NC120HD |
| Modulation index | 0.95 |

IGBT, insulated-gate bipolar transistor.

**Table 3.** Parameters for simulation and experimental studies.

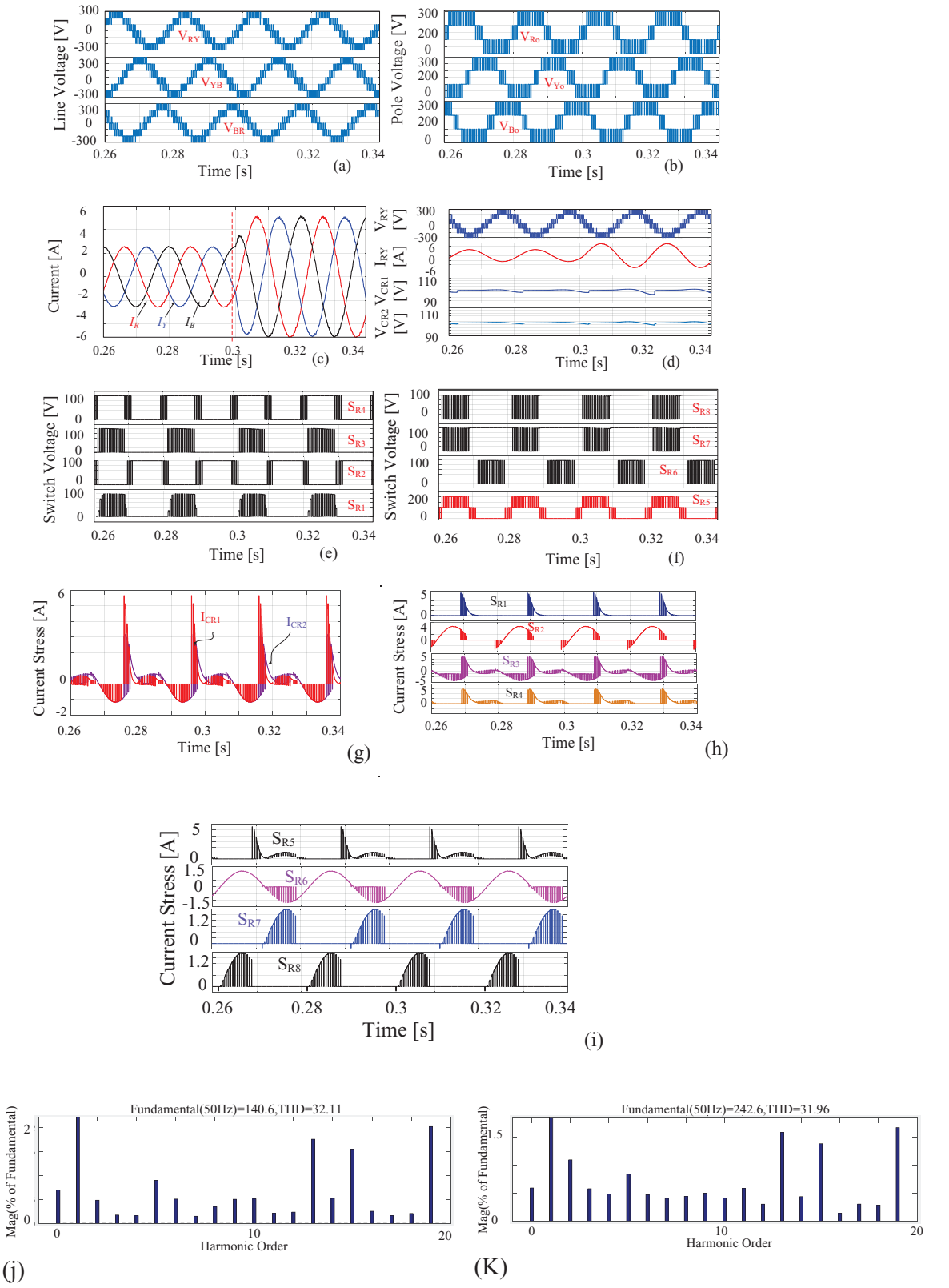


**Fig. 5.** Simulation results: (a) line voltages; (b) pole voltages; (c) load currents; (d) line voltage, load current, and voltage across the capacitors CR1 and CR2; (e) and (f) voltage stress of all switches ($S_{R1}$_$S_{R8}$); (g) voltage stress of the capacitors (h-i) current stress of switches ($S_{R1}$~$S_{R8}$ )(j) FFT analysis of $V_{RY}$; (k) FFT analysis of $V_{RN.}$ FFT, fast Fourier transform; $V_{RN,}$ phase voltage; $V_{RY,}$ line voltages.

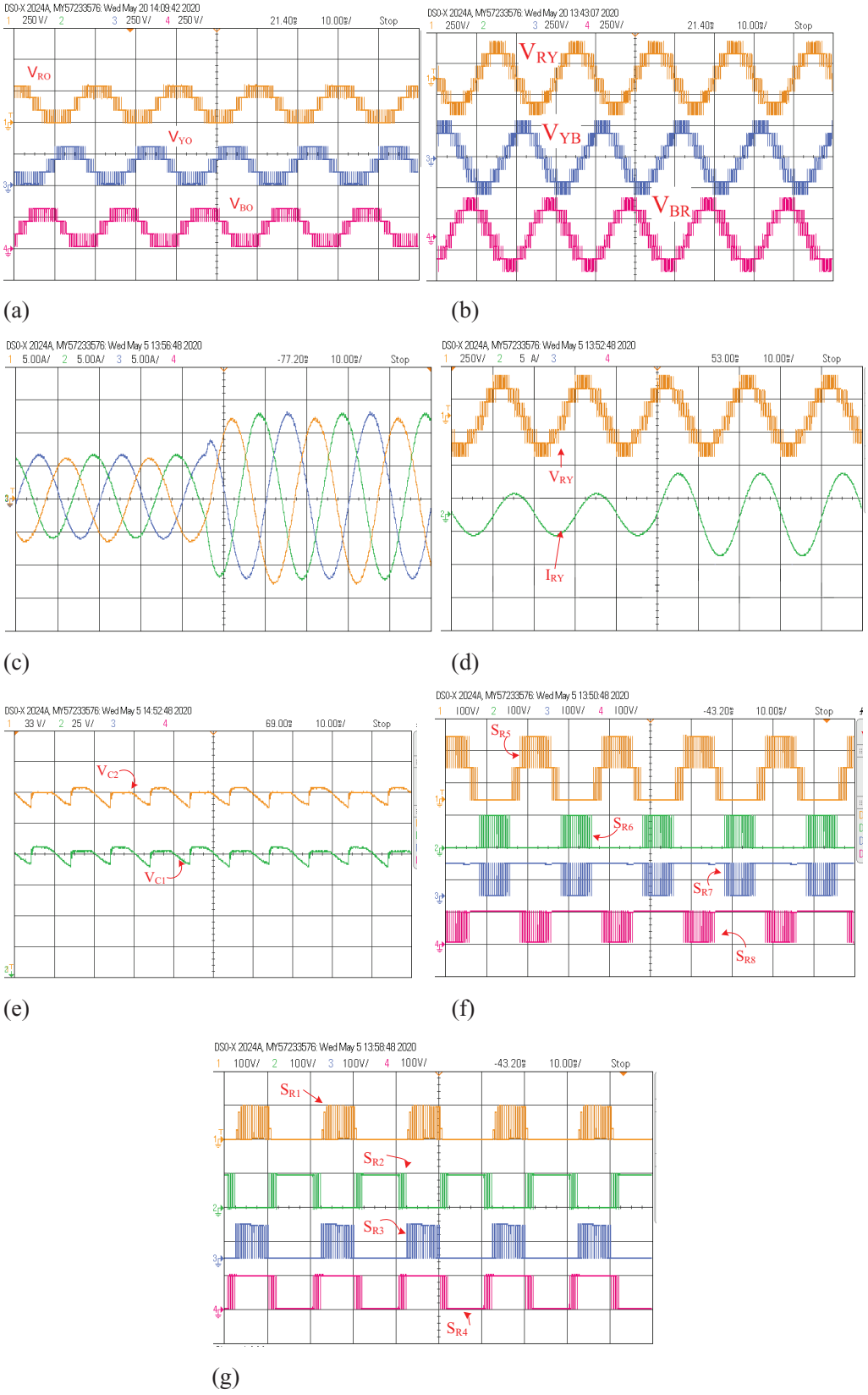


**Fig. 6.** Experimental results under balanced load conditions: (a) pole voltages; (b) line voltages; (c) load currents; (d) line voltage and load current for phase *R*; (e) capacitor voltages for phase leg *R*; (f) and (g) voltage stresses across all switches.

around an average value of 100 V (Figure 6(e)), which verifies their self-voltage-balancing capability. Figures 6(f) and 6(g) show voltages across all of the switches, which demonstrates that the voltage stresses on the switches $S_{R1}$–$S_{R4}$ and $S_{R6}$–$S_{R8}$ are within the supply voltage range, whereas the voltage stresses on the switch $S_{R5}$ are double the supply voltage range. The experimental configuration achieves an efficiency of 94.42%, which is a little less than the simulated efficiency. This could be a result of the increased losses in driving circuits. As a result, the outstanding performance of the proposed three-phase topology is confirmed by the above-mentioned experimental results.

# 6. Discussions of Results and Their Relevance

The modelling and experimental findings for the suggested design show that a seven-level waveform with thrice the voltage gain is produced. The selected values guarantee that the capacitors perform well in terms of voltage ripples under a rated load. Based on a review of the SCMLI literature, the following applications for the proposed topology have been identified.

(a) High-frequency AC distribution

Due to a significant reduction in the quantity of power conversion stages, transformer size, and filter size, the high-frequency alternating current (HFAC) power distribution system (PDS) has gained popularity in high-power-density applications such as telecommunication, spacecraft, and computer systems (Chen et al., 2016). Another novel use for this technology is the use of an HFAC PDS in small-scale networks, such as micro-grids and -structures (Antaloae et al., 2011). SCMLIs have consequently emerged as the favoured option for HFAC applications (Jena et al., 2021). At low-voltage sites, SCMLI topologies eliminate the requirement for magnetic circuits or DC–DC boost converters.

(b) EV traction systems and PV-based power generation systems

Renewable energy sources, such as PV systems, have a modest power output. Cascading PV modules, DC–DC boost inverters, or step-up transformers are the three methods for boosting voltage. Each of these techniques results in a rise in costs, volume, component count, and power losses (Kuncham et al., 2020). SCMLIs, however, offer a decent voltage gain, capacitor self-balancing, high-resolution waveforms for grid compatibility, and reduced filtering needs (Chen et al., 2021; Jena et al., 2022).

# 7. Conclusion

This article describes a novel three-phase step-up single-source inverter with a voltage gain of ‘3’. It generates four levels at the poles and seven levels in the line voltages. Comparisons with existing three-phase topologies in terms of voltage-boosting ability, gain, component count per level, and cost function demonstrate that the suggested topology is highly competent. The validity of the proposed inverter has been confirmed with both simulation and experimental results.

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